Integratie van fotodetectoren op siliciumgebaseerde fotonische circuits voor spectroscopische toepassingen

Integration of Photodetectors on Silicon Photonic Integrated Circuits (PICs) for Spectroscopic Applications

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Proefschrift ingediend tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Informatietechnologie
Voorzitter: prof. dr. ir. D. De Zutter
Faculteit Ingenieurswetenschappen
Academiejaar 2010 - 2011

UNIVERSITEIT GENT

ISBN 978-90-8578-384-8
NUR 959, 926
Wettelijk depot: D/2010/10.500/60

Universiteit Gent
Faculteit Ingenieurswetenschappen
Vakgroep Informatietechnologie

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Dit werk werd uitgevoerd in het kader van het IWT/SBO epSOC project.

Dankwoord

Doctoreren, vijf jaar lang, het waren mooie tijden! Het was wetenschappelijk onderzoek kunnen doen in bijna alle vrijheid. Dit biedt mogelijkheden die je niet hebt wanneer je onmiddellijk na je studies in het bedrijfsleven stapt: samenwerken met een jonge groep enthousiaste collega's, naar conferenties gaan in het buitenland en je soms nog eens draaien wanneer de wekker 's morgens veel te vroeg afgaat en je vriendin tegen haar zin uit bed rolt.

Eerst en vooral zou ik Roel willen bedanken die een fantastische onderzoeksgroep opgebouwd heeft gedurende al die jaren en die mij de mogelijkheid geboden heeft om onderzoek te kunnen doen in een groep die wereldwijd erkenning geniet en baanbrekend werk verricht. Mijn promoter Dries, bedankt voor de motivatie, de nieuwe inzichten, de interessante discussies, de goede tips en vooral de steun. En tenslotte Gunther, dankzij jou heb ik de smaak voor wetenschappelijk onderzoek te pakken gekregen. Je was een uitstekende thesisbegeleider en fijne collega.

Dit werk zou nooit tot stand gekomen zijn zonder de steun van vele mensen. Liesbet, Steven, jullie hielden de cleanroom draaiende. Mister Yu, thanks for the etching. Mijn epSOC collega's: Kasia en Denis, het waren leuke tijden! Merci voor de lekkere vodka en het gezelschap op de trein. My nice foreign colleagues: Shankar, Gunay, Stevan, Shahram, Khai. Thanks to you guys, my English is not that bad as it would have been without you. Hendrik en Jeroen, dankzij jullie lagen de meetsetups er altijd (of bijna altijd) voorbeeldig bij. Mijn thesisstudenten die ik begeleid heb: Elisa, Meng Yee, Alvaro. Hopelijk vonden jullie het even boeiend als ik. Wim, voor het aanhoren van mijn gezeur over Python en tenslotte nog het financiële en administratieve team en de vele mensen die ik hier niet allemaal kan opnoemen.

Mijn bureaugenoten van de laatste jaren verdienen hier een bijzondere vermelding: Koen, Elewout, Wout en Kristof, jullie waren een toffe, attente

bende, zowel overdag als 's nachts. Dat mountainbiken komt er heus wel nog eens van.

Iedereen weet ook dat de boog niet altijd gespannen kan staan en dat de beste ideeën vaak onstaan bij een kruik gerstenat of een glaazeke Schots water. De Marimain en de Vooruit lagen gelukkig niet veraf. Met de leuze "Eentje is geentje" in ons achterhoofd hebben we meermaals de werkdag goed doorgespoeld. De spurtjes naar mijn laatste trein en de gekrompen jas zal ik nooit vergeten. Bedankt gasten, dat waren memorabele momenten.

Dan zijn er nog mijn collega's met wie ik recent in een spannend avontuur gestapt ben: Jonathan, Dirk en William, hopelijk brengen we dit tot een goed einde.

Ook mijn vrienden moet ik hier bedanken voor de mooie momenten en om me te gepasten tijde te vragen wat ik nu juist weer deed aan "den Unif". Ben je nu eigenlijk al afgestudeerd? Verdien je nu al geld? Hoe zit dat nu weeral met die chips? Heb je nu al iets uitgevonden? Wie betaalt dat eigenlijk allemaal, wij zeker? ... Hehe.

Tenslotte - maar eigenlijk horen deze mensen bovenaan in dit dankwoordlijstje - wil ik mijn ouders, Silke, Nele en Lore bedanken. Pa en ma, bedankt om er altijd te zijn voor mij, de goede raad, het lekkere eten, ... Siel, je ben een sjieke zus. Nele, zonder jou zou dit dankwoord zonder twijfel nooit bestaan hebben. Merci voor je steun, ik zie je graag en ik ben er zeker van dat er ons nog fantastische tijden te wachten staan. Tenslotte, Lore, je ben nog steeds de kleinste, maar je betekent o zoveel voor ons. De slapeloze nachten neem ik er graag bij!

Bedankt en veel leesplezier!

Gent, oktober 2010
Joost Brouckaert

Table of Contents

Nederlandstalige samenvatting

1. Siliciumgebaseerde fotonisch geïntegreerde circuits

Een aanzienlijk deel van de totale kostprijs van klassieke optische systemen is de verpakking ervan. Deze optische systemen bestaan uit een combinatie van afzonderlijke subcomponenten (lasers, filters, lenzen, ...) die allemaal afzonderlijk gefabriceerd, gemonteerd en gealigneerd moeten worden ten opzichte van elkaar in eenzelfde verpakking met zeer nauwkeurige, veelal sub-micrometer toleranties. Dit vereist zeer accurate en daarom tijdrovende en dure mechanische alignatieprocessen. Door gebruik te maken van fotonisch geïntegreerde circuits kan de kostprijs sterk gereduceerd worden omdat er geen individuele subcomponenten zijn die afzonderlijk gemonteerd dienen te worden. In dit geval wordt het licht door middel van optische golfgeleiders naar de verschillende geïntegreerde componenten gestuurd. De fabricage van deze componenten met hun verbindingsgolfgeleiders gebeurt collectief, op wafer schaal en door middel van lithografische technieken en etsprocessen.

Silicium is een uitstekend materiaal voor de fabricage van passieve fotonisch geïntegreerde circuits (PICs) zoals optische filters. Het silicium-op-isolator (SOI) materiaal systeem beschikt over unieke optische eigenschappen: het brekingsindex verschil tussen silicium en isolator (silica, SiO_2) is zeer groot. Dit maakt de fabricage van zeer compacte golfgeleiders en optische filters op een zeer klein chip oppervlakte mogelijk. Om licht te geleiden tussen twee punten op de chip worden "fotonische draden" (Eng: photonic wires) gebruikt. Dit zijn lichtbaantjes met typische dimensies van slechts een aantal honderden nanometers die zeer compacte bochten kunnen maken met een bochtstraal van 1μm zonder extra verlies. Deze golfgeleiders en optische filters worden op 200mm SOI wafers vervaardigd door middel van dezelfde fabricagetoestellen die ook in de CMOS wereld gebruikt worden voor het maken van digitale elektronische ICs.

De doelstelling van dit werk is de fabricage van siliciumgebaseerde

PICs voor spectroscopische toepassingen. We spitsen ons voornamelijk toe op WDM (Wavelength division multiplexing) ontvangers voor optische communicatie enerzijds en spectrometers voor nabij-infrarood spectroscopie toepassingen anderzijds. Voor deze toepassingen moeten zowel aktieve als passieve componenten geïntegreerd worden op dezelfde chip: fotodetectoren moeten geïntegreerd worden met passieve optische filters vervaardigd in silicium.

Deze thesis bestaat uit drie grote delen. In het eerste deel beschrijven we het ontwerp en de karakterisatie van deze optische filters. Het tweede deel gaat over de technologie en het ontwerp van fotodetectoren. In het laatste deel geven we een overzicht van enkele gefabriceerde SOI PICs met geïntegreerde detectoren.

2. Optische filters vervaardigd in silicium

Het hart van elke spectrometer is de optische filter. Deze moet de verschillende golflengtes waaruit het ingangssignaal bestaat scheiden en geleiden naar verschillende locaties op de chip waar de signaalsterkte gemeten kan worden door middel van fotodetectoren. In dit werk fabriceerden we voor de eerste keer zogenaamde planaire en concave diffractieroosters (PCGs) op een nanofotonisch SOI platform. Om deze componenten te ontwerpen en om hun filterkarakteristieken te simuleren schreven we simulatiesoftware, gebaseerd op scalaire diffractie theorie. Vergelijkingen tussen metingen en simulaties toonden aan dat er een goede overeenkomst is tussen beiden waaruit we konden besluiten dat we over een krachtige tool beschikten om deze PCGs te ontwerpen. Het programma is geïmplementeerd in Matlab and berekent eveneens de coördinaten die nodig zijn om de lithografie maskers te maken die gebruikt worden tijdens de fabricage.

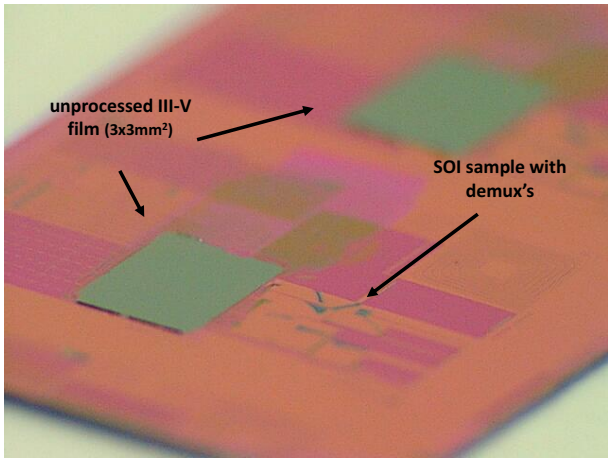
We hebben zeer compacte optische filters gefabriceerd die werkzaam zijn rond golflengtes van 1.55μm en met kanaalspatiëringen gaande van 60nm voor Fiber to the Home (FTTH) toepassingen tot 1nm voor uitleestoestellen voor optische vezelgebaseerde Bragg rooster sensors. Deze sensoren worden onder andere gebruikt om spanningen in bruggen en vliegtuigvleugels te meten. Eén van de grootste verwezenlijkingen is dat we erin geslaagd zijn om het verlies van deze componenten te reduceren tot 1.9dB zonder gebruik te maken van extra proces stappen. We hebben ook coarse WDM (CWDM) filters vervaardigd met een isolatie tussen de verschillende kanalen die beter was dan 30dB. Toch merkten we op dat PCGs met een hoge resolutie gevoeliger zijn voor kleine afwijkingen tijdens de

fabricage dan filters die gebruikt worden voor bredere golflengte filtering. Dit resulteerde in een verminderde performantie op het gebied van overspraak. Om dit probleem op te lossen hebben we ook complexere filters onderzocht die gebruik maken van een combinatie van ring resonatoren met PCGs. De bedoeling hierbij is dat een PCGs een eerste "ruwe"filtering doet van het ingangssignaal (bijv. 10 kanalen met een spatiëring van 10nm) en dat ring resonatoren vervolgens een zeer smalle piek ($<$0.2nm) uit elk kanaal filteren.

3. Heterogene integratie

Silicium is transparant in het nabije-infrarood golflengte gebied dat typisch gebruikt wordt voor optische telecommunicatie (1.31 and 1.55μm). Om bij deze golflengtes op een efficiënte manier licht te detecteren moeten er andere halfgeleider materialen geïntegreerd worden op de silicium chip. Commerciële fotodetectoren voor telecom toepassingen maken gebruik van III-V halfgeleiders, typisch InP/InGaAs. De heterogene integratie van deze halfgeleiders op silicium kan op verschillende manieren gebeuren. Onze aanpak is gebaseerd op het kleven (bonden) van niet-geproceste III-V dies op de SOI golfgeleider wafer. Daarbij maken we gebruik van een intermediaire bondinglaag, namelijk het polymeer BCB (Benzocyclobutene). Op het ogenblik van het bonden zijn de III-V dies nog niet bewerkt. Hierdoor is geen nauwkeurige alignatie vereist en een snelle "pick-and-place" procedure kan het werk doen. Na het bonden worden de InP substraten verwijderd (deze hebben toch geen optische functie) zodanig dat we meerdere zeer dunne III-V films bekomen op de SOI golfgeleider wafer. Dit is te zien in figuur 1. Hierna kunnen alle fotodetectoren op de volledige 200mm SOI wafer gelijktijdig gefabriceerd worden. Tijdens de verschillende fabricage processen van de detectoren (etsen, metallisatie, ...) gebeurt de alignatie ten opzichte van de onderliggende silicium golfgeleiders door middel van zeer nauwkeurige optische lithografie.

De Photonics research groep heeft in de voorbije jaren heel wat expertise opgebouwd in dit domein. Om echter op een efficiënte manier licht te kunnen kopppelen van de silicium golfgeleiders naar de detectoren die zich erboven bevinden moet de intermediare BCB bondinglaag zeer dun zijn. Tijdens dit onderzoek hebben we een integratieproces ontwikkeld die gebaseerd is op manuele bonding van III-V dies op SOI waarbij gebruik gemaakt werd van BCB bondinglagen dunner dan 300nm. Dit proces heeft een hoge yield en we toonden aan dat het mogelijk is om meerdere dies



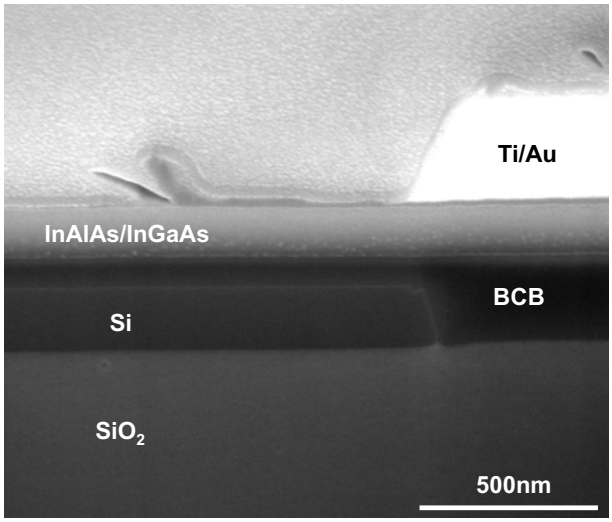
Figuur 1: Twee nog niet geproceste III-V dunne films ($3\times3\text{mm}^2$) gebond d.m.v. BCB op een SOI substraat

tergerlijkertijd te bonden. Toch is het belangrijk om op te merken dat een geautomatiseerde aanpak noodzakelijk is om een matuur fabricageproces te bekomen dat geschikt is voor commerciële toepassingen.

4. InGaAs-op-SOI fotodetectoren

Tijdens dit onderzoek hebben we zeer efficiënte InGaAs fotodetectoren ontwikkeld en vervaardigd. Deze detectoren zijn gekoppeld met SOI golfgeleiders. Ze zijn zeer compact (korter dan 20μm) en hebben een respons van 1A/W bij een golflengte van 1.55μm. Dit komt overeen met een quantum efficiëntie van 80%. De donkerstroom bedraag 5nA en de vermogen-fotostroom karakteristiek is lineair over een bereik dat groter is dan 40dB. Door de lengte van de detector en/of de dikte van de bondinglaag te variëren is het mogelijk om slechts een klein deel van het optisch vermogen in de golfgeleider af te takken voor vermogen-monitor toepassingen. We hebben rijen gemaakt van 100 detectoren op een zeer kleine pitch van 25μm zonder ook maar één defecte detector.

Simulatieresultaten tonen aan dat elektrische modulatiebandbreedtes tot 30GHz bereikt kunnen worden door gebruik te maken van standaard kontakt lithografie. Eerst metingen toonden optische bandbreedtes van 9.5GHz aan. Figuur 2 is een dwarsdoorsnede van een InGaAs detector, gebond op een silicium golfgeleider door middel van een 100nm dikke



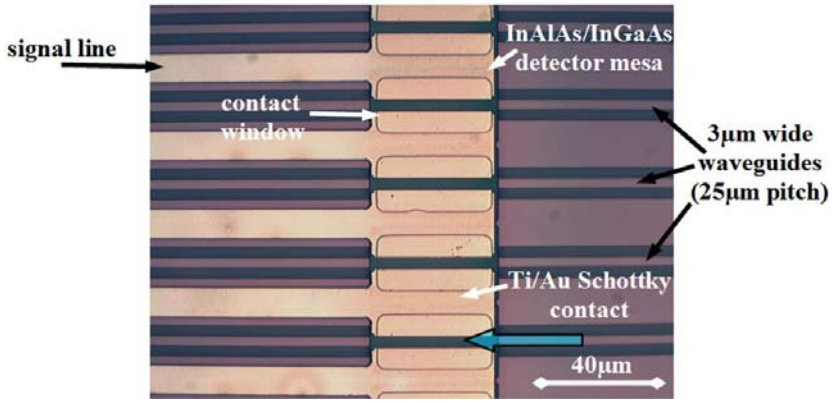
Figuur 2: Elektronen microscoop dwarsdoorsnede van een InGaAs detector gebond op een silicium golfgeleider d.m.v. een 100nm dikke BCB laag. Enkel de rechter helft is zichtbaar

BCB laag.

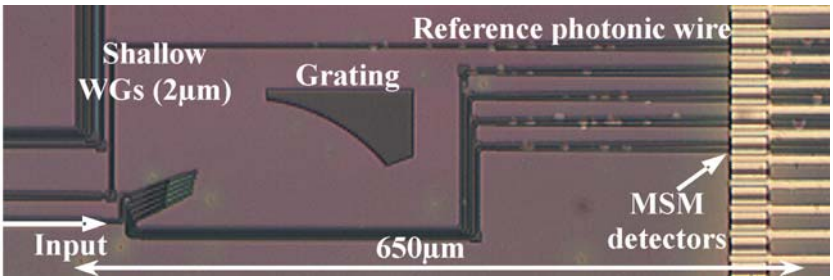
De goede performantie van deze detectoren was het resultaat van een doorgedreven procesoptimalisatie. Onze eerste componenten vertoonden verschillende problemen: een hoge donkerstroom, asymmetrisch gedrag en een grote winst bij lage vermogens. Deze problemen konden uiteindelijk opgelost worden door de droge etsstappen voor de definitie van de mesas en de contactopeningen te optimaliseren. Figuur 3 is een bovenaanzicht van een rij van verschillende 40μm lange fotodetectoren, gebond op silicium golfgeleiders. De afstand tussen deze golfgeleiders is 25μm.

5. PICs met actieve en passieve componenten

In het laatste hoofdstuk demonstreerden we SOI PICs met geïntegreerde fotodetectoren voor verschillende toepassingen: vermogen monitors, WDM ontvangers voor on-chip optische verbindingen, CWDM en FTTH ontvangers voor telecom toepassingen en een 30-kanaals nabij-infrarode spectrometer. Figuur 4 is een bovenaanzicht van de CWDM demultiplexer. Er zijn 4 uitgangskanalen die 20nm gespatiëerd zijn in het golflengte domein en waarop telkens een detector geïntegreerd is. Deze component kan dienst



Figuur 3: Bovenaanzicht op een MSM detector array. De detectoren bevinden zich op 3μm brede silicium golfgeleiders. Het licht komt rechts binnen en de detectoren zijn 40μm lang. De pitch tussen de golfgeleiders is 25μm



Figuur 4: Bovenaanzicht van een CWDM ontvanger

doen als CWDM vermogen monitor of ontvanger. De detectoren zijn opnieuw gefabriceerd op een 25μm pitch and de totale oppervlakte van de demultiplexer, inclusief detectoren bedraagt slechts 0.1mm^2.

We hebben ook een geïntegreerde nabij-infrarode spectrometer vervaardigd. De spectrometer heeft dertig kanalen die elk 3.2nm gespatiëerd zijn in het golflengte domein. De oppervlakte van de spectrometer is $\sim$2mm^2.

English summary

1. Silicon photonic ICs

A major part of the cost of classical optical systems is the packaging. These optical systems consist of a combination of different subcomponents (lasers, filters, lenses, ...) that all need to be mounted and aligned inside the same package with very accurate, often sub-micrometer tolerances. This results in time consuming and expensive mechanical alignment processes. By making use of photonic integrated circuits (PICs), the cost can be strongly reduced as there are no individual subcomponents that need to be mounted and assembled. In this case, the light is routed between different integrated components by means of low loss optical waveguides. The definition of these components and their waveguide interconnections is done by means of collective, wafer scale lithography and etch processes.

Silicon is an excellent material for the fabrication of passive PICs such as optical filters. The silicon-on-insulator (SOI) material system possesses unique optical properties: the refractive index difference between silicon and silica is very large. This allows the creation of very compact and high density waveguide circuits including so-called photonic wires with typical bend radii as small as 1μm. Moreover, these waveguide structures can be fabricated on a 200mm SOI wafer scale using the same tools as the ones used for advanced electronic CMOS processing.

The goal of this work is to fabricate silicon PICs for spectroscopic applications. We mainly focus on WDM (Wavelength division multiplexing) receivers for optical communication and spectrometers for NIR (near-infrared) spectroscopy. For these applications, active/passive integration is needed: on-chip photodetectors need to be integrated onto passive silicon optical filters.

The thesis is divided into three main parts. In the first part, we discuss the design and characterization of these optical filters. The second part is about the technology and the design of integrated photodetectors. In a last part, we give an overview of fabricated SOI PICs with on-chip photodetec-

tors.

2. Optical filters fabricated in silicon

The heart of each spectrometer is the optical filter. This device needs to spatially separate different wavelengths from the input channel and needs to route these to different locations on the chip where the intensity can be measured by means of photodetectors. In this work, we fabricated for the first time so-called planar concave gratings (PCGs) on a nanophotonic SOI platform. To design these devices and to calculate their filter characteristics, we wrote simulation software based on scalar diffraction theory. Comparison between measurements and simulations showed that there was a good comparison between both and as a consequence, we had a powerful tool for designing nanophotonic PCGs. The simulation program is implemented in Matlab and is able to provide all the coordinates of the PCG layout which are needed to make the lithography masks for the fabrication.

We demonstrated very compact optical filters that operate around central wavelengths of 1.55μm with channel spacings ranging from 60nm for Fiber to the Home (FTTH) applications down to 1nm for fiber Bragg sensor interrogators. These sensors are used to measure stress in bridges and airplane wings among others. One of the main achievements was that we succeeded in reducing the on-chip loss down to 1.9dB for these components without the need for additional processing steps. We also demonstrated coarse WDM filters (CWDM), with high channel extinction ratios better than 30dB. However, we also noticed that high resolution PCGs are more sensitive to small fabrication imperfections as compared to devices used for coarse wavelength filtering. This causes excessive crosstalk. To solve this issue, we investigated the use of cascaded filters consisting of a combination of a PCG with ring resonators filters. This way, the PCG can be used for a coarse wavelength filtering of the input signal (e.g. 10×10nm spaced channels) and ring resonators filter a very narrow peak ($<$0.2nm) out of each channel.

3. Heterogeneous integration

Because silicon is optically transparent in the near-infrared (NIR) wavelength region at which optical telecommunication typically operates (1.31 and 1.55μm), other semiconductors need to be integrated to obtain efficient photodetection at these wavelengths. Commercial photodetectors for

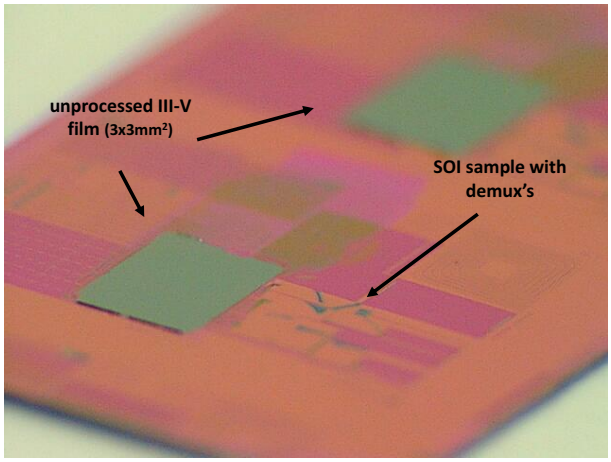


Figure 5: Two unprocessed InP-based epitaxial thin films ($3\times3\text{mm}^2$) bonded by means of BCB on an SOI substrate

telecom applications are fabricated in III-V semiconductors, typically InP/InGaAs. The heterogenous integration of InP/InGaAs on silicon can be carried out in different ways. Our integration approach is based on bonding of unprocessed III-V dies on the SOI waveguide wafer using an adhesive (benzocyclobutene, BCB) as an intermediate bonding layer. At the moment of bonding, the dies are not yet processed. Therefore, no strict alignment accuracy is needed and a fast pick-and-place procedure can be used. After bonding, the InP substrates are removed so that we obtain several unprocessed III-V films bonded onto the SOI waveguide wafer. This is shown in figure 5. After this, all photodetectors on the 200mm SOI wafer can be fabricated simultaneously. During these different fabrication processes (etching, metallization, ...), the alignment onto the underlying silicon waveguides is done by means of very accurate optical lithography.

In recent years, the Photonics research group has built a large expertise in the field of BCB die-to-wafer bonding. However, to be able to efficiently couple light between the silicon waveguides and the detectors on top, a very thin intermediate bonding layer is needed. During this research, we developed an integration process based on manual bonding of III-V dies on SOI using a sub-300nm intermediate BCB bonding layer. We demonstrated a high bonding yield and showed that multiple die-to-wafer bonding is possible. However, we also pointed out that an automated die-to-wafer bonding approach is needed in order to obtain a mature fabrication process that is suitable for commercial applications.

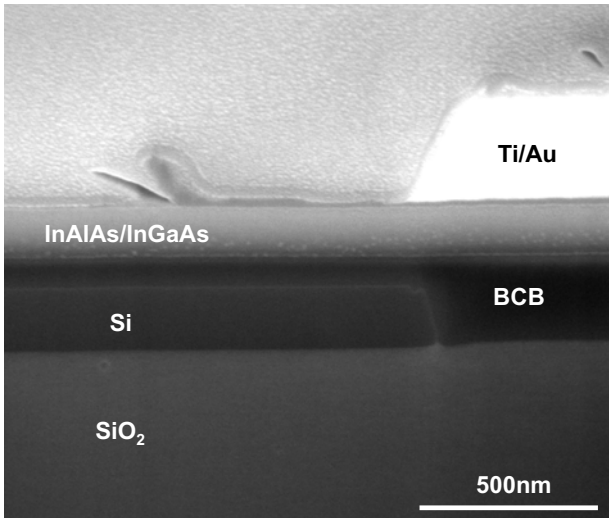


Figure 6: Cross section SEM picture of an InGaAs detector bonded on a silicon waveguide using a 100nm BCB bonding layer. Only the right half part is shown

4. InGaAs-on-SOI photodetectors

In this work, we designed and fabricated highly efficient InGaAs photodetectors coupled to SOI waveguides. We demonstrated very compact devices with a length of only 20μm, a responsivity of 1A/W at a wavelength of 1.55μm, which corresponds to a quantum efficiency of 80%, a dark current of 5nA and a linear power-current behavior over a 40dB range. By tuning the length of the detector and/or the bonding layer thickness, it is possible to tap off only a very small portion of the waveguide power for power monitor applications. We fabricated arrays of up to 100 detectors on a 25μm pitch without a single failure.

Simulation results showed that using standard contact lithography, electrical bandwidths up to 30GHz can be obtained. First high speed measurements on prototypes revealed optical bandwidths around 9.5GHz. Figure 6 is a cross section SEM picture of an InGaAs detector, bonded on SOI with a 100nm thick intermediate bonding layer.

The good performance of these detectors was the result of an intense process optimization. Initial devices that were fabricated suffered from different problems: a high dark current, asymmetric behavior and the presence of a large gain at low optical powers. These problems were solved by work-

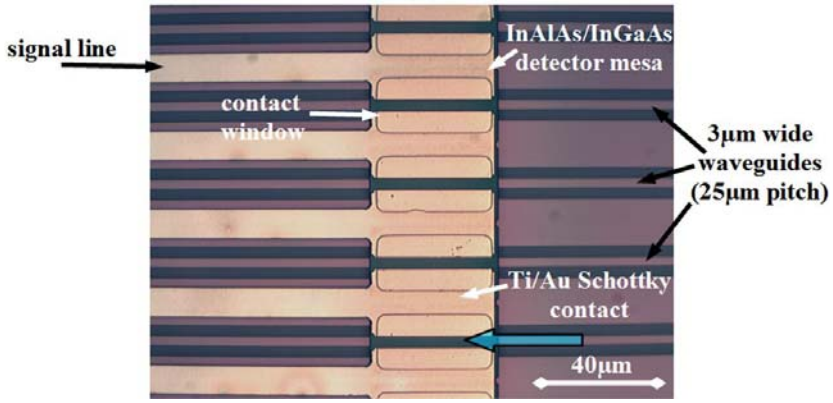


Figure 7: Top view on MSM detectors on top of 3μm wide SOI waveguides. Light enters from the right and the detectors are 40μm long. The waveguide pitch is 25μm

ing on the dry etch processes for the definition of the detector mesas and the opening of the contact windows. Figure 7 is a top view picture of an array of 40μm long MSM detectors, fabricated on top of SOI waveguides, on a 25μm pitch.

5. Active/passive PICs

In the last chapter, we demonstrated SOI PICs with integrated photodetectors for different applications: power monitors and WDM receivers for on-chip interconnects, CWDM and FTTH receivers for telecom applications and a 30-channel near-infrared spectrometer-on-a-chip. Figure 8 is a top-view picture of the fabricated CWDM demultiplexer consisting of a 4-channel PCG on SOI and heterogeneously integrated MSM detectors. This device can be used either as an integrated CWDM power monitor or receiver. The photodetectors are fabricated on a 25μm pitch and the total footprint of the demultiplexer, including photodetectors is only 0.1mm^2.

We also demonstrated an integrated near-IR spectrometer. For this device, we integrated an array of 30 photodetectors on a 30 channel PCG with 3.2nm channel spacing. The size of the spectrometer is $\sim$2mm^2.

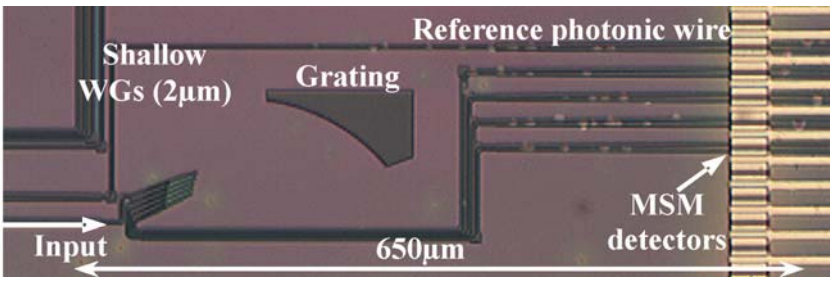


Figure 8: Top view picture of the CWDM receiver

1

Introduction

This chapter is an introduction to photonic integrated circuits (PICs). In a first part, we discuss two widespread applications of photonics: optical communication and sensing. In a second part, we briefly discuss the recent trend in photonics towards integrating different optical functionalities onto a single chip, called a PIC. PICs can be fabricated in many different material systems. In this work, we focus on the integration technology in silicon-on-insulator (SOI), called silicon photonics.

1.1 Photonics

Photonics is the branch of physics that deals with the properties, the technology and the applications of photons, which are the elementary units of light. Photonics covers all technical applications of light over the whole electromagnetic spectrum from ultraviolet over the visible to the near-, mid- and far-infrared. Most applications, however, are in the range of the visible and near-infrared.

Photonics and its applications are ubiquitous. Included are all areas, from everyday life to advanced science: optical fiber communication, data storage (CD, DVD, Blu-ray), remote controls, printers, bar code scanners, displays, lighting, image sensors, infrared cameras, solar cells, but also laser welding, laser surgery, gyroscopes, range finders, spectrometers, ...

1.1.1 Photonics for telecommunication

Photonics gained a lot of interest with the invention and the construction of the first functional laser in 1960 by T.H. Maiman [1]. Other developments followed, including the semiconductor laser diode in the 1970s, optical fibers for transmitting information and the Erbium-doped fiber amplifier. These inventions formed the basis for fiber-optic communications which revolutionized the telecommunications industry in the late 20th century and provided the infrastructure for the Internet.

Because of its advantages over electrical transmission in terms of bandwidth and attenuation, optical fibers have largely replaced copper wire communications in core networks and became the uncontested transport medium used in long distance communication. Most commonly used wavelength windows for optical telecommunication are situated around 1310nm (O-band), where the dispersion is zero, and 1550nm (C-band), where the attenuation is the lowest and the longest range can be achieved.

To efficiently use the large bandwidth of optical fibers, different signals on different wavelengths can be transported over the same fiber. This is called wavelength division multiplexing (WDM). A fiber optic telecommunication link, making use of WDM is shown in figure 1.1. A WDM system uses a multiplexer at the transmitter to join the signals of the different lasers on a single fiber. At the receiver side, a demultiplexer is used to split the different signals before they are converted into electrical signals by photodetectors. The spacings between the individual wavelengths transmitted through the same fiber serve as the basis for defining dense WDM (DWDM) and coarse WDM (CWDM).

DWDM is designed for long-haul transmission where different wave-

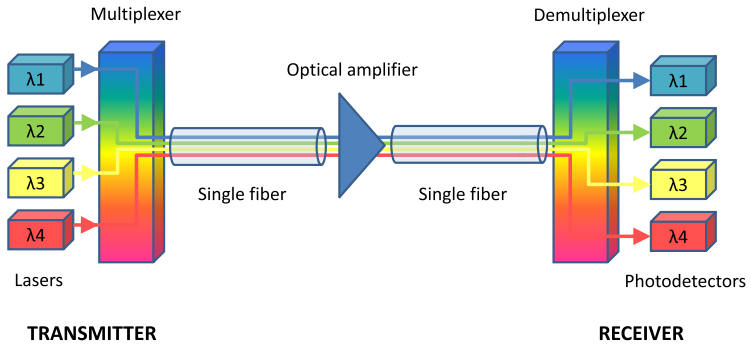


Figure 1.1: Wavelength division multiplexing (WDM) over an optical fiber

lengths are packed tightly together. It is typically used at a higher level in the communications hierarchy, for example the Internet backbone. Typical channel spacings around wavelengths of 1550nm are 1.6, 0.8 and 0.4nm. Equipment makers have found various techniques for sending 32, 64, or even 128 wavelengths over a single fiber. However, this technology is expensive as high precision filters and temperature controlled lasers are required. Coarse wavelength division multiplexing (CWDM) systems on the other hand have a channel spacing of typically 20nm on the ITU (International Telecommunication Union) wavelength grid (figure 1.2) and are designed for use with uncooled transmitter lasers. CWDM makes it possible to increase the capacity of a fiber optic link without installing expensive dense WDM (DWDM) systems. It is typically used for shorter distance communication links where a lower aggregate bandwidth is needed. Figure 1.2 shows the typical ITU wavelength grid for both CWDM and DWDM.

Fiber optic communication can also be used for data transport over much shorter distances. Fiber to the home (FTTH) is a good example of this evolution in which there is a fiber connecting each household to a central office a few miles away. At the subscriber side, a transceiver, which is a combination of a transmitter and a receiver, is needed to generate upstream signals and to receive downstream signals coming from the central office. Recently, chip maker Intel launched its Light Peak technology. This is a high-speed optical cable technology designed to connect electronic devices to each other, such as displays, disk drives, PCs, handheld devices and other consumer electronic devices. For these short distance applications, the volumes are much larger as compared to volumes for long-haul fiber-optic equipment and as a consequence, cost is a very important issue.

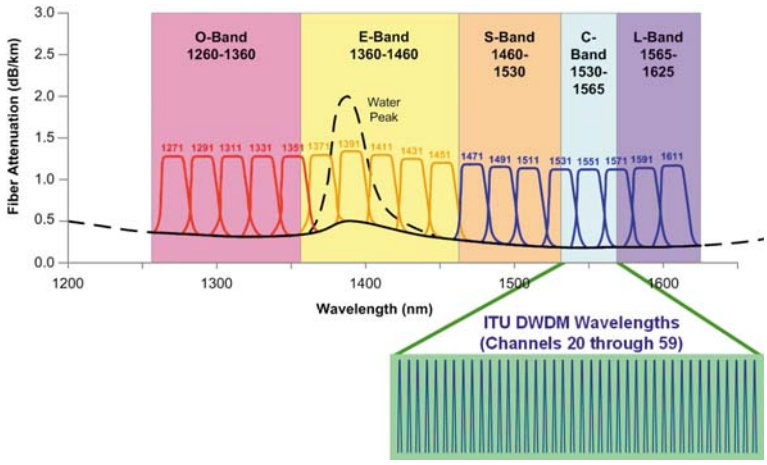


Figure 1.2: Representation of the ITU wavelength grid for CWDM and DWDM

1.1.2 Photonics for sensing

Another widespread application of photonics is sensing. Absorption of light by a unknown sample is one of the oldest and still one of the more useful methods for determining its composition. The wavelength of light that this sample will absorb is characteristic of its chemical structure. Specific regions of the electromagnetic spectrum are absorbed by exciting specific types of molecular and atomic motion to higher energy levels. Absorption of microwave radiation is generally due to excitation of molecular rotational motion. Infrared absorption is associated with vibrational motions of molecules. Absorption of visible and ultraviolet radiation is associated with excitation of electrons, in both atoms and molecules, to higher energy states. Figure 1.3 shows a typical absorption spectroscopy setup. A visible light source in this example illuminates an unknown sample. Depending on the composition, certain wavelengths will be strongly absorbed, others not. Then, a dispersive element, also called a wavelength filter (e.g. a prism, a diffraction grating) in combination with the entrance slit spatially separates the different wavelengths and a photodetector array measures the intensity of each wavelength. This allows to determine the composition of an unknown sample.

Near-infrared spectroscopy operates in a wavelength band from 800nm to 2.5μm. This wavelength range is often used for sensing blend levels between biodiesel and diesel, glucose concentration in blood, food quality control, ...

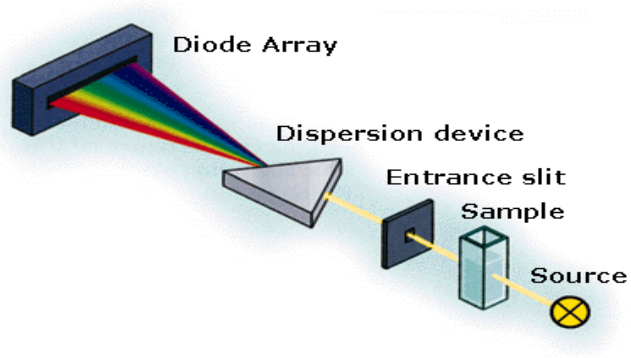


Figure 1.3: Basic components of an absorption spectroscopy setup

1.2 Photonic integrated circuits

Without a doubt, one of the greatest technological innovations of the 20th century has been the development of the electronic integrated circuit (IC). The impact of ICs arises from the ability to monolithically integrate ever more transistors and other electronic devices into a single piece of silicon. This is dictated by the famous Moore's Law. This law, named after Intel co-founder Gordon E. Moore, predicts a doubling of the number of transistors on integrated circuits every 2 years. Besides the increase of transistor count, there is an exponential improvement of other measures of digital technology: greater processing power, lower cost per device, improved reliability and reduced power requirements. This enabled countless new devices for a wide range of applications. Moore's law was first stated in 1965 and since then, it has largely held the test of time. Recent Intel microprocessors contain more than 2 billion transistors on a single silicon die.

Back in the 1950s, electronic systems were nothing but a loose combination of resistors, capacitors, and transistors. Unfortunately, this is the same stage, where most optical systems are now. Very large discrete optical components, both active (lasers, modulators, detectors, ...) and passive (multiplexers, diffraction gratings, lenses, thin film filters, optical fibers, ...) are simply put together, aligned and assembled in a package. In analogy with electronics, there is a trend in photonics towards integrating different components with different functionality onto a single chip, called a photonic integrated circuit (PIC). Just like in electronics, a PIC provides cost, space, power and reliability advantages compared to the use of a combination of discrete single-function devices.

A major part of the cost of classical optical systems is the packaging. Different components must be interconnected and aligned to each other inside the package (lasers, filters, lenses, ...) with often sub-micrometer tolerances. This requires very accurate and therefore time consuming and expensive mechanical alignment. Moreover, these different materials may have differences in optical, mechanical and thermal characteristics. This could pose reliability issues and makes the package more challenging and expensive, also due to the requirement of thermo-electric coolers. By making use of PICs, the cost can be strongly reduced as there are no individual subcomponents that need to be mounted and assembled. In this case, the light is routed between different integrated components by means of low loss optical waveguides. The definition of these subcomponents and their waveguide interconnections is done by means of collective, wafer scale lithography and etch processes. Also, by making use of PICs, the number of fiber couplings, which are often a point of failure, is strongly reduced.

1.2.1 Integrated optical transceivers and spectrometers

It wasn't until 2004 that PICs based around active elements such as lasers and detectors found commercial success. In this year, US vendor Infinera launched indium phosphide (InP)-based photonic circuits for long-haul DWDM systems [2]. In 2009, they demonstrated a 400 Gigabit per second (Gbps) transmitter PIC containing more than 300 optical functions on a single chip. This device integrates ten lasers to deliver ten optical channels, each one operating at 40Gb/s. This PIC offers advantages both in power savings and cost as compared to discrete optical component solutions: it consumes 80% less power per Gb/s and the number of packages is reduced from $\sim$70 to only 1.

This is a good example of the advantages of photonic integration. However, the monolithic integration of active and passive devices in InP/InGaAsP compound semiconductors as in the example mentioned above is a relative expensive integration technology and is typically used for long haul telecommunication. For optical communication applications that are closer to the customer end like CWDM and FTTH, cost is a critical issue and that's where silicon photonics is emerging as integration technology.

In the other field of application as mentioned in this chapter, sensing, there is also a need for integrated, cheap and rugged devices. Conventional photospectrometers in the labs used for sensing are typically large and expensive and have a performance that often exceeds the requirements for typical industrial applications. For industrial applications, what counts are the cost, size, robustness, sample volume, measurement time, ... of the

spectrometer [3]. For these applications, integrated spectrometers that can be mass fabricated are better suited and using these devices, a new range of applications such as real-time, mobile sensing becomes possible.

Integrated spectrometers do not have any moving parts, there is no air in the optical path and subcomponents (grating, slits, detectors) can be manufactured and aligned to each other by making use of very accurate lithographical techniques. These factors increase the reliability of the spectrometer and make it more rugged as there are no discrete components that could possibly shift over time.

1.2.2 Silicon photonics

Photonic integrated circuits can be fabricated in a many different material systems: silica-on-silicon, III-V semiconductors like InP/InGaAsP and GaAs/AlGaAs, silicon-on-insulator, polymers, ... Each material system has its advantages and disadvantages. Silica-on-silicon is a waveguide platform that allows to fabricate very low loss optical filters, but due to the low refractive index contrast, the devices are large and the integration density is limited. III-V semiconductors on the other hand allow to monolithically integrate active (e.g. sources, detectors) and passive components (e.g. waveguides) but it is a relatively expensive technology with a limited possible integration density. In this work, we focus on silicon photonics. This technology makes use of silicon-on-insulator wafers for the fabrication of PICs. Silicon-on-insulator offers some important advantages as compared to other material systems. Due to the high refractive index contrast, very compact and high density waveguide circuits can be fabricated. Moreover, high yield and low cost manufacturing can be realized by making use of advanced CMOS tools that are used for the fabrication of electronic integrated circuits [4].

1.3 Goal of this work

The goal of this work is to fabricate silicon PICs for spectroscopic applications. We mainly focus on WDM receivers for optical communication and spectrometers for near-infrared spectroscopy. For these applications, high sensitive, compact and reliable near-infrared on-chip detectors are needed. We will tackle integration technology, coupling schemes and detector design and fabrication.

The heart of spectrometers for WDM and sensing applications is the wavelength filter. Our goal is to fabricate compact wavelength filters with a

low insertion loss and a high channel extinction ratio. For optical communication application, we focus on coarse wavelength filtering. For sensing applications on the other hand, our main goal is to obtain very compact sensors which offer a high resolution over a broad wavelength range.

1.4 Thesis outline

This work is built around three main parts. A first part discusses silicon photonics for the fabrication of wavelength selective devices. This is the subject of chapter 2 and 3. Chapter 2 is a general introduction to silicon photonics in which we explain the concept of photonic wires and we give a short overview of recent progress in this field. In chapter 3, we discuss optical filters based on waveguide echelle gratings. We focus on the design and the fabrication and give an overview of experimental results. We also discuss some practical spectroscopic applications: WDM for optical communication and spectrometers for sensing and fiber Bragg interrogators. A second part of this work, chapter 4 and 5 is about the technology and the design of integrated near-infrared photodetectors. In chapter 4, we discuss different materials, technologies and coupling schemes that are suitable for the integration near-infrared photodetectors on silicon photonic wires. It serves as an introduction to chapter 5 in which we discuss the design, fabrication and characterization of a compact and efficient integrated InGaAs-on-Si photodetector. Chapter 6 concludes this work with experimental results of active/passive silicon PICs. We demonstrate a power monitor, resonant photodetectors, a prototype CWDM receiver and a packaged miniature near-infrared spectrometer.

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Silicon photonics

This chapter is an introduction to silicon photonics. We briefly discuss the silicon-on-insulator (SOI) material system and give a short overview of recent progress in this field. We elaborate on the CMOS compatible fabrication technology of SOI photonic integrated circuits (PICs) and discuss the concept of photonic wires. Next, we present structures that allow for easy characterization of these PICs and before going into more detail in the next chapter, we give an introduction to wavelength selective devices based on photonic wires.

2.1 Introduction

Since the introduction of silicon photonics by R.A. Soref in the mid to late 1980s [1], impressive progress has been achieved in this field with the demonstration of both passive and active building blocks which allow to couple [2], guide [3], filter [4], generate [5, 6], modulate [7] and detect [8, 9] optical signals. The ever growing interest in silicon photonics is fueled by several factors [10, 11]. The silicon-on-insulator (SOI) material system possesses unique optical properties: silicon and silica are transparent for wavelengths typically used for optical communications (1.31-1.55μm) and the refractive index difference between both materials is very large. This allows the creation of very compact and high density waveguide circuits including so-called photonic wires with bend radii as small as 1μm. Moreover, these waveguide structures can be fabricated on a wafer scale using existing CMOS (complementary metal oxide semiconductor) processing infrastructure. CMOS is the dominant technology for the fabrication of digital electronic integrated circuits.

Thanks to the compactness, the ability to obtain very close spacing of the waveguides and the wafer scale processing, dense integration of multiple optical functions on the same chip becomes possible. This is expected to bring the same advantages that propelled the success of CMOS electronics: increase of performance and reliability, the possibility of creating compact components with complex functionality and a spectacular decrease of the cost per function by making use of high yield, wafer scale processes.

2.2 Silicon-on-insulator

2.2.1 SOI wafers

A silicon-on-insulator (SOI) wafer consists of a thin silicon waveguide layer on top of a buried oxide (SiO_2) layer on a silicon substrate. The top silicon layer (n=3.47) is the waveguide core and the oxide layer is the bottom cladding (n=1.44) layer. The silicon substrate itself has no optical functionality and acts as a mechanical support. SOI wafers are available up to diameters of 300mm at the moment (and even 450mm in the near future). We use 200mm mono-crystalline SOI wafers from SOITEC which are fabricated by means of a combination of direct wafer bonding, layer splitting and chemical mechanical polishing (CMP) (figure 2.1).

SOI wafers are not only used for photonic applications. They are also widely used in the microelectronics industry and are compatible with the existing CMOS fabrication tools and processes.

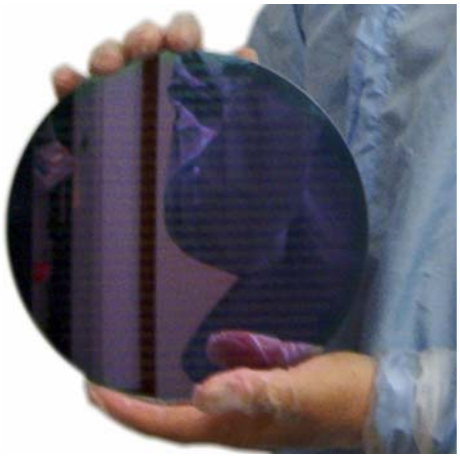


Figure 2.1: 200mm SOI wafer

2.2.2 Photonic wires in SOI

The SOI material layer stack used throughout this work has a 220nm thick silicon waveguide layer and a 2μm buried oxide layer. This oxide bottom cladding layer is sufficiently thick to prevent leakage of light to the substrate. The top cladding can be air, a protective oxide layer or even a polymer (e.g. BCB in case adhesive wafer bonding is used for integrating III-V semiconductors). The thickness of the silicon waveguide layer is kept below 270nm in order to support one guided transverse-electric (TE) and one guided transverse-magnetic (TM) slab waveguide mode for light with a wavelength around 1.55μm.

By etching completely through the 220nm thick silicon waveguide layer, a very high refractive index contrast is obtained, both horizontally and vertically (n_{air}=1, n_{oxide}=1.44 and $n_{silicon}$=3.47). This allows to fabricate photonic wire waveguides. Photonic wires are conventional waveguides that have a submicron core and high refractive index contrast. With a core thickness of 220nm, single-mode (one TE-like mode and one TM-like mode) SOI waveguides without oxide top cladding should be narrower than 580nm for 1.55μm wavelengths [13]. Typical dimensions of these photonic wires are 220nm $\times$ 500nm with a propagation loss of 2.4-2.7dB/cm [14, 15] (figure 2.3(a)). The high index contrast gives rise to very strong confinement, which makes it possible to make very sharp bends without radiation losses in the bend. The typical excess loss of a 90 degree bend with 5μm bend radius is only 0.004dB, while bends with a 1μm bend radius have a loss of only 0.09dB [16]. The strong confinement makes it also possible to fabri-

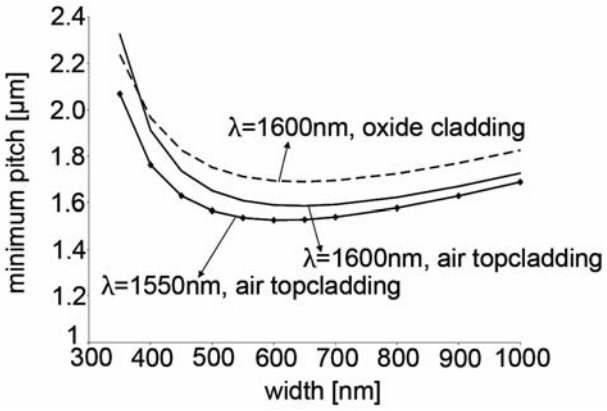


Figure 2.2: Simulated minimum pitch needed for less than -20dB/cm coupling between parallel wires. Courtesy of P. Dumon [12]

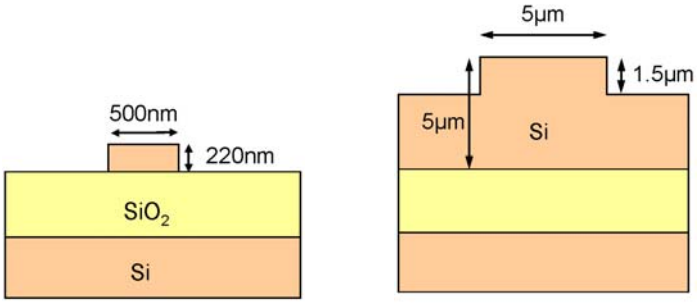
cate these photonic wires on a very small pitch. Figure 2.2 shows that a gap of 1μm is sufficient to decouple 700nm wide wires.

The enormous integration density of these photonic wire waveguides makes it possible to integrate a lot of functionality onto a single chip. However, the small waveguide size also creates some problems. Due to the large mode mismatch between a single mode fiber and a photonic wire, the fiber-to-waveguide coupling is challenging and dedicated couplers such as spot-size converters or waveguide gratings are needed. The photonic wires are also very polarization dependent and sensitive to any dimensional variation. Therefore, a high resolution fabrication process is needed to be able to control dimensions in the range of 1-5nm [14].

2.2.3 Large-core SOI

The material system as discussed earlier is often referred to as a nanophotonic SOI platform because it allows to fabricate waveguides with a width of a few hundred nanometers. Another type of SOI that is often used is the large-core SOI material system. The thickness of the silicon waveguide layer of these large-core SOI wafers is typically several micrometer [17]. Although these thick slab waveguides also support higher order modes, it is possible to fabricate single mode rib waveguides by careful adjusting the etch depth and the waveguide width [18, 19]. This requires shallow etching of the waveguides in order to reduce the lateral refractive index contrast. A typical configuration of these rib waveguides is shown in figure 2.3(b).

As the reduced index contrast severely increases the necessary bend



(a) Nanophotonic waveguide (photonic wire)

(b) Large-core rib waveguide [17]

Figure 2.3: SOI waveguide technology (drawing not on scale!)

radius and waveguide pitch in this material system, the integration density is limited. Also, we will show later that the thick slab waveguide has some important drawbacks for the fabrication of echelle grating demultiplexers. Large-core SOI also offers some important advantages: low waveguide propagation loss, low coupling loss to fiber and low polarization dependence.

2.2.4 CMOS compatibility

One of the major advantages of using SOI as a platform for the fabrication of silicon photonic integrated circuits (PIC's) is the compatibility with CMOS processing. By making use of industrial CMOS fabrication tools, we can take advantage of not only the enormous processing infrastructure but also the knowledge base and process maturity of these fabrication processes. In this work, we made use of the advanced CMOS research environment of IMEC in Belgium.

2.3 Waveguide patterning

2.3.1 Waveguide layouts

Our basic SOI waveguides are etched in a two level process. For the fabrication of photonic wires and other standard waveguide structures, the 220nm silicon layer is completely etched through. For other structures such as fiber couplers (paragraph 2.4) and shallow waveguides (chapter 3), we only etch 70nm deep into the Si waveguide layer. The alignment accuracy

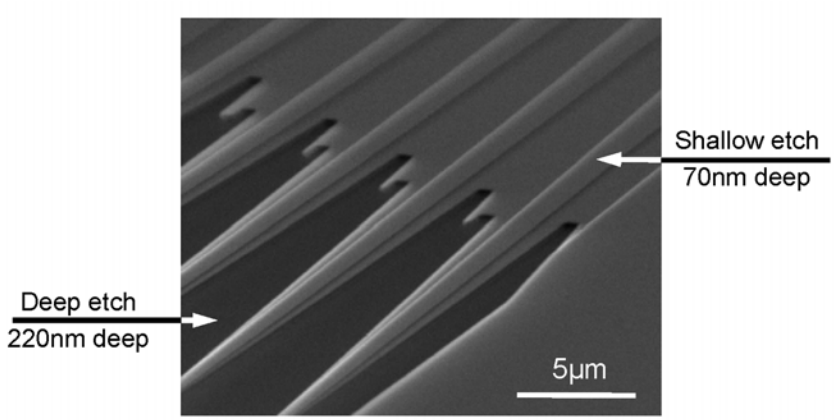


Figure 2.4: SEM picture of a waveguide taper using a combination of deep and shallow etching

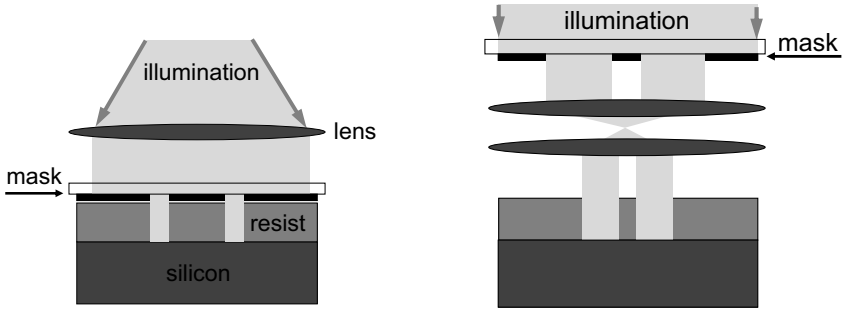
between these two lithography steps is better than 50nm. Figure 2.4 is an SEM picture of a double taper structure that is fabricated using a combination of deep and shallow etching. This taper is an adiabatic transition from a deeply etched photonic wire to a shallowly etched waveguide.

2.3.2 Fabrication technology

2.3.2.1 Optical lithography

The SOI waveguide wafers are processed using deep-UV (DUV) lithography in combination with dry etching. Deep-UV lithography is an optical projection lithography technique with an illumination wavelength in the deep ultraviolet range. The advantage of optical lithography in comparison with other fabrication techniques such as e-beam lithography are its high throughput and mass production capabilities.

Optical lithography makes use of light to transfer a pattern that is present on a mask in a photosensitive layer, called photoresist. The mask is a glass plate with a patterned chrome layer on top. Two types of lithography can be used: contact lithography and projection lithography. Both methods are show in figure 2.5. In contact lithography, which we use for our III-V fabrication processes in the INTEC cleanrooms, the mask is brought in close contact with the photoresist coated wafer. Contact lithography is mainly used for research purposes. For mass fabrication, projection lithography is used. In this case, the mask does not make contact with the photoresist but the pattern on the mask is projected onto the wafer using a lens



(a) Contact lithography (b) Projection lithography

Figure 2.5: Optical lithography

system. The patterns on the mask are typically magnified four or five times and the lens system reduces the pattern to its original size.

The resolution of optical lithography systems depends on several factors but the main limiting factor is the illumination wavelength. The contact lithography setup in the INTEC cleanrooms has an UV light source with a wavelength limited to $\sim$320nm. The minimum linewidth that can be patterned is 0.5-1μm. This is sufficient for the fabrication of our III-V photonic components, but not sufficient for the patterning of SOI photonic wires.

2.3.2.2 Deep-UV lithography

In this work, the first SOI wafers were patterned using deep-UV lithography at wavelength of 248nm. The use of 248nm DUV lithography for fabricating nanophotonic integrated circuits was explored to great extent by Bogaerts et al. [15]. This work demonstrated the feasibility of using CMOS fabrication tools for the fabrication of photonic integrated circuits and structures with a period down to 400nm. By switching to 193nm DUV in a later stadium of this work, there was a substantial improvement in terms of achievable uniformity and resolution. This technology was introduced in the photonics research group of INTEC/IMEC by S.K. Selvaraja et al. and is clearly described in [14].

Figure 2.6 gives an overview of the 193nm process flow [14]. An ASML step-and-scan system is connected to an automated track for preprocessing (coating and baking) and postprocessing (baking and developing). The light source is an ArF laser. The processing starts with cleaning the 200mm SOI wafers followed by spinning and baking an anti-reflection coating. This coating reduces the reflections from the SOI wafer which

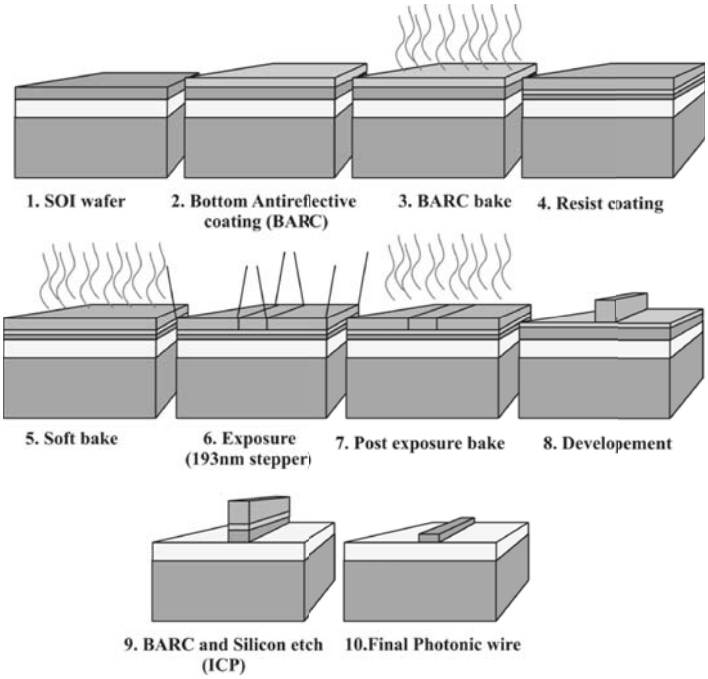


Figure 2.6: Fabrication process overview of SOI photonic IC's using 193nm deep-UV lithography. Picture courtesy of S.K. Selvaraja [14]

causes an unwanted resist profile. Then, a layer (330nm) of photoresist is spun and the wafer is baked again to remove the solvents from the applied layers. After this, the wafer is sent to the stepper, which illuminates the wafer with the pattern on the mask. The pattern, which determines the size of a single die (12mm $\times$ 12mm for example) is repeated several times over the 200mm wafer. This allows to vary the exposure conditions (exposure dose and focus) while stepping across the different dies to find the optimum conditions. After exposure, the wafers are baked again and developed to remove the exposed part of the photoresist in a developer solution. The photoresist is then used as a mask for etching the silicon waveguide layer.

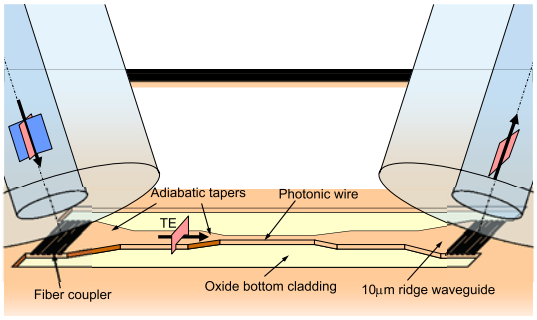
2.3.2.3 Etch process

Following lithography, the pattern defined in the photoresist is transferred into the underlying Si layer by means of inductively coupled plasma-reactive ion etching (ICP-RIE) in combination with a Cl_2/HBr/CF_4/O_2 gas mixture. The etch recipe consists of a four steps with a different chemistry. For more details, we refer to [14].

2.4 Characterization

In order to characterize SOI waveguide devices, we couple light from a standard single mode fiber, which is positioned at a 10° angle from vertical into a 10μm wide ridge waveguide and vice versa using fiber couplers as can be seen in figure 2.7(a). These broad waveguides are then tapered down to photonic wires using adiabatic tapers. The fiber couplers are one-dimensional first order gratings, which are shallowly etched (70nm deep). For coupling of light with a wavelength of 1.55μm, the grating period is typically 630nm with a 50% fill factor. The theoretical coupling efficiency of these fiber couplers is 35% at a wavelength of 1.55μm. The measured efficiency is around 30%, which corresponds with a coupling loss of 5dB. The 1dB bandwidth is approximately 40nm as can be seen in figure 2.8 [20]. Figure 2.7(b) is a photograph of an SOI sample on the measurement setup. Translation stages are used to accurately position the fibers on top of the couplers. By making use of so-called raised gratings, coupling efficiencies up to -1.6dB have been demonstrated recently [21].

It is important to notice that the one-dimensional gratings as described here only couple one linear fiber polarization into the waveguide TE polarized mode. In chapter 3, we will discuss two-dimensional fiber couplers which couple both orthogonal fiber polarizations into the SOI chip. For characterizing SOI devices, we typically connect one fiber to a light source



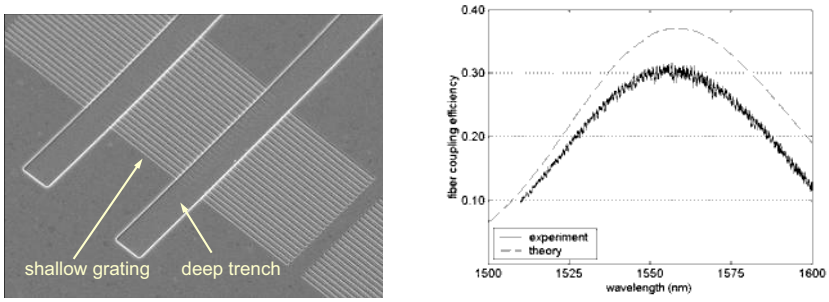
(a)

(b)

Figure 2.7: Schematic layout and picture of the SOI measurement setup using fiber couplers for interfacing with single mode optical fibers

(typically a tunable laser or a broadband superluminescent LED) and one fiber to a power meter or spectrum analyzer. As the standard 1-D fiber couplers only couple one fiber polarization into the SOI chip, we make use of polarization wheels to control the polarization and to couple TE-polarized light into the waveguides.

When measuring passive devices (such as wavelength demultiplexers), we normalize the measured transmission spectrum to the transmission spectrum of a reference photonic wire. This reference waveguide is a straight 500nm wide photonic wire, which is coupled to an input and output fiber coupler. This allows us to calculate the on-chip transmission by filtering out the spectrum of the light source and the transmission of the fiber couplers.



(a) SEM picture (b) Coupling efficiency

Figure 2.8: Fiber coupler efficiency [20]

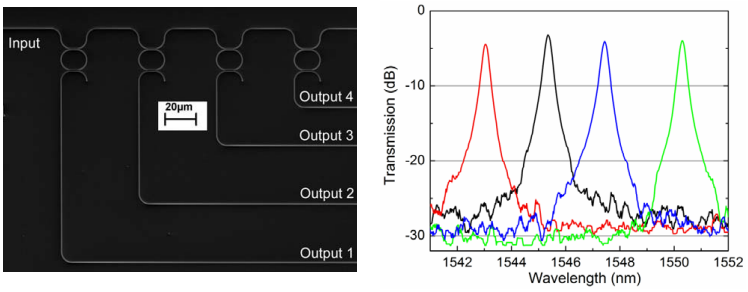
2.5 Wavelength selective devices in SOI

We briefly discussed waveguide devices based on SOI photonic wires to guide and route light on the PIC but also to couple light from an optical fiber into the chip and vice versa. Also wavelength filtering is another important passive functionality. Before going into detail in chapter 3, we introduce these devices and explain the operation of multi-channel wavelength filters such as arrayed waveguide gratings and echelle gratings.

2.5.1 Introduction

The operation principle of many integrated wavelength filters is based on the interference of different light paths which experience a wavelength selective phase delay with respect to each other. In the case of a Mach-Zehnder interferometer (MZI), two light paths interfere. In the case of a ring resonator (RR), the light path interferes with itself and in a diffraction grating, multiple light paths interfere. A different type of filters are devices that rely on the interference of different waveguide modes in a single structure instead of interference of different light paths. Examples of these filters are directional couplers (DCs) [22] and multimode interference filters (MMIs).

The large refractive index contrast of the nanophotonic SOI platform used in this work allows to significantly reduce the footprint of wavelength filters as compared to similar components fabricated in other material systems like glass (silica) or InP/InGaAsP. By making use of photonic wire waveguides with a bend radius of a few micrometer, many of these devices can be integrated on a certain chip area. However, there are also some



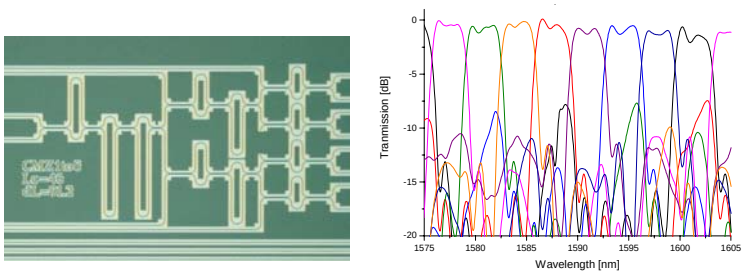
(a) SEM picture (b) Frequency response

Figure 2.9: WDM based on cascaded ring resonators. Taken from [23]

drawbacks. The high index contrast, sub-micrometer size waveguides are very sensitive to phase noise caused by small dimensional variations on a nanometer scale. This means that on one hand, advanced fabrication technology should be used and on the other hand, the devices have to be designed in a clever way to make them tolerant to fabrication imperfections and fabrication variations within a die, wafer or batch of wafers. This will be discussed in detail in chapter 3.

Ring resonators and MZIs can be used to drop or to add a single wavelength channel from or to a broader wavelength spectrum. The resonant behavior of RRs results in a very sharp channel selection. In the case of a MZI, only two light paths interfere and this results in a periodic sinusoidal wavelength response [4]. By cascading these filters [23–25], one could make in principle multi-channel filters. In [23], four rings with a slightly different circumference were connected to the same input waveguide to make a 1×4 (de)multiplexer as shown in figure 2.9. This filter is very compact but the main issues associated with this type of device is the limited operational wavelength range and the fact that the channel spacing is very sensitive to waveguide width variations and as a result, difficult to control.

Figure 2.10(a) is a micrograph of a 1×8 cascaded MZI demultiplexer [24]. It consists of a binary tree of single 1×2 MZIs where each output is connected to another MZI. The first filter is a multi-stage MZI with three delay sections for dense flat-top filtering. The second level filters are double stage MZIs and the third level filters are classical MZIs for coarse wavelength filtering. This results in a 8-channel transmission spectrum with flat-top shaped wavelength channels as show in figure 2.10(b). However, the extinction ratio of the suppressed channels is worse than 10dB making



(a) Micrograph (b) Frequency response

Figure 2.10: WDM based on cascaded Mach-Zehnder interferometers. Taken from [24]

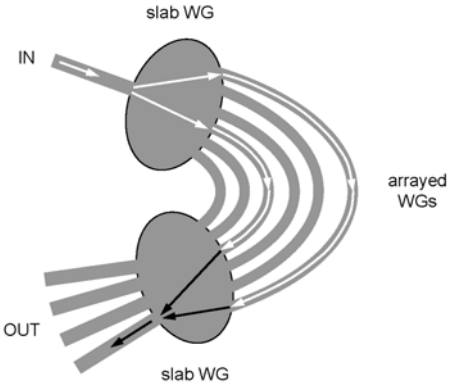
this particular device unsuitable for practical telecom applications. This is most probably caused by small width variations of the delay lines which causes phase errors.

These two examples demonstrate that multi-channel SOI wavelength filters can be fabricated by cascading simple 1×2 demultiplexers such as RRs or MZIs. However, more elegant solutions exist which possibly offer a higher flexibility and performance and which are based on a single component: arrayed waveguide gratings (AWGs) and planar concave gratings (PCGs). These devices are often called planar spectrographs and can act as multi-channel filters in WDM optical communication networks. With increasing resolution and channel counts, these filters could also find applications in the domain of sensing and spectroscopy. In chapter 6, both cases will be studied.

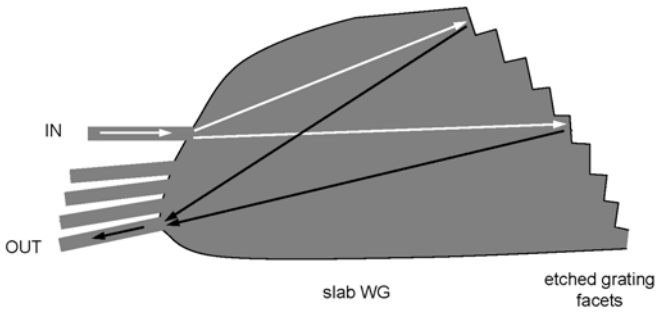
2.5.2 Planar spectrographs

The functioning of planar spectrographs like AWGs and PCGs (and diffraction gratings in general) is based on the interference of multiple light paths. These devices split up the light into different contributions. Each contribution propagates along a light path with a constant length increment ΔL. Depending on the wavelength, these contributions will constructively or destructively interfere in a certain direction, producing an interference maximum or minimum respectively. The wavelength at which constructive interference will occur is given by

$$\lambda = \frac{n_{\text{eff}}\Delta L}{m} \tag{2.1}$$



(a) Arrayed Waveguide Grating



(b) Planar Concave Grating

Figure 2.11: Schematic top view of an AWG and a PCG

where n_{eff} is the effective index, λ is the wavelength and ΔL the delay length. The integer number m is called the order of diffraction.

Both AWGs and PCGs make use of a combination of a slab waveguide which serves as a (de-)focusing medium and a section which introduces a phase delay between different contributions. This section consists of arrayed waveguides in the case of an AWG and a concave grating which is etched in the slab waveguide in the case of a PCG. A schematic drawing of both devices are shown in figure 2.11(a) and 2.11(b).

An AWG consist of two slab waveguides, also called star couplers which are connected with arrayed waveguides. Typically, the arrayed waveguides have a constant length increment, ΔL between them. The light from the input waveguide is spread out over the different arrayed waveguides by means of the input star coupler. In the output star coupler, the different light

paths come together and depending of the wavelength, the light will be focused on one of the output waveguides. A PCG on the other hand consists of a slab waveguide in which a grating is etched on one side and waveguides which are connected on the other side. The functioning of a PCG is similar to that of an AWG: the input waveguide is connected with the slab waveguide and the input light propagates until the grating is reached. The concave grating then both diffracts and refocuses the light, depending on its wavelength onto one of the output waveguides.

Due to the similarity between both devices, general grating theory can be used to describe both these devices [26]. As a result, the characteristics and formulas describing the wavelength filtering such as order of diffraction, dispersion and free spectral range of AWGs [12] and PCGs [15] are similar. However, there are some important differences, which have an influence on device performance. First, in a PCG, the delay medium and the focusing medium are the same: the slab waveguide. In an AWG, this is not the case and this results in more design freedom. Secondly, an AWG is a transmissive device while a PCG is a reflective device. This means that the insertion loss of a PCG depends on the grating reflectivity and it is typically larger for PCGs as compared to AWGs. Third, in an AWG, the waveguide arms replace the slab section and grating facets of a PCG. As a consequence, in an AWG, the phase delay of the different contributions not only depends on the waveguide core thickness but also on the exact waveguide width. This additional source of phase noise, which is not present in PCGs can degrade the performance, especially in high index contrast material systems.

2.5.2.1 Arrayed waveguide gratings

After their invention in the late 1980s, AWGs have become increasingly popular, especially for wavelength filtering in WDM (wavelength division multiplexed) optical communication systems in the 1.5-1.6μm wavelength range [27]. Commercially available AWGs have been mostly fabricated in low index contrast silica-on-silicon waveguides [28]. These devices have a low insertion loss in the order of a few decibels, a high channel isolation and low polarization dependency. AWGs in other low to moderate index contrast material systems such as InP/InGaAsP [29] and large-core SOI platforms [30, 31] have also been reported.

Recently, these devices have also been fabricated in SOI photonic wire technology [32–34]. These first devices showed that translating the AWG technology directly from a low index contrast silica material system to a nanophotonic SOI platform is challenging, mainly due to polarization de-

pendency and significant crosstalk arising from phase errors. The submicrometer size waveguides are very sensitive to small waveguide width variations that can give rise to significant phase errors, thereby degrading the performance. Due to advances in processing technology (using 193nm DUV lithography for example) but also due to clever design to decrease the phase noise [35] and the polarization dependency [36], significant improvement has been made in recent years. In 2010, our group reported a very compact 8×3.2nm SOI AWG with an on-chip loss of 2dB and -25dB crosstalk [35].

2.5.2.2 Planar concave gratings

PCGs have been reported in many material systems such as silica-on-silicon [37–39], InP/InGaAsP [40–44] and large-core SOI [45–49]. In literature, different names are used for integrated grating based demultiplexers: integrated echelle gratings, etched diffraction gratings or planar concave gratings (PCGs).

As mentioned before, PCGs are reflective devices and this has some serious consequences. Whereas AWGs in most material systems consist of shallowly etched waveguides, PCGs require deeply etched grating facets. Moreover, their performance critically depends on grating profile imperfections and particularly the verticality of these deeply etched grating facets is a critical issue. Early PCGs mainly suffered from large insertion loss and polarization sensitivity. These problems hindered commercial applications in favor of AWGs, which became the dominant (de)multiplexing technology due to their more tolerant fabrication technology.

In 2007, we successfully demonstrated for the first time a PCG fabricated on a nanophotonic SOI platform [50]. This was a 4×20nm PCG. Although the insertion loss of this device was relatively high, we obtained a very low crosstalk ($<$ -30dB). This was better or at least comparable to PCGs fabricated in lower contrast material systems. In 2008, we demonstrated that the insertion loss can be reduced down to 1.9dB without the need for additional processing steps [51].

Since this first demonstration of a nanophotonic SOI PCG, there has been a growing interest. Recently reported results include devices with smaller channel spacing down to 3.2nm [52, 53], the heterogeneous integration with InGaAs photodetectors [53, 54], Fiber-to-the-Home (FTTH) demultiplexers [55], devices fabricated in amorphous silicon (a-Si) [56] and high resolution filters consisting of a PCG cascaded with (tunable) ring resonators [57, 58].

In chapter 3 the design, simulation and characterization of nanopho-

tonic SOI PCGs will be discussed in detail. We will show that a major advantage of this high index contrast material system is the relaxed fabrication tolerance of the grating verticality. Also, as mentioned above, the main sources of phase errors in nanophotonic SOI AWGs, being the small waveguide width variations, are not present in PCGs. This has some serious consequences. Whereas AWG demultiplexers tended to outperform PCGs in low index contrast material systems, this is not longer the case for devices fabricated in the nanophotonic SOI material system as presented in this work. Especially for coarse WDM filters and devices with a large channel count (e.g. spectroscopy applications), they can possibly outperform AWGs.

2.6 Conclusions

This chapter was a brief introduction to silicon photonics. We explained the difference between the nanophotonic and the large-core SOI material system. Only the nanophotonic SOI platform makes a very high integration density possible by making use of photonic wire waveguides. We discussed the fabrication technology and the characterization method for these PICs. We also gave a brief intro to multichannel wavelength filters such as cascaded MZIs and RRs, AWGs and PCGs and we pointed out that filters based on photonic wire waveguides are very sensitive to small dimensional variations imposing the need for fabrication tolerant design and nanometer-scale processing accuracy.

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3

Waveguide echelle gratings in SOI

In this chapter, we will discuss optical filters based on planar concave gratings, also called waveguide echelle gratings, fabricated on a nanophotonic SOI platform. In a first section, we will explain the device layout and the basic properties of the grating. In a second section, we show that the nanophotonic SOI platform offers important advantages for the fabrication of these echelle gratings as compared to other material systems. A third section elaborates on the design, the simulation and the experimental results. In a last part, we demonstrate cascaded filters based on these echelle gratings.

3.1 Introduction

Few devices invented by man have contributed more to our understanding of the physical world than the diffraction grating. The first experiments with diffraction gratings carried out in the 1820s by Joseph von Fraunhofer proved they were extraordinary tools for studying the world at both microscopic and cosmological scale. A well-written retrospective can be found in [1]. As of today, the applications of diffraction gratings are numerous: x-ray diffraction studies of crystals, monochromators, spectrometers, wavelength division multiplexing (WDM) devices for optical communications, distributed feedback (DFB) and distributed Bragg reflector (DBR) lasers, fiber Bragg gratings (FBGs) and many other optical instruments and devices.

The first man-made diffraction grating was fabricated around 1785 by the American astronomer David Rittenhouse, who wrapped a wire between two finely threaded screws. At the end of the 19th century, Rowland developed the first concave reflection grating which provided both diffraction and imaging with a single device [2]. As of today, the concave grating in a Rowland configuration is still being widely used both in modern spectroscopic instruments but also in integrated planar concave gratings (PCGs) as presented in this chapter. The first demultiplexers based on a grating etched in a slab waveguide were demonstrated in the early 1990s in various material systems including silica-on-silicon and III-Vs [1]. As explained in chapter 1, the integration of photonic functions on a single chip offers many advantages: compactness, reliability, stability and significantly reduced fabrication and packaging costs. Moreover, because integrated gratings - in contrast with free-space bulk gratings - are defined by means of photolithographic techniques, there is no design restriction on the exact position or shape of the focal field (output channels) and the grating facets. This allows to slightly shift these positions away from the exact Rowland geometry, not only to decrease aberrations [3] (see paragraph 3.6.3) but also to tailor the spectral shape of the channel transmission [4] or to obtain a focal field parallel to the chip edge for easy hybridization with photodetectors or fiber arrays [5].

In chapter 2, we mentioned that PCGs fabricated in low to medium index contrast material systems (e.g. silica-on-silicon, InP/InGaAsP, GaAs/AlGaAs) often suffer from large optical losses and low channel extinction ratios. This is mainly caused by the deeply etched grating which is very sensitive to fabrication imperfections. In this chapter, we will elaborate on the first time demonstration of a PCG fabricated on a nanophotonic SOI platform [6]. We will show that this material system offers many advantages

for the fabrication of PCGs as compared to other material systems and that most of the existing issues can be solved. Next to the general advantages such as high integration density and compatibility with CMOS processing, there are more PCG-specific advantages. First, as the slab waveguide is only a few hundred nanometer thick, there is no need for dedicated deep etching techniques to define the grating facets. Also, the strict fabrication tolerances on facet non-verticality which exist in other material systems are strongly relaxed and finally there is no deterioration of insertion loss and crosstalk caused by multimodal propagation in the slab region. To solve the issue of polarization sensitivity, we will demonstrate that by making use of 2D grating couplers, a polarization diversity approach can be implemented (see paragraph 3.7.3.1).

3.2 Device layout

A concave grating combines the function of a flat grating to spatially separate (demultiplex) or combine (multiplex) different wavelengths from the input waveguide(s) and a focal lens to focus the light into one or a series of output waveguides. A SEM picture of a fabricated 1×4 demultiplexer with one input- and four output waveguides is shown in figure 3.1. A schematic drawing of the device is shown in figure 3.2(a). The input waveguide ends at point I and connects with an unetched slab waveguide, called the free propagation region (FPR). In the FPR, the light beam propagates and expands into the direction of the grating. The concave grating both diffracts and refocuses the reflected light back into a series of output waveguides. This device can also be used to multiplex four wavelength channels. In that case, the input waveguide becomes an output waveguide and the four outputs become the four inputs.

Next to the standard Rowland geometry [2, 7, 8], we will also discuss more advanced layouts in this chapter, such as configurations with one and two stigmatic (i.e. aberration-free) points.

3.2.1 Rowland configuration

The design principles of a PCG based on the Rowland configuration are well known and widely described in literature [9]. In this particular mounting, the input and output waveguides are positioned along a circle with a radius R, called the Rowland circle. The grating facets on the other hand sit on a grating circle with a radius $2R$ and both circles touch at the middle of the grating, called the pole (P). The centers of the individual grating facets are positioned on the grating circle in such a way that, when projected onto

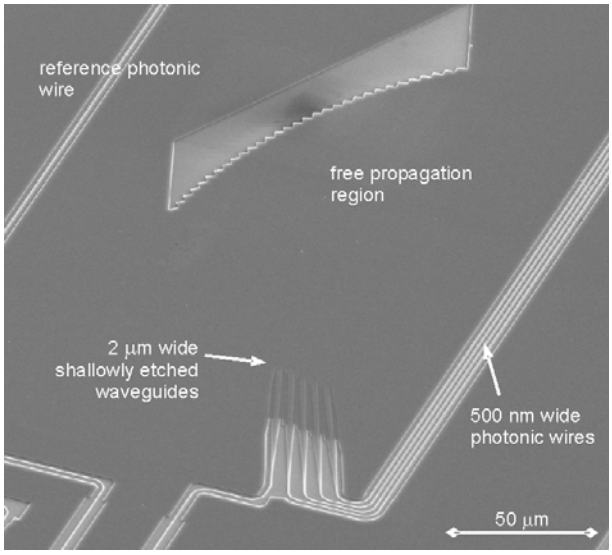


Figure 3.1: SEM picture of a fabricated 1×4 PCG demultiplexer

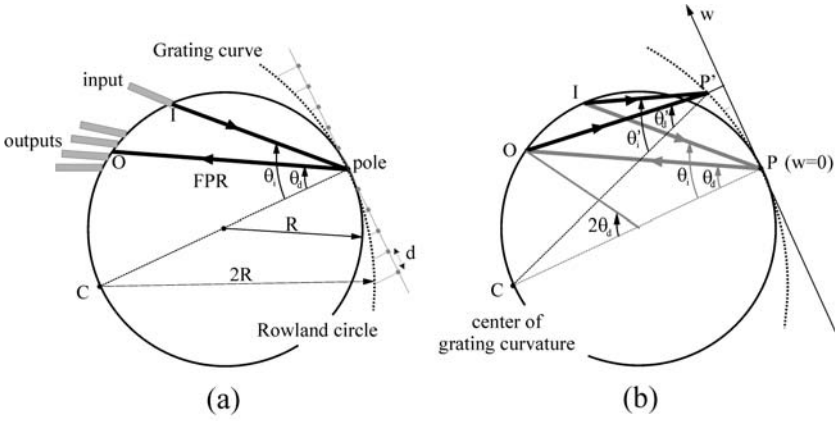


Figure 3.2: (a) Schematic drawing of a PCG demultiplexer based on a Rowland configuration and (b) geometry of the Rowland layout

the tangent of the circles at the pole, they are spaced equidistantly at distance d, the grating period, as can be seen in figure 3.2(a).

Using this configuration, any point on the Rowland circle is imaged on the same circle with a reflection angle determined by the grating equation:

$$d(sin\theta_i + sin\theta_d) = m\frac{\lambda}{n_{eff}} \tag{3.1}$$

where d is the grating period, θ_i and θ_d are the angles between the grating normal at the pole and the incident and diffracted beams respectively. The whole number m is the order of diffraction, λ is the wavelength in vacuum and n_{eff} is de effective index of the slab mode.

To demonstrate that light from a point source on the Rowland circle is focused on another point on the same circle, consider the two reflecting grating surfaces at P and P' as shown in figure 3.2(b). There is a theorem which states: "if two triangles are inscribed in a circle and share a chord of the circle as a common side, then the angles opposite this common side are equal". If the grating is small enough, both P and P' can be considered to be on the Rowland circle. In this case, the cord IC is common to the triangles IPC and $IP'C$ and thus $\theta_i = \theta_i^{'}$. So for each point on the grating, the angle of incidence in respect with the grating normal is the same. Equation 3.1 predicts that in this case, the angle of diffraction will also be the same for each point along the grating: $\theta_d = \theta_d^{'}$ (figure 3.2(b)). According to the same theorem, the diffracted beams will focus on the same point O on the Rowland circle.

3.2.2 Positioning of the grating facets along the grating curve

Equation 3.1 states the condition for constructive interference for diffracted beams from adjacent grating facets. The incident and diffracted angles are related by the same equation as in the case of a planar grating. This equation allows us to calculate the position of the focal point but it tells us nothing about the image quality. This can be analyzed by evaluating the expression for the path length $(IP' + P'O)$ for a ray that is incident on the grating at a general point P'. One can show that for the Rowland configuration, the pathlength $(IP' + P'O)$ can be expressed in terms of a single coordinate of P, the w coordinate (with the zero coordinate being the grating pole, see figure 3.2(b)). The difference in path length ΔL for rays passing via P' and P can be written as follows [10]:

$$\begin{aligned}\Delta L &= (IP' + P'O) - (IP + PO) \\ &= -w(sin\theta_i + sin\theta_d) + \frac{w^4}{(2R)^3}\left[\frac{sin^2\theta_i}{cos\theta_i} + \frac{sin^2\theta_d}{cos\theta_d}\right] \\ &+ \frac{w^5}{(2R)^4}\left[\frac{sin^3\theta_i}{cos^2\theta_i} + \frac{sin^3\theta_d}{cos^2\theta_d}\right]\end{aligned} \tag{3.2}$$

The expansion has been limited up to the fifth order in w. In order for the grating to diffract the light from point I and for the light to constructively interfere at O, the path length difference ΔL between neighboring facets should differ by an integral number of wavelengths where the integer is the order of diffraction, m. If one grating facet is centered around P, then the other grating facets should be positioned along the grating curve so that

$$\Delta L \quad = \quad km\frac{\lambda}{n_{eff}} \tag{3.3}$$

where k is an integer that gives the "number" of the grating facet (i.e. the k^{th} element counted from P). If we consider the region of the grating around the pole ($w \ll 2R$) then the fourth and fifth order terms are negligible in comparison to the leading term. In this case, the w-coordinate of the k^{th} grating facet can be found by the expression

$$\Delta L = km\frac{\lambda}{n_{eff}} = -w_k(sin\theta_i + sin\theta_d) \tag{3.4}$$

This equation shows that the region of the grating around the pole P will focus light with a wavelength λ from point I to point O if the spacing between the grating facets has a constant projection d onto the w axis. The constant projection is given by

$$d = \left|\frac{w_k}{k}\right| = \frac{m\lambda}{n_{eff}(sin\theta_i + sin\theta_d)} \tag{3.5}$$

This equation is identical to the grating equation and confirms that for the Rowland configuration, the centers of the grating facets should, to a first approximation, have a spacing whose projection onto the w axis is constant

and equal to the grating period d. This solution however is based on the assumption that the higher order terms in the path length expression may be neglected. These terms will become more significant further away from the pole and in the case of the Rowland mounting where the projection onto the w axis is constant, they describe the path length errors that degrade the image quality. For example, the fourth order term in w in expression 3.2 is analogous to the spherical aberration of lenses [10].

3.3 Basic properties

Out of the grating equation (equation 3.1) and the Rowland geometry (figure 3.2), important parameters such as the linear dispersion (LD) and the free spectral range (FSR) can be deduced [9]. By differentiation of the grating equation, we obtain the grating angular dispersion:

$$\frac{d\theta_d}{d\lambda} = \frac{1}{cos\theta_d}\frac{m}{d}\frac{n_g}{n_{eff}^2} \tag{3.6}$$

where m is the order of diffraction, d is the grating period and n_g is the group index of the slab mode:

$$n_g = n_{eff} - \lambda\frac{dn_{eff}}{d\lambda} \tag{3.7}$$

The linear dispersion is defined as the shift of the image along the Rowland circle per unit of wavelength shift. From the construction of the Rowland geometry (figure 3.2), we obtain the expression of the LD:

$$LD = 2R\left(\frac{d\theta_d}{d\lambda}\right) = \frac{2R}{cos\theta_d}\frac{m}{d}\frac{n_g}{n_{eff}^2} = \frac{2R}{\lambda}\frac{(sin\theta_i + sin\theta_d)}{cos\theta_d}\frac{n_g}{n_{eff}} \tag{3.8}$$

The LD is an important parameter as it determines the wavelength spacing $\Delta\lambda$ between two demultiplexer channels for a given spacing Δs between the output waveguides along the Rowland circle: $LD = \frac{\Delta s}{\Delta\lambda}$

The expression of the FSR can be deduced from the grating equation by setting the condition that the direction of a diffracted beam with wavelength λ in an order $(m+1)$ is the same as the direction of a beam with higher wavelength $(\lambda + \delta\lambda)$ diffracted in a lower order m:

$$FSR = \frac{\lambda}{m}\left[1 - \frac{m+1}{m}\left(1 - \frac{n_g}{n_{eff}}\right)\right]^{-1} \tag{3.9}$$

In most publications, the term $dn_{eff}/d\lambda$ is not taken into account and n_g is replaced by n_{eff} in equation 3.8 and 3.9. We will show later that for the nanophotonic SOI platform, the term $dn_{eff}/d\lambda$ is important and cannot be neglected.

As can be seen in equation 3.8, the LD is proportional with the Rowland radius, R and hence the size of the device. This means that for a given pitch of the output waveguides, Δs, the device size is inverse proportional to the channel spacing, $\Delta\lambda$: the denser the wavelength filtering, the larger the device.

3.4 Echelle gratings fabricated on nanophotonic SOI

As mentioned in chapter 2, integrated diffraction gratings etched in slab waveguides have been fabricated in many material systems. In 2007, we demonstrated for the first time a grating demultiplexer on a nanophotonic SOI platform [6] and proved that this material system offers many advantages for the fabrication of PCGs in terms of device cost, size and performance.

We fabricated echelle grating demultiplexers on 200mm SOI wafers with a silicon waveguide layer of 220nm and a buried oxide layer of 2μm. The devices were fabricated in the CMOS line of IMEC-Leuven using 248nm and 193nm deep-UV lithography in combination with ICP-RIE etching. The fabrication on high quality, low cost SOI wafers using waferscale CMOS processing techniques opens the way for the realization of low cost components that can be mass fabricated.

Due to the high refractive index contrast, PCGs on nanophotonic SOI can be made spectacularly smaller as compared with similar PCGs in other material systems. This high refractive index contrast allows to closely space the output waveguides along the Rowland circle while avoiding optical coupling between them. In glass material systems for example, the waveguide mode size at the input is limited to a minimum of several micrometers, and coupling between closely spaced waveguides also limits the dense packing of the output waveguides. The size of the PCG can be calculated by means of equation 3.8: the Rowland radius, R scales linearly with the required linear dispersion of the design. By closely spacing the output waveguides, the required LD and hence the size of the device for a given channel spacing $\Delta\lambda$ can be strongly reduced. In our designs, the output waveguides are typically spaced only 5μm apart on the Rowland circle (see paragraph 3.6) and this makes it possible to shrink the device by a factor 3 as compared to reported silica-on-silicon PCGs [11], a factor 3 to 5 as compared with InP/InGaAsP PCGs [12, 13] and a factor 4 as compared to PCGs on

	Nanophotonic SOI platform, Si slab height = 220nm	Large-core SOI platform, Si slab height = 5μm [14]
λ	1.55μm	1.55μm
n_{eff}	2.83	3.47
$dn_{eff}/d\lambda$	-0.57μm^{-1}	-0.08μm^{-1}
$(1 - \frac{\lambda}{n_{eff}} \frac{dn_{eff}}{d\lambda}) = \frac{n_g}{n_{eff}}$	1.31	1.04

Table 3.1: Comparison of the properties of the fundamental TE slab mode for two different SOI platforms

a large-core SOI platform [14]. On top of that, photonic wire access waveguides with a bend radius of a few micrometer allow to further decrease the size of the device [15–17]. In chapter 6, we will demonstrate for example the routing of 30 wavelength channels to on-chip photodetectors using photonic wire waveguides.

Not only the high refractive index contrast, but also the high modal dispersion of the 220nm thick Si waveguide layer is advantageous in terms of size reduction. The effective index of refraction of the fundamental TE-polarized slab mode n_{eff} = 2.83 around a central wavelength of 1.55μm. The change of this index as a function of wavelength $dn_{eff}/d\lambda$ = -0.57 μm^{-1}, resulting in a group index n_g of 3.7. Equation 3.8 shows that the larger the ratio of the group index over the effective index, the smaller the device size for a given linear dispersion and a given design will be. Table 3.1 gives a comparison between typical values of n_g/n_{eff} for the nanophotonic SOI platform considered in this paper and an SOI platform with a 5μm high Si slab waveguide [14]. From the values stated in table 3.1, we can conclude that the demultiplexer with the same layout and specifications (LD, λ, m, θ_i and θ_d) can be made roughly 21% smaller on the SOI platform considered in this paper as compared to a large-core SOI platform.

If we compare the required Rowland radius for PCGs on SOI and miniature spectrometers based on bulk free-space diffraction gratings, the difference is even more striking. In vacuum or air, the dispersion is negligible. More important, miniature near-infrared spectrometers make use of linear InGaAs photodetector arrays, typically containing 512 or 1024 pixels. The pixel pitch of modern linear arrays is $\sim 25 - 50\mu$m [18]. This is an order of magnitude larger as compared with the 5μm pitch of the SOI waveguides and will result in devices which are also an order of magnitude larger for the same device specifications. Moreover, due the photolithographic defini-

tion of the waveguide apertures and grating facets, integrated spectrometers offer more design freedom, accuracy and reliability.

PCGs fabricated in more conventional material systems such as silica-on-silicon [11], InP/InGaAsP [13] and large-core SOI substrates [14] have a grating which is defined by etching completely through the typically several micrometer thick waveguide layer. In these material systems, the tolerance on grating verticality is very stringent. For example, a deviation from verticality of 2° results in an dramatic excess loss of 10dB in the InP/InGaAsP platform in [13]. For the nanophotonic SOI platform as presented in this work, we only need to etch through the 220nm Si waveguide layer and a deviation of 10° from verticality results in a minor excess loss of ∼0.3dB. This will be discussed in more detail in paragraph 3.6.4.2. As the tolerance of grating verticality on nanophotonic SOI is very relaxed, we do not need to make use of dedicated deep etching techniques [11, 13] and the grating and waveguides can be defined in the same processing steps.

Another advantage of the thin slab waveguide in terms of performance is the absence of propagation of higher order modes in the vertical direction (see paragraph 3.8). In most other material systems, this behavior is responsible for creating so-called "ghost-peaks" in the transmission spectrum. This is due to the fact that different modes have different effective refractive indices and as a consequence, will be focused on a different point along the Rowland circle.

3.5 Simulations

3.5.1 Introduction

To verify our designs, we performed optical simulations to analyze the influence of the different design parameters on the transmission spectrum of the PCGs. Due to their large size (in terms of wavelength), it is impossible to fully simulate a PCG with a numerical method such as FDTD because of the large computation time and memory needed.

Due to its simplicity, scalar diffraction theory has become popular and is commonly used for the simulation of PCGs [19–22]. However, this method has some limitations. The accuracy can become limited if the grating facets are relatively small in respect to the wavelength (i.e. for low diffraction orders or large angles of incidence). More important, this scalar diffraction method does not take into account the polarization dependent behavior of the grating diffraction. This has been solved by adopting a hybrid simulation method in which scalar diffraction formulas are used for the calculation of the propagation in the slab region and a rigorous coupled-

wave analysis (RCWA) is used to calculate the diffraction at the grating [23, 24]. Other simulation methods that also take into account the polarization dependence of the grating are based on MoM (method of moment) [25] and BEM (boundary element method) [26].

We have chosen to write a simulation program that is based on scalar diffraction theory because our PCGs but also the fiber couplers and photonic wire waveguides are designed for TE-polarized light only. If polarization independent behavior is needed (for receiver applications for example), a polarization diversity approach can be used. This will be discussed in detail in paragraph 3.7.3.

The simulation program is implemented in Matlab and is able to calculate the grating parameters for a certain design with a given central wavelength, free spectral range and channel spacing $\Delta\lambda$. After determining the PCG parameters, the transmission spectrum can be calculated. This program also provides all the coordinates of the PCG layout which are necessary for the fabrication of the lithography masks (gds-file).

3.5.2 Scalar diffraction theory

The entire simulation can be divided into the following parts:

1. Calculation of the incident field on the grating
2. Calculation of the diffracted field from the grating along the Rowland circle
3. Calculation of the overlap between the diffracted field and the output waveguide modes for different wavelengths

First of all, we calculate the incident field on the grating facets. This is done by propagating the field at the input aperture into the FPR section. Secondly, we calculate the diffracted field from the grating to the Rowland circle. The last step is the calculation of the spectral response. The spectral response of a channel can be obtained by calculating the overlap integral of the output waveguide mode(s) and the diffracted field over the output waveguide cross-section for different wavelengths. A schematic view of the grating and the coordinate system used is shown in 3.3.

3.5.2.1 Calculation of the incident field on the grating

According to the Kirchhoff-Huygens diffraction formula, the incident electric field E_{inc} at the center points of the grating facets (P') at a distance r_1 and at an angle α can be calculated as:

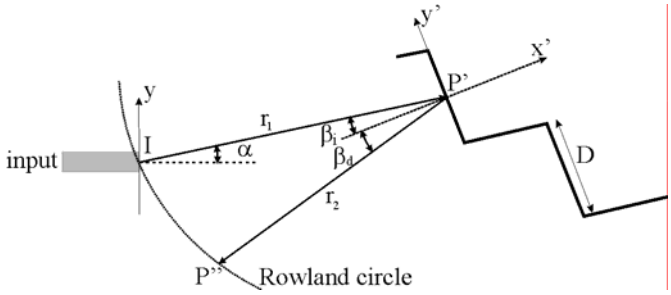


Figure 3.3: Schematic view of the grating and the coordinate system used for simulations

$$E_{inc}(P') = \frac{1}{2}\sqrt{\frac{n_{eff}}{\lambda}}\int_{input} E_{wg}(y)\frac{e^{-jkr_1}}{\sqrt{r_1}}(1+cos\alpha)dy \quad (3.10)$$

where $k = 2\pi n_{eff}/\lambda$ is the wavenumber within the slab waveguide and E_{wg} is the electric field profile of the TE-polarized fundamental mode of the input waveguide. This formula is the 2D variant of the more general Fresnel-Kirchhoff diffraction formula [7].

Depending on the needed accuracy, different approximations can be made to solve this equation. A first approximation, which works well for low index contrast material systems is to approximate the waveguide mode profile E_{wg} by a Gaussian functions with a certain mode width [19]. In this case, equation 3.10 can be directly solved by an analytical expression. However, for higher index contrast systems (like SOI), this approximation is less accurate as the exponential mode tails and the discontinuity in the electric field perpendicular to the waveguide sidewall become important.

Another point of attention is the one-dimensional representation $E_{wg}(y)$ of the two-dimensional mode profile of the waveguide aperture. One option is to use an effective index approximation. Again, the accuracy increases for waveguides with a lower index contrast. Another option is to use a horizontal slice of the 2D field through of vertical position of the waveguide for which the field is maximal. These issues are also present in the design of SOI AWGs and are described in more detail in the PhD of P. Dumon [27]. The standard apertures we use are 2μm wide shallowly etched waveguides (see paragraph 3.6.2). The index contrast of these shallowly etched waveguides is smaller than the contrast of 500nm wide photonic wire waveguides and both options, as described above, are good approximations and result in similar 1D mode profiles. We calculate the eigenmodes of the

waveguides using a 2D mode solver (Fimmwave). We extracted a horizontal slice to obtain a 1D mode profile and imported this data in Matlab.

As mentioned before, our standard PCG designs have 2μm wide shallowly etched waveguides apertures and only the fundamental mode of these waveguides is launched in the FPR. This will be discussed in paragraph 3.6.2. For tailoring the shape of the channel response other waveguide apertures with more complex mode profiles can be used such as multimode interference couplers (MMIs) [28].

3.5.2.2 Calculation of the diffracted field along the Rowland circle

Similarly, the diffracted field E_{out} on the Rowland circle is calculated by adding the fields of all the grating facets:

$$E_{out}(P'') = \frac{\eta}{2}\sqrt{\frac{n_{eff}}{\lambda}} \sum_{grating} \int_{-D/2}^{+D/2} E_{inc}(y')\frac{e^{-jkr_2}}{\sqrt{r_2}}(cos\beta_i + cos\beta_d)dy' \quad (3.11)$$

where β_i and β_d are the incident and diffracted angles with respect to the normal of each grating facet and η is the reflection coefficient of the grating. The reflectivity at the Si/air interface of a grating facet is about 30% as will be discussed in paragraph 3.6.4. The energy of light diffracted by each grating facet can be guided in a specific direction (blaze point O, see figure 3.2) by inclining the facets. This procedure is called blazing the grating. For an optimal diffraction efficiency, both β_i and β_d should be kept as small as possible as can be seen in equation 3.11. This is the case if the blaze point O is positioned as close as possible to the input waveguide aperture I. Then, the angle of incidence and diffraction, θ_i and θ_d are nearly equal (see figure 3.2) and the grating facets are almost perpendicular illuminated: $\beta_i = 1/2|\theta_i - \theta_d| \simeq 0$ for the center facet at the grating pole (see figure 3.2 and 3.3). This configuration is called the Eagle mounting [1].

Equation 3.11 simplifies a lot if we assume that the magnitude of the incident field, $|E_{inc}|$ is constant over each facet and the phase of this field changes linearly along the length of the facet:

$$E_{inc}(y') = E_{inc}(y' = 0)e^{+jky'sin\beta_i} \quad (3.12)$$

This approximation is valid if the size of the facets is small compared to the distance to the input and if the angle of incidence β_i is small. These conditions are easily fulfilled. First of all, β_i is small for near-Eagle mountings. Secondly, the size of the facets are typically a few micrometer, whereas the distance between the input aperture and the facets is typically hundreds to thousands of micrometer: $D \ll r_1$.

By making use of the following assumptions:

$$\begin{aligned} e^{-jkr_2} &= e^{-jk(R_2+y' sin\beta_d)} \\ r_2 &= R_2 \text{ (in the denominator of equation 3.11)} \\ sin\beta_i = \beta_i \quad &; \quad sin\beta_d = \beta_d \\ R_2 &= |P'P"| \\ (cos\beta_i + cos\beta_d) &= \text{ constant as a function of } y' \end{aligned} \tag{3.13}$$

we obtain this analytical expression:

$$E_{out}(P'') = \frac{\eta}{2}\sqrt{\frac{n_{eff}}{\lambda}} \sum_{grating} D.\frac{e^{-jkR_2}}{\sqrt{R_2}} E_{inc}(y'=0)(cos\beta_i + cos\beta_d)\frac{sin[k(\beta_i-\beta_d)D/2]}{[k(\beta_i-\beta_d)D/2]} \tag{3.14}$$

This means that the output field is a summation of sinc-shaped field profiles. These are the far field profiles of the individual grating facets. These sinc-functions reach a maximum for $\beta_d = \beta_i$. Each grating facet is inclined in a such a way that this direction corresponds with the blaze point O.

It is important to notice that the width of the grating facets also determines the loss variation over the wavelength range of application. This can be easily calculated using equation 3.14. As the grating facets become smaller, the sinc-shaped diffraction envelope of a single grating facet will broaden, resulting in smaller loss variations over a given spectral range [9].

3.5.2.3 Calculation of the spectral response

Finally, the spectral response of each channel can be obtained by calculating the overlap integral between the diffracted field E_{out} and the field profile modes of the output waveguides:

$$I(\lambda) = \frac{\left| \int E_{out}(\lambda, y").E^*_{outputWG}(\lambda, y")dy" \right|^2}{\int |E_{outputWG}(\lambda, y")|^2 \, dy". \int |E_{inputWG}(\lambda, y)|^2 \, dy} \quad (3.15)$$

Again, the 1D mode profiles were calculated using Fimmwave and imported in Matlab. The standard output apertures are the same as the input apertures: 2μm wide shallowly etched waveguides. These waveguides support higher-order modes but these modes are filtered out as the waveguides are adiabatically tapered down to 500nm wide, single-mode photonic wires. This means we only need to calculate the overlap integral between the diffracted field and the field profile of the fundamental mode of the output waveguide. For applications in which a rectangular shaped (flat-top) spectral response is needed, a broad multimode output waveguide can be used. In this case, it is necessary to include higher order modes [20, 29].

3.6 Design of echelle gratings on nanophotonic SOI

3.6.1 Introduction

The design process starts with determining the order of diffraction. Equation 3.9 gives the relation between the order of diffraction and the FSR. As the FSR has to be larger than the operational spectral range of the demultiplexer, the upper limit of the order of diffraction can be calculated. The operational range is equal to the number of channels times the channel spacing. A diffraction order $m = 10$ results in a FSR of 115nm for a central wavelength of 1.55μm. Next, the incident and diffracted angles are chosen and from equation 3.1, we can calculate the grating period d. This parameter also determines the channel uniformity across the operational spectral range as explained above. Smaller grating facets will result in a smaller loss variation. This can be obtained by decreasing m as can be seen from equation 3.1, but then smaller grating facets are more sensitive to profile imperfections due to fabrication. Consequently, it is best to use the upper limit of the order of diffraction based on the calculation of the required FSR or channel uniformity.

Our standard PCGs have 2μm wide shallowly etched output waveguides which are spaced 5μm apart on the Rowland circle. Based on the required channel spacing $\Delta\lambda$ of the (de)multiplexer design, the linear dispersion can be calculated. The linear dispersion is the waveguide spacing divided by the channel spacing. The Rowland circle radius R and hence the size of the device can then be calculated from equation 3.8.

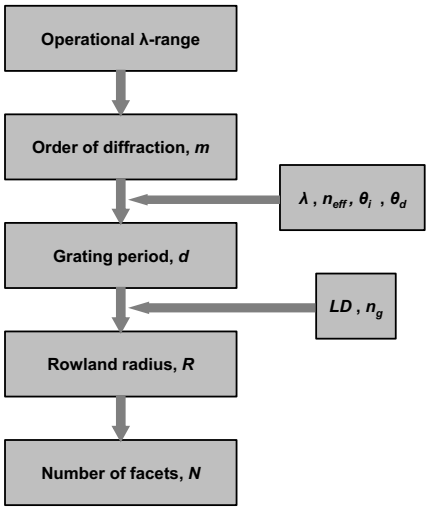


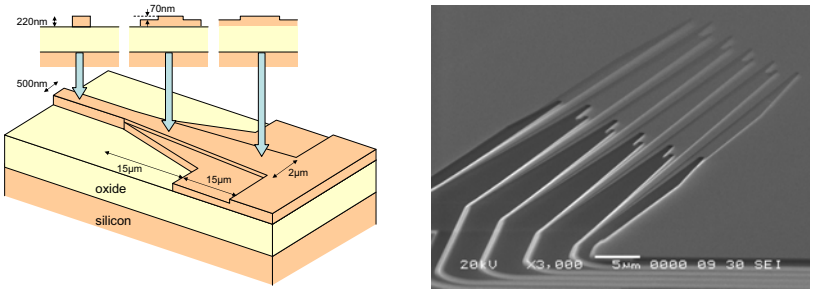
Figure 3.4: Possible design flow of a PCG demultiplexer

The grating facets are individually blazed to maximize their reflection at the blaze point O (figure 3.2). This point is chosen to be in the middle of the output waveguides in order to obtain a symmetrical response across the output channels. The number of facets should be chosen large enough in order to capture most of the incident light. The number of grating facets needed is determined by the distance between the input aperture and the grating, the width of the grating facets and the mode width of the input waveguide. The design method as explained here is schematically represented in figure 3.4

3.6.2 Waveguide aperture design

3.6.2.1 Aperture configuration

The apertures of the entrance and exit waveguides are positioned on the Rowland circle where they connect with the unetched free propagation region. In order to reduce the reflection loss at the interface between the waveguide and slab region, the waveguides are shallowly etched (70nm deep). This reduces the index contrast of the waveguide apertures and has already been successfully implemented by our group in the star couplers of AWGs [16]. Double adiabatic linear tapers are used for the transition from a 500nm wide deeply etched photonic wire waveguide to a broader (2μm) shallowly etched (70nm deep) waveguide aperture on the Rowland circle as



(a) (b)

Figure 3.5: Schematic view and SEM picture of the double adiabatic tapers for the transition from deeply etched 500nm wide photonic wire waveguides to shallowly etched 2μm wide waveguide apertures

can be seen in figure 3.5

The fiber couplers for interfacing with an optical fiber are shallowly etched as well (70nm deep). This allows to fabricate both structures in the same processing step.

3.6.2.2 Aperture position

According to formula 3.8, the ratio between the Rowland radius, R and the linear dispersion, LD can be expressed as follows:

$$\frac{R}{LD} = \frac{\lambda}{2} \frac{cos\theta_d}{(sin\theta_i + sin\theta_d)} \frac{n_{eff}}{n_g} \tag{3.16}$$

This means that for a certain design (LD, λ, n_g and n_{eff} fixed), the Rowland radius and hence the size of the PCG is strongly dependent on the position of the input and output waveguides. By assuming that $\theta_i = \theta_d = \theta$, equation 3.16 can be written as:

$$\frac{R}{LD} = \frac{\lambda}{4} \frac{cos\theta}{sin\theta} \frac{n_{eff}}{n_g} \tag{3.17}$$

This relationship is plotted in figure 3.6 for $\lambda = 1.55\mu$m and $n_g/n_{eff} = 1.31$ (table 3.1).

From this graph, we can conclude that large angles of incidence and diffraction will result in a compact device. However, we have to note that

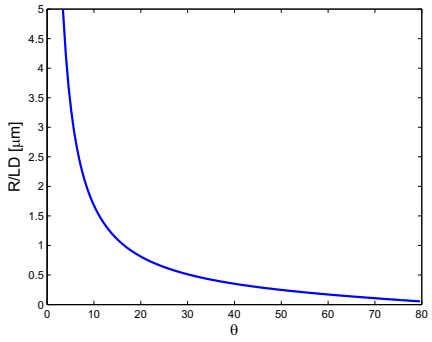


Figure 3.6: R/LD versus waveguide angle

when increasing the angle of diffraction, the effective waveguide spacing will decrease for a fixed waveguide pitch along the Rowland circle by a factor $cos\theta_d$. This means that when increasing the angle of diffraction, the waveguide pitch should also be increased to avoid coupling between them. So if we would plot the Rowland radius versus the waveguide angle θ for a design with a given channel spacing $\Delta\lambda$, the term $cos\theta$ disappears in equation 3.17.

In terms of device size, it might be advantageous to have large waveguide angles. However, the performance in terms of diffraction loss but more important side lobe level (crosstalk) will decrease with increasing waveguide angles. This is shown in figure 3.7. We simulated the performance of three PCGs with one 2μm wide shallowly etched waveguide and a linear dispersion $LD = 250$. This means that for a wavelength variation of 20nm, the image will shift over 5μm along the Rowland circle. The central wavelength is 1.55μm. At this wavelength, the light will be diffracted under an angle $\theta_i = \theta_d = \theta$. The only difference between these three designs is the angle θ. The design with $\theta = 10^\circ$ requires a Rowland radius $R = 838\mu$m. On the other hand, the PCG with $\theta = 60^\circ$ only requires a radius $R = 85\mu$m to realize the same LD. This can be seen in the data in figure 3.7. These drawings are not on scale and we assume perfectly reflecting grating facets.

We also plotted the diffraction back into the input waveguide by calculating the overlap integral of the diffracted field along the waveguide aperture (red line) and the fundamental mode of the waveguide. As can be seen, the larger the waveguide angle (and hence the more compact the PCG), the higher the insertion loss, the broader the spectrum and the stronger the side lobes. This will limit the crosstalk between neighboring channels. The worse performance for large angles of incidence is due to increased aber-

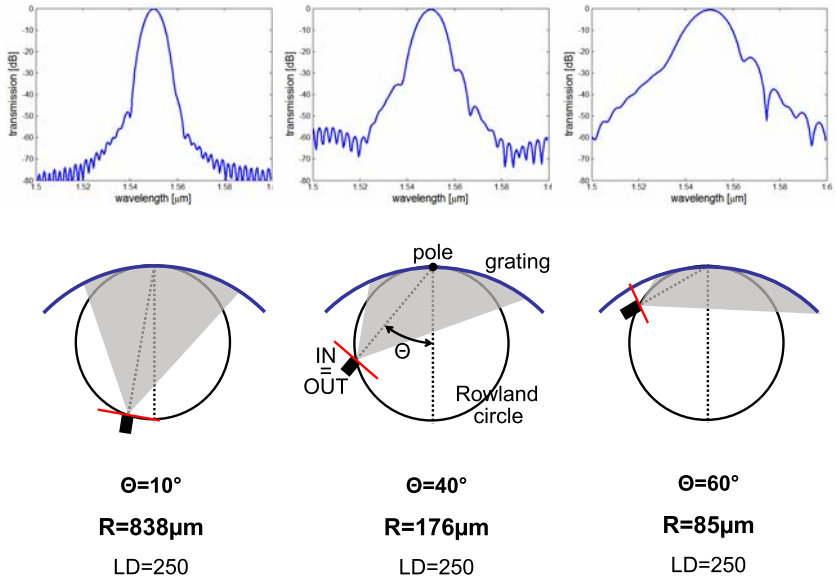


Figure 3.7: Three PCGs with identical linear dispersion ($LD = 250$) but different incident and diffraction angle ($\theta_i = \theta_d = \theta$) to demonstrate their influence on device size and performance. The spectral transmission is also plotted. Perfectly reflecting grating facets are supposed and the drawing is not on scale!

rations which are caused by illumination of facets further away from the grating pole. For these facets, the higher order terms in the expression of the optical path length (equation 3.2) become more important. This was discussed earlier. On top of that, larger angles of incidence will also result in larger shaded facets (i.e. the part perpendicular to the illuminated part of the facet). Using RCWA (Rigorous coupled wave analysis), it has been shown that due to this effect, the diffraction efficiency also decreases for increasing angles [30]. This effect however cannot be analyzed with scalar diffraction theory as shaded facets are ignored.

To conclude, it is clear that the choice of θ_i and θ_d involves a trade-off between device size and performance. In literature, angles between 30° and 50° are most common [13, 14, 31]. The waveguide angles of our first devices are also in this range. Smaller angles of incidence and diffraction have been reported mainly for applications in which a very large FSR (>100nm) and/or a high uniformity across the wavelength channels are needed [29, 32]. These designs require small orders of diffraction, $m < 10$ and in order to avoid a too small grating period, θ_i and θ_d have to be chosen small enough as can be derived from the grating equation (equation 3.1). Smaller grating facets tend to be more sensitive to grating profile imperfections such as corner rounding.

Also, to obtain an optimal diffraction efficiency, the input waveguide(s) and output waveguide(s) should be positioned as close as possible to each other. In this configuration (Eagle mounting), the angle of incidence and diffraction are almost equal and the grating facets are almost perpendicular illuminated (see paragraph 3.5).

3.6.2.3 Aperture width and spacing

The width of the shallowly etched apertures along the Rowland circle also strongly influences the device size and performance. Generally speaking, smaller waveguides allow a denser waveguide positioning along the Rowland circle. This results in a smaller LD and hence a smaller Rowland radius for a design with a given channel spacing $\Delta\lambda$.

On the other hand, the beam launched in the FPR has a larger angle of divergence for narrow waveguides. Narrow waveguides require a relatively large grating in order to capture the incident light. Again, this will result in increased aberrations as more grating facets further away from the grating pole will be illuminated. This is demonstrated in figure 3.8. We simulated three identical PCGs with one waveguide ,which acts both as input and output. The LD is 250 and the waveguide angle $\theta = 40°$. The plots at the top of figure 3.8 show the modulus of the incident electric field on

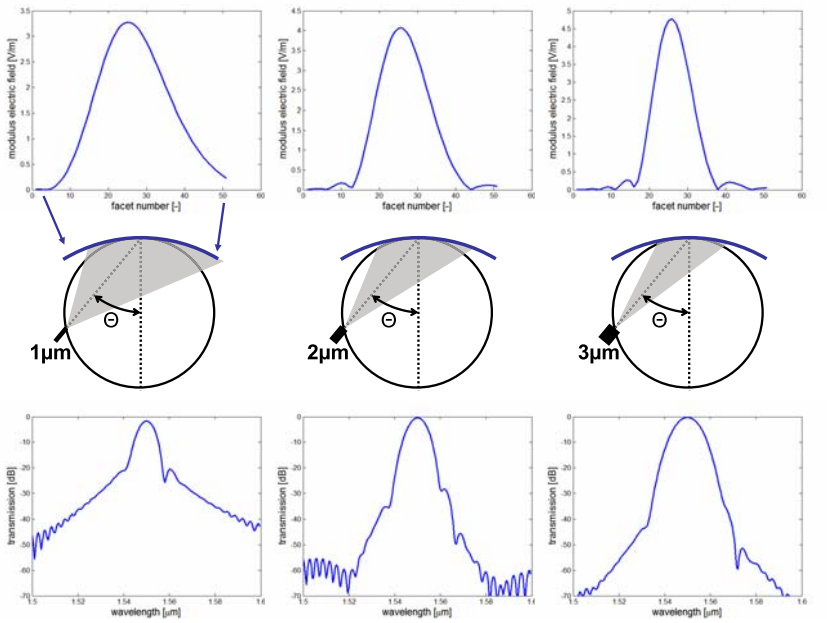


Figure 3.8: Three identical PCGs ($\theta = 40°, LD = 250$) but with different waveguide apertures (1, 2 and 3μm) are compared. The incident field on the grating and the spectral transmission are plotted for each configuration. Again, we consider facets with a reflectivity $\eta = 1$

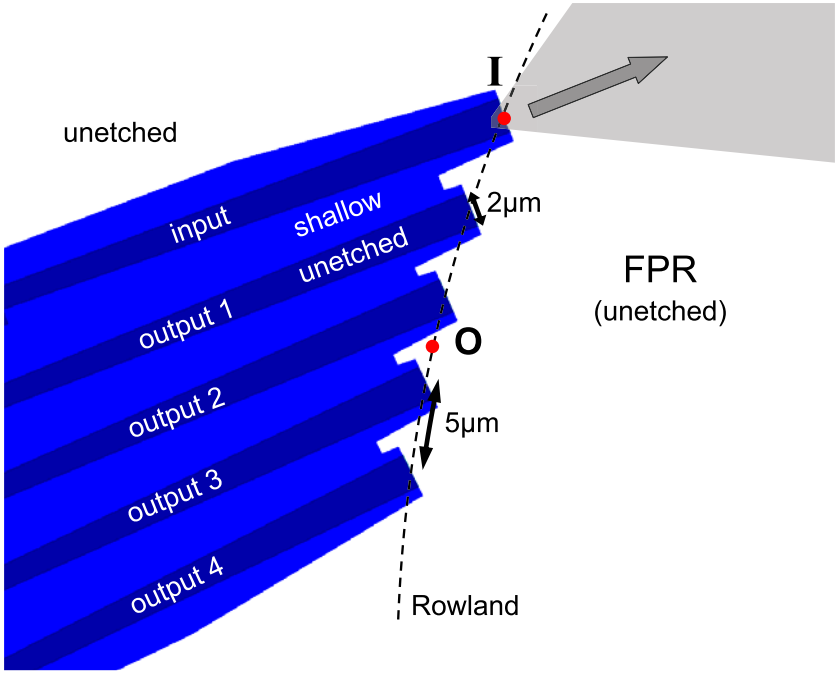


Figure 3.9: Mask layout of the waveguides along the Rowland circle for a 1×4 demux. Our standard waveguides have a center to center spacing of 5μm, are shallowly etched and 2μm wide

the grating facets. The left plot is for the PCG with a 1μm wide shallowly etched waveguide, the middle for 2μm and the right plot is for the 3μm wide waveguide. As can be seen, 50+ facets are needed to capture most of the light from the 1μm wide waveguide whereas only 30 and 20 facets are needed for the 2μm and 3μm wide waveguides respectively. The plots at the bottom show the diffracted signal back into the same waveguide. First of all, we notice that broader waveguides result in broader channel transmissions. This is because an image of the input field distribution is formed along the Rowland circle with a magnification of 1. More important, we notice that the side lobe level strongly increases for narrower waveguides due to the larger grating as described above.

Our standard devices have a waveguide aperture width of 2μm and a center to center spacing of 5μm along the Rowland circle. This is shown in figure 3.9. The aperture width of 2μm is a compromise between device size and performance (side lobe level). The waveguide pitch of 5μm is chosen in order to avoid optical coupling and shading between neighboring

waveguides. If the pitch is chosen too small, the trench of one waveguide can block the reflected light originating from the facets at the grating edge and prevent coupling into a neighboring waveguide.

3.6.3 Positioning of individual grating facets

3.6.3.1 Rowland mounting

For a standard Rowland configuration, the centers of the grating facets are positioned on the grating curve and their projection onto the tangent through the pole is equidistant with a spacing equal to the grating period d. In paragraph 3.2.2 we showed that in this case, the higher order terms in the path length expression are neglected. These higher order terms become significant for facets further away from the pole and give rise to aberrations, which degrade the imaging quality [10]. We previously demonstrated that these aberrations are responsible for the high side lobe level in PCGs with narrow input waveguides or large waveguide angles.

The residual aberrations can be reduced by shifting the position of the individual grating facets from the standard Rowland geometry. This procedure is called stigmatization. Designs with one or two stigmatic points are commonly used and clearly described in literature [33]. Figure 3.10 shows the PCG layout for these three different mountings: the Rowland mounting, a configuration with one stigmatic point/wavelength and a configuration with two stigmatic points. For each mounting, we also plotted the transmission spectrum of a 4-channel demultiplexer with a channel spacing of 20nm. The design parameters are summarized in table 3.3 and the positioning of the waveguide apertures are shown in figure 3.9. These PCGs are identical except for the exact positioning of their 31 grating facets. In order not to overload figure 3.10, we only plotted 7 out of 31 grating facets.

3.6.3.2 One stigmatic point mounting

For the one stigmatic (i.e. aberration-free) point design, the correction is performed for only one wavelength. Residual aberrations for other wavelengths will still exist. In the following, we will examine a configuration having a fixed point of incidence I and one stigmatic point O, both on the Rowland circle. The corresponding stigmatic wavelength is λ_1. The light of wavelength λ_1 is launched into the slab region at the input waveguide aperture I. It is then diffracted by the grating G and focused at point O where an output waveguide aperture can be located for receiving the wavelength λ_1. The imaging of the input field located at I onto O will be aberration-free if

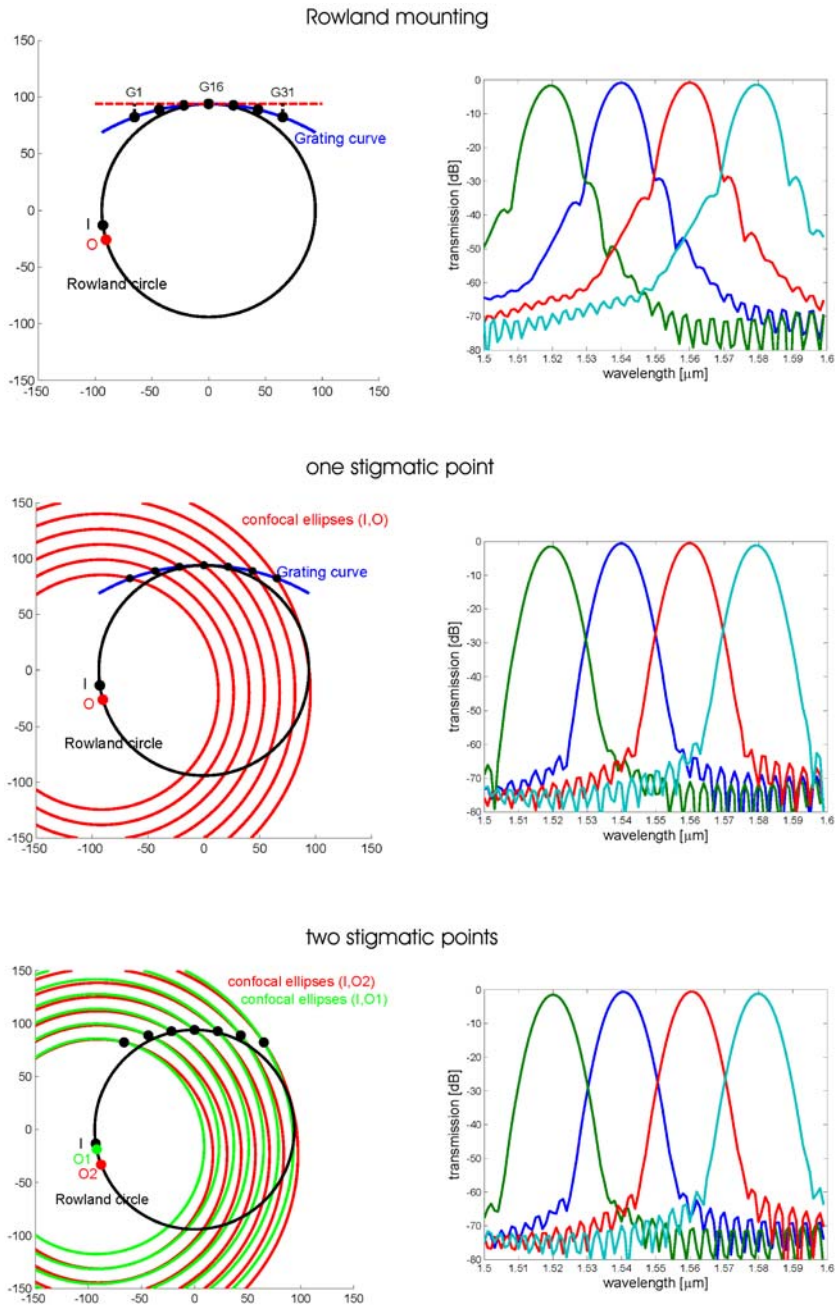


Figure 3.10: Overview of different grating mountings: standard Rowland configurations and mountings with one and two stigmatic points. The PCG is a 1×4 demux with a channels spacing of 20nm. The centers of 7 out of 31 grating facets are plotted

the path length difference ΔL for neighboring facets differs by an integral number m of wavelengths:

$$IG_{i+1} + G_{i+1}O - (IG_i + G_iO) = m\frac{\lambda_1}{n_1} \tag{3.18}$$

where n_1 is the effective refractive index of the slab mode at a wavelength λ_1. If the grating has N facets, equation 3.18 can be reduced to N equations with x_i and y_i being the $2N$ unknown coordinates of the centers of the facets. As these centers are also positioned on the grating curve, their position can then be found at the intersection of the grating curve and a family of confocal ellipses with I and O being the two focal points.

In our example the stigmatic wavelength is the central wavelength in the operating range (1.55μm). The corresponding stigmatic point O is located in the center of the output waveguide apertures (see figure 3.9). When comparing the transmission spectra of the Rowland mounting and the 1-stigmatic point configuration, we clearly see the improved imaging quality. The side lobes which appear at -30dB in the Rowland mounting almost completely disappear and the near-channel crosstalk decreases.

3.6.3.3 Two stigmatic points mounting

Even lower aberrations over the operational wavelength range can be obtained using a configuration with two stigmatic points [33]. In this case, two stigmatic points O_1 and O_2 corresponding with the stigmatic wavelengths λ_1 and λ_2 are chosen on the Rowland circle. For each facet G_i, two similar equations to equation 3.18 can be written:

$$\begin{aligned} IG_{i+1} + G_{i+1}O_1 - (IG_i + G_iO_1) &= m\frac{\lambda_1}{n_1} \\ IG_{i+1} + G_{i+1}O_2 - (IG_i + G_iO_2) &= m\frac{\lambda_2}{n_2} \end{aligned} \tag{3.19}$$

For each grating facet G_i these equations can be reduced to two equations for both optical paths $IG_i + G_iO_1$ and $IG_i + G_iO_2$. This means that the centers of the facets are no longer positioned along the grating curve but at the intersection point of two families of confocal ellipses. The first family has I and O_1 as focal points and the second family I and O_2.

In our example, the two stigmatic points $O1$ and $O2$ are fixed at channel one and channel four. As the channel spacing is 20nm, the corresponding

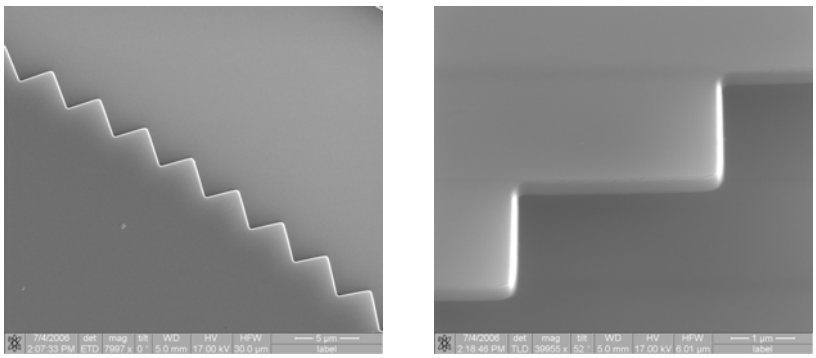
stigmatic wavelengths are 1.58μm and 1.52μm respectively (larger wavelengths diffract under larger angles). For each of these mountings, the position of the grating facets remain almost unchanged in the region around the grating pole as the phase errors in the central region of the grating are small. If we compare the spectra of the one- and two stigmatic mountings, there seems to be no major improvement. In the two stigmatic point mounting, the central wavelengths of channel 1 and channel 4 are exactly 1.58μm and 1.52μm respectively. This is not the case for the PCG in the one stigmatic mounting as the linear dispersion of the grating depends on λ, n_g, n_{eff} and θ_d. No major difference in the shape of the channel transmission is visible between the stigmatic mountings due to the fact that this design is rather conventional. More extreme devices (larger waveguide angles, narrower waveguide apertures, larger FSR) clearly show decreased side lobes for the two stigmatic point configuration.

P. Cheben showed that aberrations can be even further reduced by allowing small variations in the position of the input and output waveguides [1] from their original position at the Rowland circle. All these aberration reduction steps would be extremely difficult to realize with conventional bulk diffraction gratings, in contrast to integrated optics as presented in this work in which the optimized positions of both waveguides and grating can be easily produced using lithography and etching. A more general and detailed overview of these stigmatic mountings can be found in [33]. In paragraph 3.7, we will discuss experimental results of PCGs fabricated using these different mountings.

3.6.4 Design of grating facets

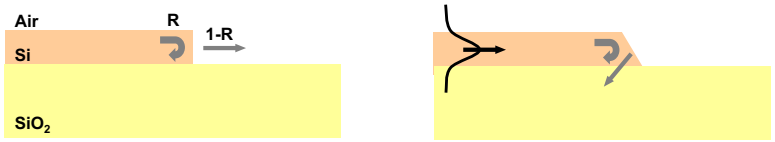
The concave grating of the PCG demultiplexer both diffracts and focuses the light onto one of the output waveguides depending on the wavelength of the incident light. Figure 3.11 shows two SEM pictures of standard grating facets, deeply etched in the silicon slab. The major issue of these etched grating facets is the small Fresnel reflection at the Si/air interface. This will result in a very high on-chip loss as only 35$\%$ of the light will be reflected by the grating. By changing the design of the grating facet or by coating the backside of the grating with a highly reflective metal, the grating reflectivity can be dramatically increased.

During this work, we demonstrated for the first time the use of distributed Bragg reflector (DBR) type facets. These facets fully exploit the accurate patterning possibilities of 193nm deep-UV lithography for the fabrication of very small features on a nanophotonic SOI platform and allow to increase the grating reflectivity without the need for additional pro-



(a) (b)

Figure 3.11: SEM pictures of 3μm wide flat grating facets



(a) Fresnel reflection loss at a perfectly vertical facet

(b) Loss due to grating non-verticality

Figure 3.12: Cross-section of a deeply etched SOI grating facet

cessing steps and without compromising on design freedom.

3.6.4.1 Reflection loss

Figure 3.12(a) is a drawing of the grating cross-section. The grating is defined by etching completely through the 220nm silicon waveguide layer. Using eigenmode expansion, the Fresnel reflection at the interface can be easily calculated. The deeply etched facet as shown in figure 3.12(a) has a reflectivity of 35% at a wavelength $\lambda = 1.55\mu$m, corresponding to a reflection loss of 4.6dB. When integrating active components (photodetectors, laser, modulators, ...) using BCB bonding or when protecting the wafers with on oxide cladding, the situation gets even worse. In case the air (n=1) top cladding is replaced by BCB (n=1.54), the reflectivity is only 18%, resulting in a reflection loss of 7.3dB.

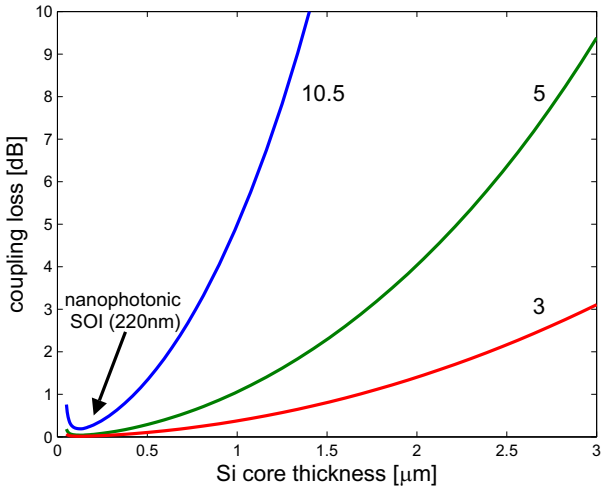


Figure 3.13: Excess coupling loss between incident and reflected fundamental TE slab mode ($\lambda = 1.55\mu$m) as a function of Si core thickness. Parameter is the deviation from verticality (degrees)

3.6.4.2 Non-verticality of the etched grating

A second contribution to the total grating reflection loss is caused by the non-verticality of the grating facets. This causes excess coupling loss between the incident fundamental slab mode and the reflected fundamental slab mode as shown in figure 3.12(b). As mentioned before, ICP-RIE dry etching is used for the definition of our structures, including the grating facets. This process is not optimized to create perfectly vertical sidewalls and results in a rather large non-verticality of 10.5° for the first generation devices. However, this only gives rise to an additional loss of 0.3dB. This brings the total modal reflection loss including Fresnel loss at 4.9dB. These reflection losses were calculated by means of eigenmode expansion. A staircase approximation was used for the simulation of the reflection loss at the angled facet.

It is important to mention that PCGs fabricated in most other material systems (large-core SOI substrates, InP, GaAs, silica, ...) have a several micrometer thick free propagation region with deeply etched grating facets [11, 13, 14]. In these materials, a similar sidewall non-verticality would completely destroy the transmission characteristics as can be seen in figure 3.13. In this figure, we plotted the modal reflection loss as a function of silicon core thickness for different values of grating non-verticality. This was done by calculating the overlap integral between the fundamental modes

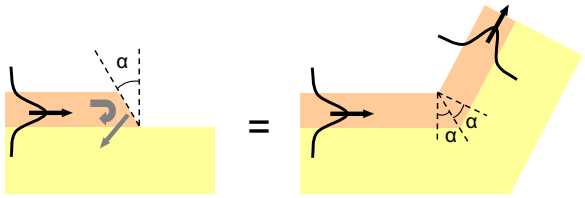
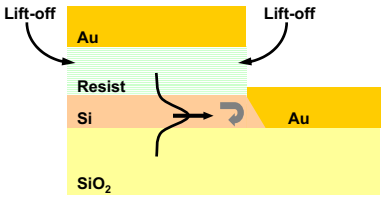
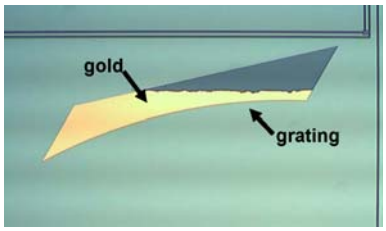


Figure 3.14: Calculation method of reflection loss at a tilted facet. From an electromagnetic field point of view, the modal reflection at a tilted facet with α being the deviation from verticality can be modeled as a mode-coupling problem between two identical waveguides, joined with an angle of 2α



(a) Drawing of the situation after evaporation but before lift-off



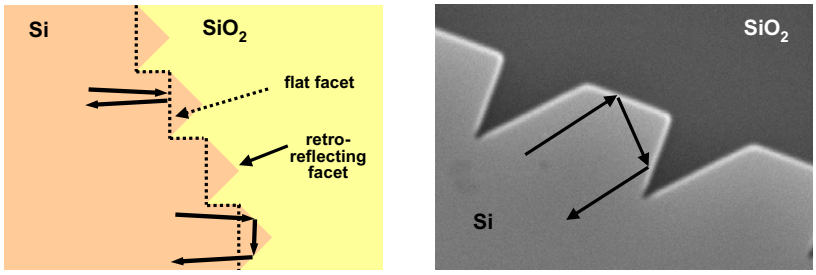
(b) Top view of the grating trench filled with gold

Figure 3.15: Metal coated grating facets

of two tilted slab waveguides (figure 3.14). An even thinner Si core layer (<220nm) could be envisioned, further decreasing the reflection loss at the angled facets. However, when the core layer becomes too thin (<130nm), mode size will increase again resulting in a higher modal reflection loss as can be seen in figure 3.13.

3.6.4.3 Metal coated grating facets

A popular technique to reduce the reflection loss at the grating facets is to coat the backside with a layer of highly reflecting metal (gold, aluminum) [11, 29, 34]. This is mostly done by means of tilted evaporation. A drawback of this method is that is cannot be carried out on a waferscale. We applied another technique: before stripping the photoresist used to define the deeply etched structures (wires, broader waveguides and diffraction gratings), we evaporated a 220nm thick gold layer on the etched gratings making use of a plastic evaporation mask to cover other deeply etched trenches



(a) Schematic drawing. Incident light comes from the left, confined in the slab waveguide

(b) SEM picture of fabricated grating using 248nm DUV lithography

Figure 3.16: Retro-reflecting V-shaped facets. Standard flat facets are also drawn for illustration (dashed lines)

followed by lift-off. This process was carried out on cleaved dies. However, it could be carried out on a waferscale. This way, the metal layer perfectly covers the grating sidewall without covering the top of the slab waveguide. In order to obtain a good adhesion however, a few nanometer of titanium needs to be evaporated prior to gold evaporation. As this is a strongly absorbing metal, this has some negative impact on the grating reflectivity.

Figure 3.15(a) is a drawing of the situation after the evaporation of gold. The grating trench is filled with a 220nm thick layer of gold covering the sidewall. In a next step, the gold on top of the photoresist is removed by means of lift-off. Figure 3.15(b) is a top view picture of the grating after lift-off. The grating trench is partially filled with gold and the backside is covered.

3.6.4.4 Retro-reflecting V-shaped facets

Although a very high reflectivity can be obtained by metal coating, this technique has some drawbacks: it requires several extra processing steps (evaporation mask, evaporation and lift-off) and doing this on a waferscale is challenging. This can be avoided by changing the design (shape) of the grating facets. One way to do this is by making use of retro-reflecting V-shaped facet [35, 36].

In this case, each flat facet is replaced by a 90° corner reflector so that the light hits each grating facet at an angle of $\sim 45°$ which is greater than the angle needed for total internal reflection ($\sim 16°$). This is shown in figure 3.16.

In theory, a very high diffraction efficiency is possible since total inter-

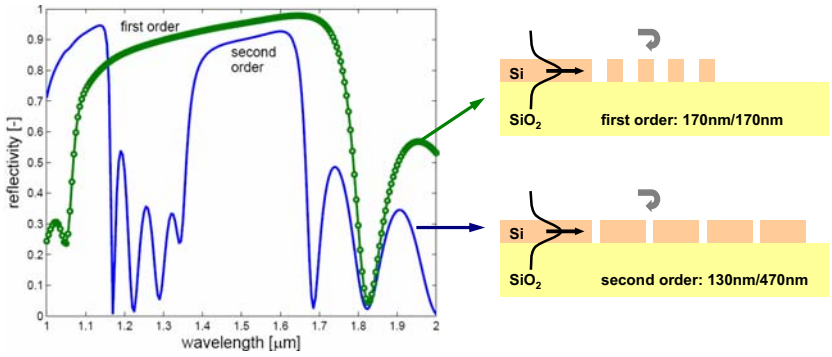


Figure 3.17: Reflectivity of 4.5 period first- and second order DBR-type facets. First order DBRs consist of 170nm wide trenches in between 170nm wide un-etched regions, second order DBRs consist of 130nm wide trenches in between 470nm wide un-etched regions

nal reflection takes place (twice) to retro-reflect incident light rays. However, because this requires two reflections per grating facet and the number of corners increases, the losses due to grating imperfections (roughness, non-verticality, corner rounding) will also increase. Moreover, some design freedom is lost due to the fact that these facets are retro-reflecting. As a consequence, it is no longer possible to individually blaze each facet in order to maximize the diffraction efficiency in one direction and the peak diffraction efficiency will be reached at the input waveguide.

3.6.4.5 Distributed Bragg Reflector type facets

To be able to individually blaze each facet without the need for additional processing steps, we developed a new technique. We replaced each flat facet by a distributed Bragg reflector (DBR)-type facet. Figure 3.17 shows the power reflectivity of two DBR designs as a function of wavelength (calculated using eigenmode expansion). These DBRs are deeply etched and have 4.5 periods. First order DBRs with a period of 340nm and a fill factor of 50% have a reflectivity above 80% over a very broad wavelength range (600nm) around 1.55μm. However, in view of fabrication feasibility using 248nm deep-UV lithography for first generation devices, we also designed second order DBRs. The optimum period of these reflectors is 600nm with a 130nm wide deeply etched trench and 470nm wide un-etched regions. Second order DBRs have a reflectivity of $> 80\%$ for wavelengths in the range of 1.45-1.65μm (figure 3.17). Although the bandwidth of these se-

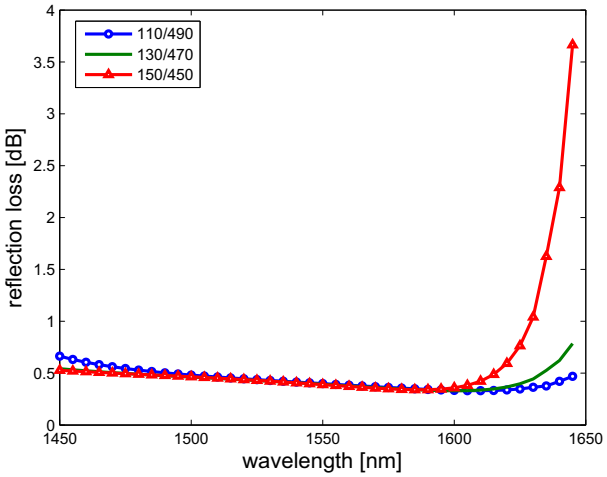


Figure 3.18: Simulation results of the reflection loss of a 4-period DBR-type facet. The period is 600nm and the trench width varies from 110nm to 150nm, the un-etched part from 490nm to 450nm. Perfectly vertical sidewalls are supposed

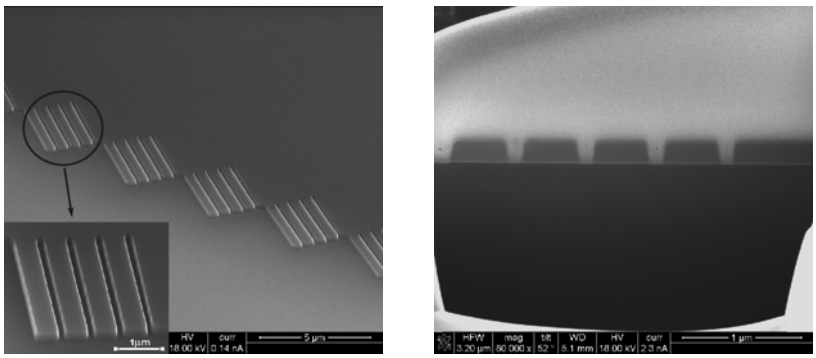
cond order gratings is narrower in comparison to first order gratings, it is broad enough for most applications as it spans of full free spectral range of a 10^{th} order PCG which is about 115nm. Figure 3.19(a) and 3.19(b) are two SEM pictures of fabricated second order DBR-type grating facets.

Figure 3.18 plots the reflection loss of a DBR facet consisting of four 600nm periods and vertical sidewalls. When using a trench width of 130nm, the reflection loss is below 0.5dB in the entire 1.5-1.6μm wavelength range. These facets are very tolerant of fabrication errors. A 15% trench width deviation does not result in a higher loss for wavelengths from 1.5μm up to 1.6μm.

To conclude, we can remark that the DBRs we presented here are deeply etched. Shallowly etched DBRs (70nm deep) could also be a envisioned but in order to obtain a high reflectivity, more periods will be needed. This will result in a smaller bandwidth making it impossible to obtain a high reflectivity in the 1.5-1.6μm wavelength range.

3.7 Experimental results

A large number of PCG demultiplexers were fabricated during this work with varying design parameters but also with different fabrication technolo-



(a) Perspective (b) Cross-section

Figure 3.19: SEM pictures of distributed Bragg Reflector facets

gies: 248nm DUV lithography for first generation devices and 193nm DUV lithography for later generations. We will give an overview of most notable devices in chronological order.

The first generation devices were fabricated using 248nm DUV lithography in the PICSOI7 processing run. The design was based on the standard Rowland configuration without corrections for aberrations. These were the first PCG demultiplexers ever fabricated on a nanophotonic SOI platform making this processing run a proof of principle experiment. We obtained good results with four channel coarse wavelength demultiplexers in terms of efficiency and crosstalk. These results proved that the nanophotonic SOI platform offers advantages for the fabrication of these PCG demultiplexers as compared with other material systems. The main advantages are first, the possibility to make compact devices using CMOS processing technology, second, the relaxed tolerance on grating verticality and third, the thin slab region which only supports one guided TE and TM mode. These results were also published [6, 37]

For the second generation, we focused on decreasing the on-chip loss and demonstrating demultiplexers with a smaller channel spacing and a larger number of wavelength channels. This was the PICSOI10 processing run in which some devices were fabricated using 248nm DUV lithography but also for the first time 193nm DUV lithography was used. To increase the reflectivity of the grating, we replaced the standard flat grating facets with gold coated facets, retro-reflecting V-shaped facets and DBR-type facets. Thanks to 193nm DUV lithography, the grating could be fabricated more accurate resulting in a further decrease of the insertion loss. Also, for the first time, the PCGs were corrected for aberrations by stigmatization (one

	Fabrication	Design	Goal
Generation 1	248nm DUV	flat facets and standard Rowland	proof of principle experiment
Generation 2	248nm DUV and 193nm DUV	high reflective facets and stigmatization	decrease on-chip loss, higher resolution
Generation 3	193nm DUV	high reflective facets and stigmatization	cascaded filters, polarization diversity, fiber Bragg interrogators, FTTH demux

Table 3.2: Overview of different generations of PCG demultiplexers

stigmatic wavelength). This resulted in the fabrication of 30-channel spectrometers with a channel spacing of 400GHz (3.2nm) and a low insertion loss and crosstalk. Results on the increased grating reflectivity and the 30-channel spectrometer were also published. [38, 39]

In the third generation PCGs (PICSOI12, PICSOI15, PICSOI17 and LETI02), we tried to increase the channel isolation and crosstalk by fabrication devices with two stigmatic (i.e. aberration-free) wavelengths. However, no major improvement in the transmission spectrum was noticed. Also, more complex devices to demonstrate polarization independent operation, fiber Bragg sensor interrogators, fiber-to-the-home (FTTH) demultiplexers and cascaded filters were designed. Table 3.2 summarizes the three PCG generations. These results are described below in detail.

3.7.1 First generation

As mentioned before, the first generation devices served as the proof of principle experiment. These devices were fabricated using 248nm DUV lithography and the design is according to the standard Rowland configuration. This means that the projection of the center points of the grating facets are equidistant.

3.7.1.1 4-channel coarse wavelength demultiplexer

One of the first devices we designed and fabricated was a 1×4 PCG demultiplexer with a 20nm channel spacing around a central wavelength of 1.55μm resulting in central channel wavelengths of 1.52, 1.54, 1.56 and

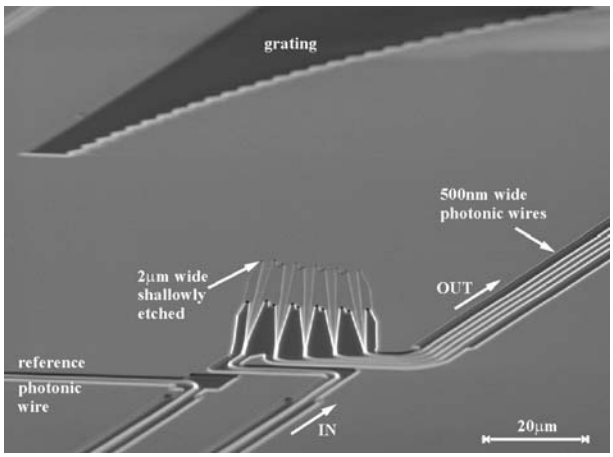


Figure 3.20: SEM picture of a fabricated 1×4 PCG demultiplexer

1.58μm. A SEM picture of the fabricated device is shown in figure 3.20. It has a footprint of only 280μm×150μm, including photonic wire access waveguides.

As described in paragraph 3.3, the design process starts with determining the order of diffraction. The operational range of the coarse wavelength demultiplexer is 4×20nm. This means that the order of diffraction, m should be chosen large enough so that the FSR is larger than 80nm. In this design, it is chosen to be $m = 10$. According to equation 3.9, this results in a FSR of 115nm. The incident and diffracted angles are chosen to be $\theta_i = 41^\circ$ and $\theta_d = 37^\circ$. From equation 3.1, we can calculate the grating period $d = 4.35\mu$m. The 2μm wide shallowly etched output waveguides are spaced 5μm apart on the Rowland circle. This results in a required linear dispersion of 0.25μm/nm. The Rowland circle radius R and hence the size of the device can then be calculated from equation 3.8, which in this design results in $R = 94\mu$m. The PCG has 31 grating facets that are individually blazed to maximize their reflection at the middle of the 4 output waveguides in order to get a symmetrical channel response. The number of grating facets should be chosen large enough so to capture most of the input beam. Using equation 3.10, we can calculate the modulus of the incident electric field on the center points of each grating facet. This is shown in figure 3.21. Table 3.3 summarizes the design parameters.

Figure 3.22(a) shows the simulated transmission spectrum. For these simulations, the reflectivity of the grating, η is set to 1. The non-uniformity across the channels is 0.9dB and the insertion loss for the two central channels is 0.7dB (without taking into account grating reflection loss).

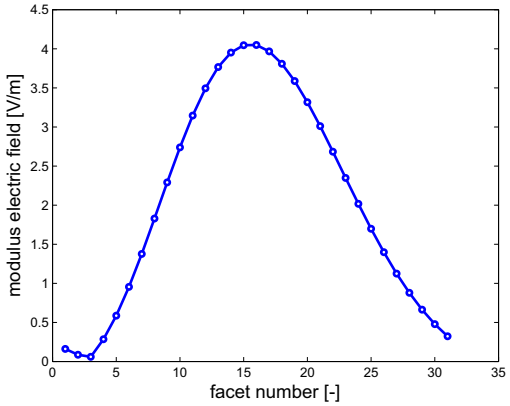
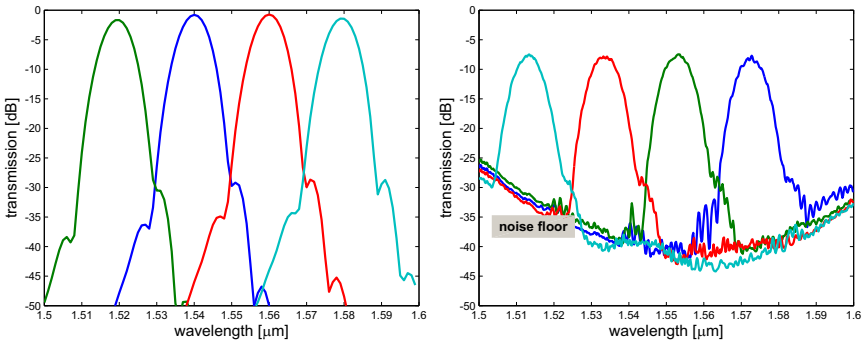


Figure 3.21: Modulus of the incident electric field for $\lambda = 1.55\mu$m

4-channel coarse wavelength demux			
λ_0	1.55μm	FSR	115nm
$\Delta\lambda$	20nm	waveguide spacing	5μm
θ_i	41°	waveguide width	2μm
θ_d	37°	facet number	31
d	4.35μm	LD	250
m	10	R	94μm

Table 3.3: Summary of design parameters 1



(a) Simulation (b) Measurement

Figure 3.22: Transmission spectrum of the 4-channel coarse wavelength demultiplexer

The measured transmission spectrum (TE polarization) is shown in figure 3.22(b). This transmission spectrum is normalized to a reference photonic wire waveguide. The on-chip loss for the central channels is 7.5dB with a crosstalk better than -30dB. The loss variation over the channels is 0.6dB. Measurement results are slightly disturbed by the high noise floor of the measurement setup: the high noise floor at the edges of the operational range is due to the limited bandwidth of the fiber couplers resulting in low absolute transmission at these wavelengths. As compared to simulation results, there is a shift in the transmission spectrum of 6nm towards shorter wavelengths, which can be attributed to a slightly smaller n_{eff} as compared to the value used in the simulations.

The on-chip loss of 7.5dB results from several factors. The largest contribution, 4.6dB is caused by Fresnel reflection loss at the grating since no measures were taken to enhance the reflectivity of the grating facets. A second contribution (0.3dB) is due to the non-verticality (10.5°) of the grating facets as explained in paragraph 3.6.4.2. This causes coupling loss between the incident fundamental slab mode and the reflected fundamental slab mode. This brings the total grating reflection loss at 4.9dB. A third contribution, which is inherent to the design, is the diffraction loss of 0.7dB for the central channels. This means that 1.9dB of loss is caused by other effects, mainly grating profile imperfections like facet corner rounding and surface roughness. This low value, as compared to previous reported SOI PCGs [14, 40], is partially due to the fact that the grating only needs to be etched 220nm deep, making it possible to obtain a high quality grating profile making use of standard dry etching techniques as can be seen in figure

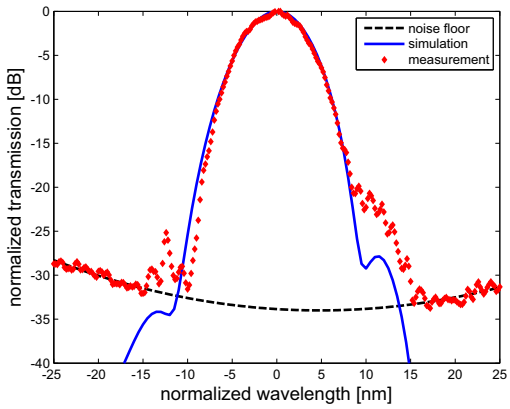


Figure 3.23: Comparison between measurement and simulation for channel 3 ($\lambda_0 = 1560nm$)

3.11.

To prove the validity of the simulation method based on scalar diffraction theory, we compared the measured and simulated transmission of the third channel as shown in figure 3.23. The two spectra are normalized to 0dB transmission and the measured spectrum is shifted over 6nm so that the transmission maxima coincide. The spectral shapes around the central channel wavelength overlap almost perfectly. As explained before, comparison of the side lobes is harder because of the high noise floor of the measurement setup. However, we clearly see two side lobe structures at -12nm and +12nm both in the measured and simulated transmission. The measured side lobe level is 10dB higher as compared to simulations. This discrepancy originates mainly from small fabrication imperfections and will be discussed in more detail in paragraph 3.8. Side lobe structures like these limit the crosstalk value of the device, which is still better than -30dB.

3.7.1.2 Other first generation designs

We also designed and fabricated devices with a smaller channel spacing of 3.2nm. However, these devices suffered from high crosstalk values and high side lobe levels of about -10 to -15dB. This is mainly due to the fact that the design of the first generation devices is based on the standard Rowland configuration. In this case, the position of the grating facets is not corrected to reduce residual aberrations as discussed in paragraph 3.6.3. Demultiplexers with a 3.2nm channel spacing in the standard Rowland configuration have already an intrinsic side lobe level as high as -20dB. Due to

various fabrication imperfections, these side lobes increase another 5-10dB to unacceptable values. Simulation results of this device will be presented in the next paragraph.

3.7.1.3 Conclusions

By fabricating a 1×4 demultiplexer with a record-small footprint and good performances in terms of excess loss and crosstalk, we proved that the nanophotonic SOI platform offers many advantages for the fabrication of PCG demultiplexers as compared with other material systems. Especially the strongly relaxed fabrication tolerance on grating verticality are striking. Also, by comparing these measurement results with our simulation results, we showed that scalar diffraction theory is an adequate tool for simulating these filters. Also, our Matlab/Python code both for simulation and mask-design will be very useful for further device optimization and fabrication.

On the other hand, we also identified some issues which need to be solved in next generation devices. First of all, the on-chip loss of $>$7dB is very high and unacceptable for commercial applications. As indicated, the largest part of this loss is caused by the limited reflection of the grating and could be avoided by changing the grating design. Secondly, larger filters with an increased linear dispersion and a smaller channel spacing suffer from relatively high side lobe levels.

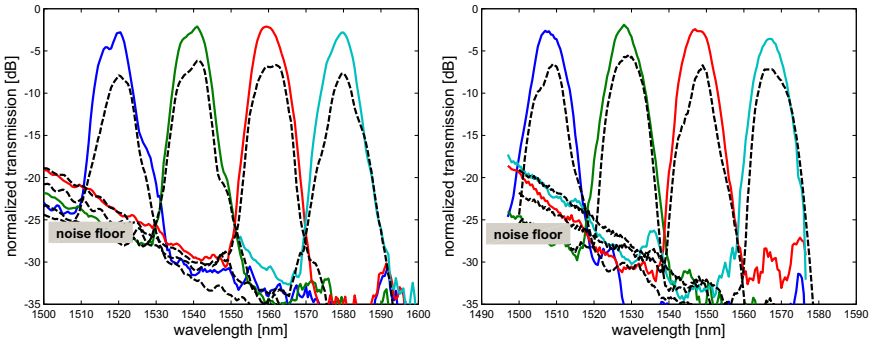
3.7.2 Second generation

The goal of the second generation devices was twofold: to increase the grating reflectivity and to demonstrate filters with a smaller channel spacing (3.2nm). As discussed in paragraph 3.6.3, simulation results pointed out that side lobe levels can be decreased by stigmatization. All second generation filter are designed with one stigmatic wavelength, i.e. the central wavelength of the filter.

3.7.2.1 4-channel coarse wavelength demultiplexer

In order to reduce the large on-chip loss of the 4×20nm PCG with standard flat facets, we coated the backside of the grating with gold as explained in paragraph 3.6.4.3. Figure 3.24(a) plots the on-chip transmission spectrum of two identical PCGs, one with uncoated flat facets, and the other one with Au coated flat facets. These devices were fabricated with 248nm DUV lithography and have one stigmatic wavelength.

The on-chip loss of the central channels of the uncoated device is $\sim 6.7dB$. The largest contribution of 4.9dB is caused by the reflection loss at



(a) PCGs fabricated with 248nm DUV lithography. Devices with uncoated (dashed line) and Au coated facets are compared

(b) PCGs fabricated 193nm DUV lithography. Devices with flat (dashed line) and DBR-type facets are compared

Figure 3.24: On-chip transmission spectrum of 4-channel PCG demultiplexers with high reflectivity grating facets

the grating facets as mentioned earlier (taking into account a 10.5° sidewall non-verticality). Other contributions are diffraction loss of 0.5dB (0.2dB lower than first generation due to stigmatization) and excess loss due to grating profile imperfections, which adds 1.3dB. This is also a reduction as compared to the first generation device due to some small device layout optimizations. The insertion loss of the Au coated device is 4.5dB lower resulting in an insertion loss of only 2.2dB for the central channels. It's important to notice that the reflectivity enhancement is rather constant over the operational wavelength range of the device. This means that the Fresnel reflection loss is reduced from 4.6dB down to 0.1dB.

Figure 3.24(b) shows the transmission spectrum of the same device, but now fabricated with 193nm DUV-lithography. The spectra of PCGs with flat facets and DBR-type facets are compared. The loss of the central channels of the flat facet design is $\sim$6.3dB. Again, 4.9dB is caused by reflection loss, 0.5dB by diffraction loss. This means that 0.9dB is caused by grating profile imperfections. This value is slightly better as compared with the PCG fabricated with 248nm DUV lithography. This means that a more perfect grating profile is obtained using 193nm DUV lithography.

The minimal insertion loss of the device with DBR-type facets is 1.9dB, with a non-uniformity of 1.7dB across the four channels (2.6dB-1.9dB-2.4dB-3.6dB). The insertion loss is 3.9dB better on average as compared with the flat facet device (figure 3.24(b)). This means that the average reflection loss at the facets decreases from 4.9dB down to 1.0dB by replacing the facets with second order DBRs. This value is slightly higher

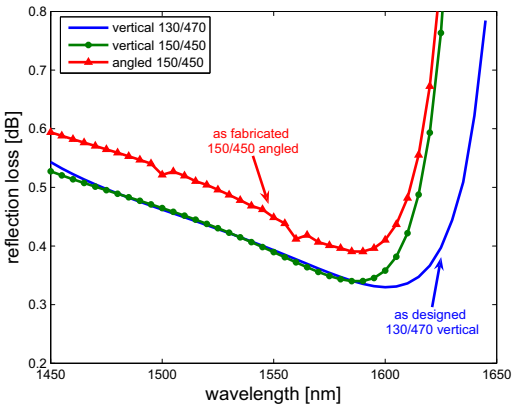


Figure 3.25: Simulated reflection loss of a 4.5-period DBR-type facet. The ideal DBR (470nm/130nm and vertical sidewalls) is compared with the fabricated DBR (450nm/150nm and 10° non-verticality for the isolated sidewall, 5° for the non-isolated sidewalls)

	flat facets	**DBR facets**
grating reflection loss	4.9dB	1dB
diffraction loss	0.5dB	0.5dB
excess loss	0.9dB	0.9dB
total on-chip loss	**∼6.3dB**	**∼2.4dB**

Table 3.4: Different contributions to the total on-chip loss of a 4×20nm PCG fabricated using 193nm DUV lithography

as compared with the simulation results shown in figure 3.18 which predict an average facet loss of 0.4dB in the 1.5-1.6μm range. However, these simulations do not take into account fabrication imperfections like grating non-verticality and trench width deviation of the DBRs. The cross-section (3.19(b)) revealed a trench width of 150nm whereas a trench width of 130nm was expected. Also, there is a deviation from verticality of $\sim 5^{\circ}$ for the non-isolated sidewalls and $\sim 10^{\circ}$ for the isolated sidewall. These simulation results are shown in figure 3.25 and predict an increase of only 0.1dB in the 1.5-1.6μm range. This means that the somewhat higher than expected facet reflection loss is due to other DBR imperfections like roughness and trench-width non-uniformity.

The crosstalk of the device does not seem to be significantly deteriorated by the use of the DBR-type facets and is better than -25dB. However, it is difficult to draw conclusions concerning crosstalk values due to the high noise floor of the measurement setup.

Table 3.4 summarizes the different contributions to the central channel losses of these two PCGs fabricated with 193 DUV lithography (flat facets vs. DBR facets)

3.7.2.2 30-channel dense wavelength demultiplexer

For near infrared spectroscopy applications (biodiesel/diesel sensing, glucose monitoring,...) a higher resolution is necessary. For this purpose, we designed a 1×30 demultiplexer with a 400GHz (3.2nm) channel spacing. A microscope picture is shown in figure 3.26.

This design is similar to the design of the coarse wavelength demultiplexer but as the Rowland radius is inversely proportional with the channel spacing (for a given waveguide spacing), the size of this dense demultiplexer is much larger. Again, the 2μm wide waveguides are positioned along the Rowland circle with a 5μm pitch. To obtain a 3.2nm channel spacing, the required linear dispersion is 1.56μm/nm. The Rowland circle has a radius of 554μm and the curved grating sits on an 1108μm radius

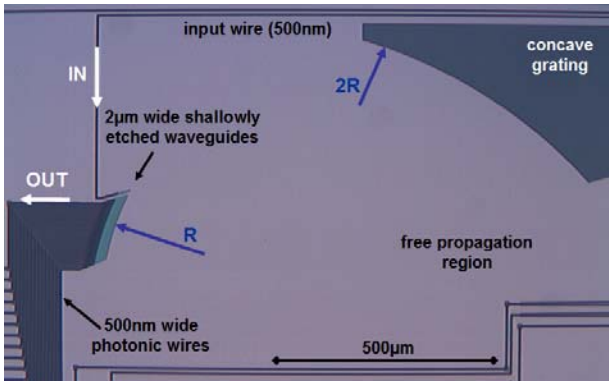


Figure 3.26: Microscope picture of a 1×30 PCG demultiplexer

30-channel dense wavelength demux			
λ_0	1.55μm	FSR	115nm
$\Delta\lambda$	3.2nm	waveguide spacing	5μm
θ_i	43°	waveguide width	2μm
θ_d	38.5°	facet number	141
d	4.2μm	LD	1562.5
m	10	R	554μm

Table 3.5: Summary of design parameters 2

circle. The order of diffraction is 10, the angle of incidence, $\theta_i = 43°$ and $\theta_d = 38.5°$. The 141 grating facets are positioned along the grating curve using the 1-stigmatic point approach. Again, this point is situated at the center of the output waveguides with a corresponding stigmatic wavelength of 1.55μm. A summary of the design parameters is shown in table 3.5

The simulated transmission spectrum is plotted in figure 3.27(a) and 3.27(b). Again, a perfectly reflecting grating is supposed. In the standard Rowland configuration, the minimum diffraction loss is 2.2dB and the side lobe level is -20dB. As mentioned earlier, the crosstalk of these fabricated devices (first generation) was unacceptably high. A significant improvement of diffraction loss and side lobe level can be obtained with a one-stigmatic point approach: the (simulated) minimum diffraction loss decreases to 0.6dB and the side lobe level decreases to -50dB.

The measured transmission spectrum (normalized to a reference photonic wire waveguide) of the 30-channel demultiplexer with DBR-type grating facets is shown in figure 3.27. The on-chip loss varies from 3dB for the central channels down to 6-7dB for the channels at the edge. The near-

channel crosstalk varies between -22dB and -15dB. The higher loss for the long wavelength channels as compared to the short wavelength channels is due to the fill factor of the DBRs which is slightly smaller then the designed value (too broad trenches). This results in a blue shift of the DBR reflection band as shown in figure 3.18 and 3.25.

3.7.2.3 Conclusions

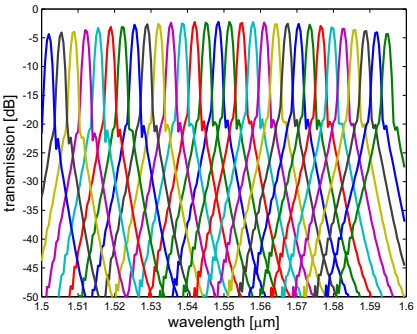
We demonstrated that it is possible to decrease the on-chip loss down to 1.9dB by replacing each flat grating facet with a DBR-type facet. This approach has important advantages as compared to retro-reflecting and metal coated grating facets in terms of performance, design freedom and processing complexity. There is no need for additional processing steps which could increase the cost of commercial products.

By stigmatization (one stigmatic wavelength), we were able to decrease the side lobe level of filters with 3.2nm channel spacing down to -22dB. If we compare the coarse ($\Delta\lambda = 20nm$) and the denser ($\Delta\lambda = 3.2nm$) wavelength filters, we can also conclude that side lobe levels increase with decreasing channel spacing. This is because the Rowland radius of a PCG is inversely proportional to the channel spacing: for narrower wavelength channels, the spatial focusing resolution of the device needs to be increased, which requires a longer slab region. Devices with longer slab regions are more sensitive to variations in the thickness of this slab. This will be discussed in paragraph 3.8.

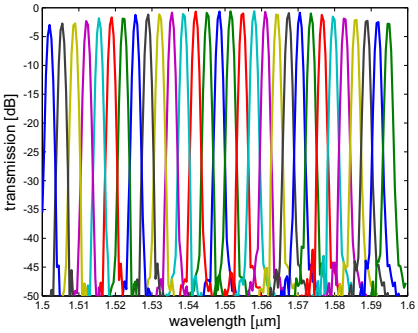
3.7.3 Third generation

For the third generation devices, we fabricated devices with a channel spacing of 3.2nm and two stigmatic wavelengths in order to try to decrease the side lobe level. However, we did not observe any significant improvement and as a consequence, these results will not be covered in this chapter.

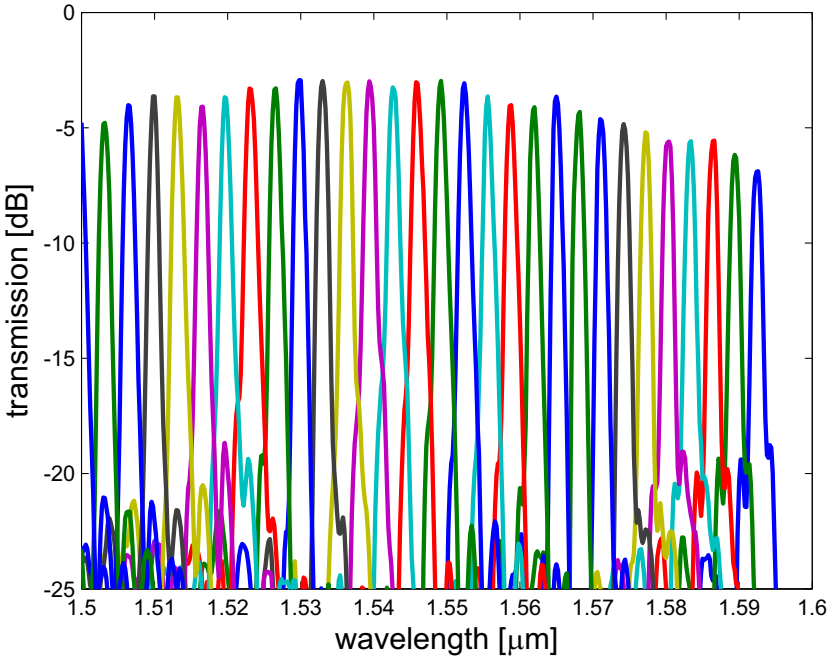
Another problem we tackled here was the polarization sensitivity: by making use of a polarization diversity approach, we will show that it is possible to make polarization independent PCG filters. We also designed some application-specific filters: fiber Bragg interrogators and fiber-to-the-home (FTTH) demultiplexers. For spectroscopy applications, a high resolution in combination with a large operation wavelength range is needed. As the performance of PCG demultiplexers has the tendency to decrease for increasing resolution, we tried to solve this problem by fabricating cascaded filters. The idea is to make use of a PCG to perform coarse wavelength filtering and another filter (ring resonators, AWGs, ...) to perform denser



(a) Simulation Rowland configuration

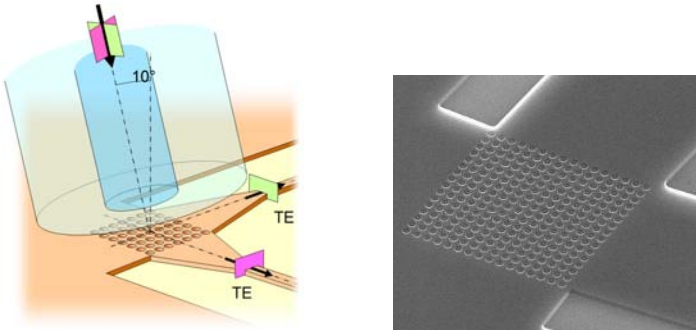


(b) Simulation one stigmatic point



(c) Measurement

Figure 3.27: Transmission of the 30-channel PCG demultiplexer



(a) Drawing (b) SEM picture

Figure 3.28: 2D grating coupler

filtering.

3.7.3.1 Polarization diversity

When light is generated on chip or more general, for transmitter PICs, the polarization of the light is known and the optical circuit (filters, waveguides, photodetectors, ...) can be designed for one polarization only. For most other applications however, like spectrometers, WDM-receivers ... , the polarization of the incoming light (from fiber or free-space) is variable and unknown. In this case it is necessary that the optical circuit operates independent of the polarization.

Nanophotonic SOI devices are strongly polarization dependent due to their wavelength scale critical dimensions and the high refractive index contrast of the material system. That's why in practice, these devices are optimized for one single polarization, being either TE or TM. If we take a PCG as an example, the effective indices of refraction of the TE and TM-polarized slab modes are widely different: 2.83 versus 1.89 respectively at a wavelength of 1.55μm. As a consequence, two different images will be formed along the Rowland circle, each corresponding to a differently polarized slab mode. This results in a wavelength shift between the TE and TM spectrum and can be calculated using the grating equation (equation 3.1).

One approach to overcome this problem is to insert a polarization compensator in the slab region of the PCG [41]. However, this is far from trivial in terms of fabrication tolerances and device performance. A different approach is to implement a polarization diversity approach [42]. In this case, the random polarization of the incoming light is split (on-chip) into its two orthogonal polarization states. One polarization is then rotated by

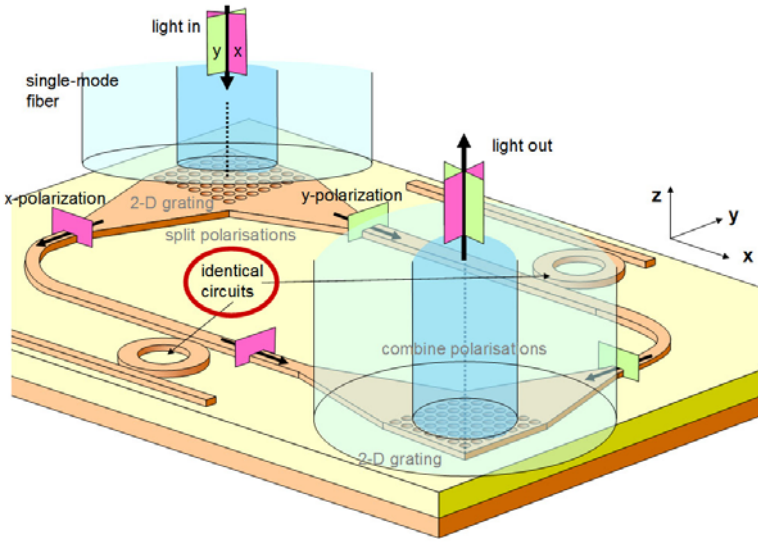


Figure 3.29: Polarization diversity approach using 2D grating coupler

90°, resulting in two channels with identical polarization. Both arms feed an identical polarization sensitive device and at the output, one polarization is rotated by 90°. Finally, both orthogonal polarizations are recombined. By making use of 2D fiber couplers, the necessary polarization splitters and rotators can be avoided as can be seen in figure 3.28. In this case, the orthogonal polarization components of the incoming light are coupled into two near orthogonal waveguides. In these waveguides, the polarization is identical (TE) [43]. This way, a 2D fiber coupler combines the functionality of a standard fiber coupler, a polarization splitter and a 90° polarization rotator in one arm.

The principle of polarization diversity using 2D fiber couplers is shown in figure 3.29. The working principle is explained above. This approach has already been successfully demonstrated by our group in combination with AWG filters [44] and here, it is demonstrated in combination with PCGs. Figure 3.30 is a top view picture of a 4-channel coarse wavelength demultiplexer in a polarization diversity configuration. The PCG is identical as the one described in paragraph 3.7.1.1. On the left hand side, two input 2D fiber couplers are visible. One input connects to reference waveguides and the other fiber coupler connects with the input of two PCGs. On the right hand side, 4 output fiber couplers connect to the four PCG channels and the fifth is the output coupler of the reference waveguide.

In order to obtain polarization independent operation, the two PCGs

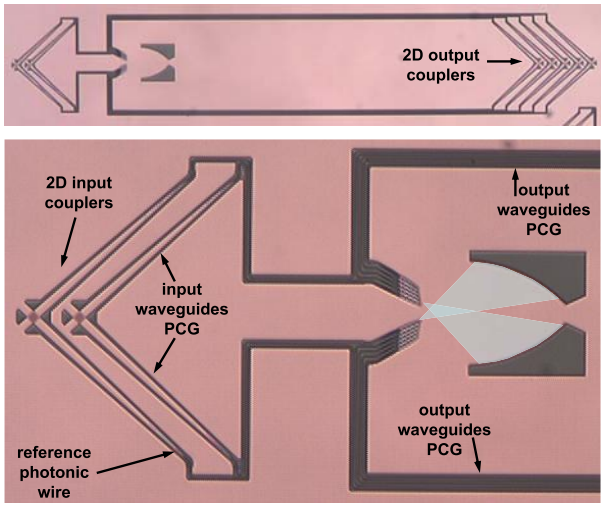
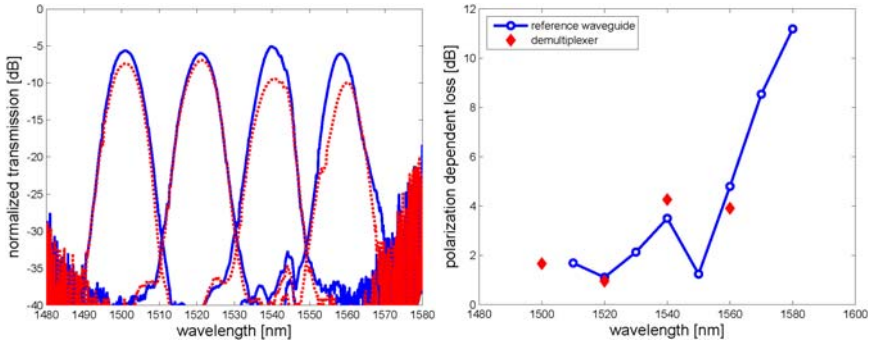


Figure 3.30: 4-channel PCG in a polarization diversity configuration

have to function identically. Otherwise, there will be a polarization dependent loss (PDL) and wavelength shift. An AWG can operate in a bidirectional way as demonstrated in [44] requiring only one device in a polarization diversity schema. Because the layout of PCG is not symmetric, an identical bidirectional operation is almost impossible to realize and two identical PCGs have to be fabricated in each arm of the 2D fiber couplers. In a high contrast system like SOI, this requires very accurate fabrication. As can be seen in figure 3.30, the two PCGs share the same free propagation region. This is advantageous in terms of compactness but more important, by fabricating the PCGs as close to each other as possible, we avoid the variations of the waveguide layer thickness over the wafer.

To measure the spectrum of the demultiplexer for different polarizations, we used an SLED light source connected to a fiber optic polarizer. Using polarization wheels, an arbitrary polarization can be selected at the end of the input fiber. The position of the fibers on top of the fiber couplers was optimized in order to minimize the PDL. Figure 3.31(a) plots the measured normalized transmission spectrum of the 4-channel PCG. For each wavelength channel, the polarization was changed in order to obtain maximum and minimum transmission and these spectra were recorded. The polarization dependent wavelength shift is negligible for three channels. The PDL ranges from 1dB for channel number two up to 4dB for channel 3 and 4, which is too high for practical applications. This is also plotted in figure 3.31(b), together with the PDL of the reference waveguide. The minimum



(a) Transmission spectrum of the 4-channel demux. The polarization was changed to obtain both maximum (blue) and minimum (red) transmission

(b) PDL versus wavelength

Figure 3.31: Polarization diversity measurements

PDL of the reference waveguide ($\sim$1dB) is only obtained in a narrow wavelength window. This limitation has already been noticed and described in previous work [45] and optimization of the 2D fiber couplers is needed to broaden that wavelength window. The minimum PDL is somewhat higher than expected ($\sim\ 0.4dB$) and might be due to fabrication imperfections and/or fiber misalignment.

As can be seen, the PDL of the demultiplexer and the reference waveguide are similar. Although these values are too high for practical applications, we can conclude that the PDL of the PCG is similar with the PDL of the reference waveguide. This validates the design of intersecting PCGs and further optimization of the 2D fiber couplers is needed to obtain a low PDL over the entire 100nm wavelength range.

3.7.3.2 Fiber Bragg interrogator

A fiber Bragg grating (FBG) is a type of distributed Bragg reflector constructed in a short segment of optical fiber that reflects particular wavelengths (Bragg wavelength) of light and transmits all others. This is achieved by adding a periodic variation to the refractive index of the fiber core, which generates a wavelength specific dielectric mirror (figure 3.32). The Bragg wavelength (λ_B) is sensitive to both temperature and strain of the fiber Bragg grating. This means that fiber Bragg gratings can be used as sensing elements for strain, temperature, but also acceleration and pressure. FBGs have numerous significant advantages over more conventional elec-

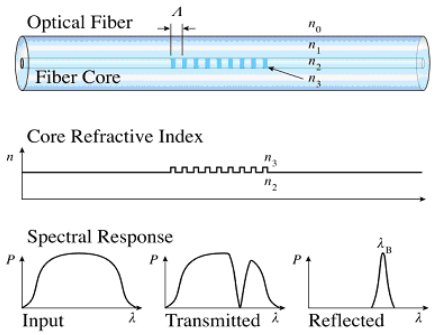


Figure 3.32: A Fiber Bragg Grating, with refractive index profile and spectral response [46]

trical sensor technologies. One of these advantages is multiplexing: many tens of FBGs can be written into one optical fiber and hundreds of fibers can be connected to measure temperature or strain in different locations. They are typically used for the health monitoring of aerospace and civil engineering structures.

To measure and monitor the wavelength shifts of FBG sensors, fiber Bragg grating interrogation systems are used. The field interrogations of multi FBG sensors are still a big challenge due to the lack of portable, robust, high performance multi sensor interrogation devices. Optical spectrum analyzers (OSA) are currently the most popular choice for the interrogation of optical fiber Bragg grating sensors. Though they offer a large measurement range, their measurement resolution only reaches 10pm. In addition they are bench top equipment, lab-oriented and not suitable for field applications. In recent years, several types of micro spectrometers have been developed and became commercially available. These spectrometers however are targeting a large wavelength range and their typical measurement resolution (1nm) is too limited for practical interrogation devices, which require a resolution of ($\sim$1pm) [47].

Different approaches have been proposed and demonstrated to overcome the limited resolution of commercially available micro spectrometers. A first approach is based on shifting the transmission spectrum of a spectrometer (PCG, AWG) by thermal tuning. Xiao and coworkers obtained a resolution better than 1pm by using a thermally tuned InP PCG demultiplexer with a channel spacing of 1.6nm [47]. In a second approach, the demultiplexer is designed in such a way that the Bragg grating spans several demultiplexer channels. The ratio of the signal strengths in each channel

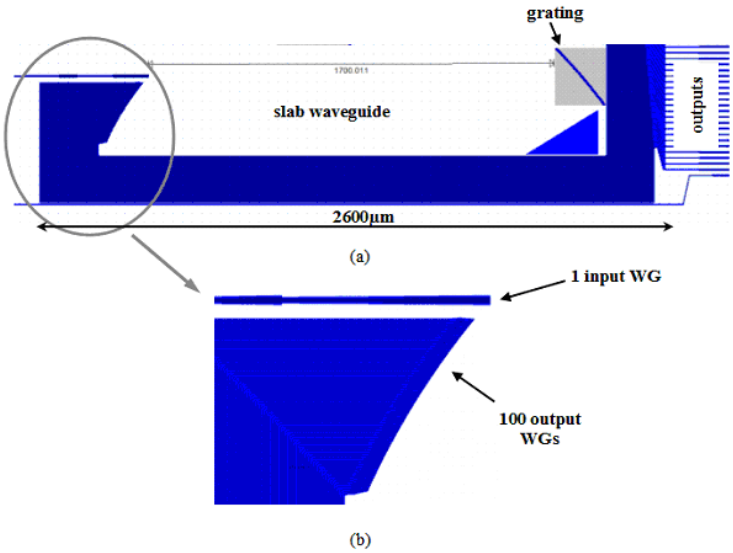


Figure 3.33: (a) Mask layout of the fiber Bragg interrogator sensor and (b), detailed view on the input and output waveguide apertures

are used to compute the actual wavelength (centroid detection) resulting in an increased resolution and accuracy. Again, sub-pm resolution has been demonstrated using spectrometers (AWGs) with a nanometer channel spacing [48–50].

We fabricated a prototype FBG interrogator based on this last approach. We designed a grating demultiplexer with 100 wavelength channels and a channel spacing of 1nm. The device spans the wavelength range from 1.5μm to 1.6μm. The mask layout of the device is show in figure 3.33. Figure 3.33(a) is a top view picture of the interrogator. Only a part of the waveguide fan-out (100$\times$25μm) is shown. The size of the device is $\sim$3mm$\times$1mm. Figure 3.33(b) is a detailed picture of the waveguide apertures. The input waveguide is 10μm wide and the output waveguides are 1μm wide. The grating has 71 facets. The main difference between this design and the previously discussed PCG designs is the size of the waveguide apertures. By making the input waveguide considerably wider than the output waveguides (10μm vs. 1μm), the diffracted beam will spread out over several output waveguides at a certain wavelength. As a consequence of that, the transmission spectrum of the interrogator will consists of 100 strongly overlapping channels. The design parameters are shown in table 3.6. The design has two stigmatic channels (channel 26 and 75) with

100-channel FBG interrogator			
λ_0	1.55μm	FSR	115nm
$\Delta\lambda$	1nm	waveguide spacing	3μm
θ_i	40°	waveguide width	IN:10μm OUT:1μm
θ_d	35.5°	facet number	71
d	4.47μm	LD	3000
m	10	R	1180μm

Table 3.6: Summary of design parameters 3

1525.1nm and 1574.1nm being the corresponding wavelengths.

Figure 3.34 shows the transmission spectrum. Not all the channels are shown on these graphs (four arbitrary wavelength regions are represented). The power in each channel is expressed in absolute values (dBm). The side lobe level is at -10dB to -15dB and for each wavelength, a signal (above the side lobe level) is detected in at least four different channels. By analyzing the power ratio in these channel, the position of a the Bragg wavelength can be determined with sub-nm resolution.

This device demonstrates the possibility of making very compact FBG interrogators based on silicon-on-insulator PCGs. In-depth characterization of these interrogators has to be carried out in the future to determine their wavelength accuracy, resolution and maybe more important, the impact of the relatively strong side lobes. Moreover, this devices also proves that we are able to "design on demand": we can fabricate PCGs with Gaussian shaped transmission channels and with an almost arbitrary channel spacing, channel overlap and channel bandwidth for many different applications.

3.7.3.3 FTTH transceiver

Current broadband services such as copper-based access technologies have reached there limits and the growing demand for bandwidth is driving the deployment of optical networks. Without a doubt, Fiber-To-The-Home (FTTH) is the most impressive technology for realizing very high bandwidths. Point-to-point FTTH optical access networks require large volume and low-cost optical transceivers, both at the subscriber and the central office side. From the perspective of the transceiver at the subscriber side, 1310nm is the upstream channel and 1490nm and 1550nm are the downstream channels for data and CATV. The passive optical part of a FTTH transceiver has to couple and demultiplex these three communication channels.

Figure 3.35 is a microscope picture of a nanophotonic SOI FTTH trans-

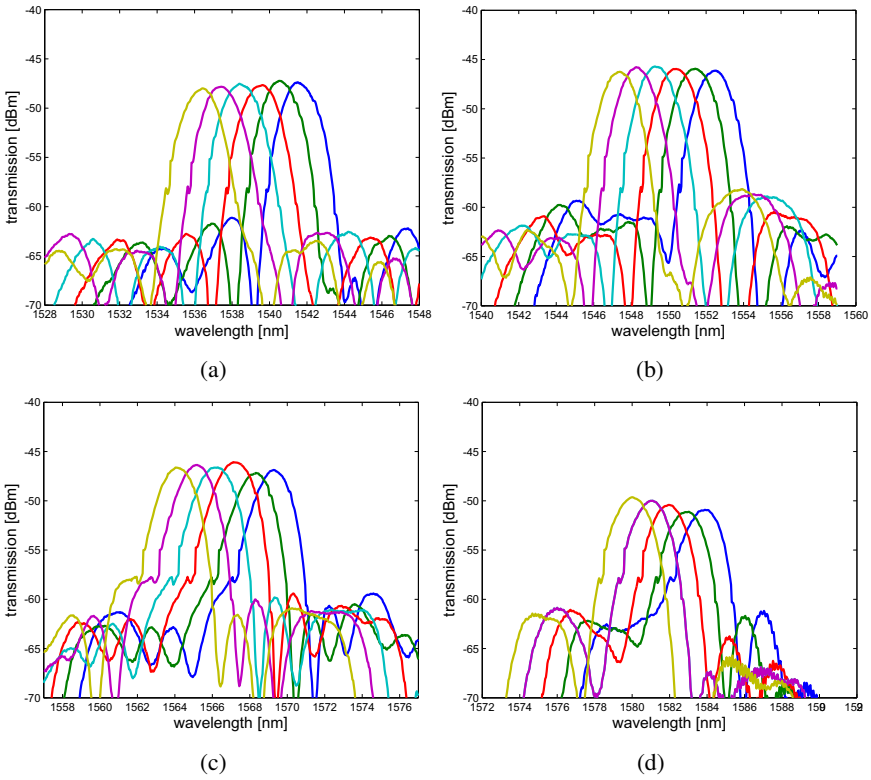


Figure 3.34: Transmission spectrum (not normalized) of a fiber Bragg interrogator (100×1nm)

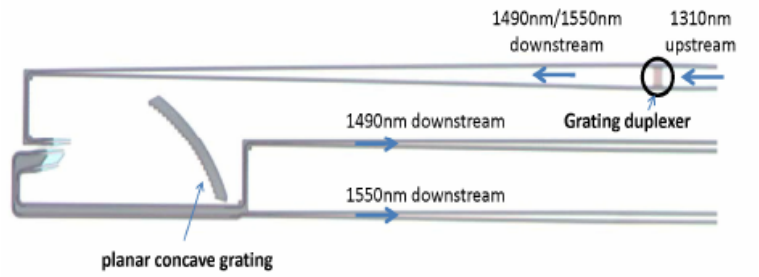


Figure 3.35: Microscope image of a grating duplexer in combination with a PCG for FTTH applications [51]

2-channel FTTH demux			
λ_0	1.52μm	FSR	120nm
$\Delta\lambda$	60nm	waveguide spacing	10μm
θ_i	41°	waveguide width	2μm
θ_d	35°	facet number	21
d	4.34μm	LD	167
m	10	R	67μm

Table 3.7: Summary of design parameters 4

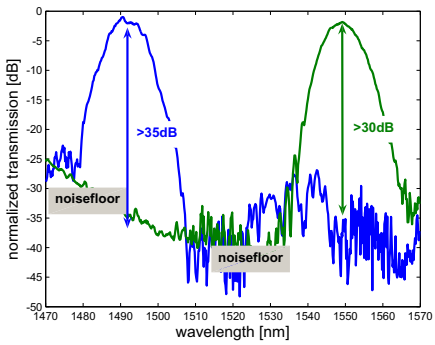


Figure 3.36: Transmission spectrum of a PCG demultiplexer for separating the 1490nm and 1550nm channels. The spectrum is normalized with respect to a reference photonic wire

ceiver. The design and the fabrication of this device has been done in our group in the framework of the PhD of D. Vermeulen and has been published in 2008 [51]. With a grating duplexer the light is coupled from the fiber into the chip and the 1310nm upstream channel is spatially separated from the downstream channels. With a PCG demultiplexer, the downstream channels 1490nm and 1550nm are split and the 1310nm wavelength channel is filtered to reduce the crosstalk levels.

The design parameters of the PCG are shown in table 3.7. It has a very compact footprint of $\sim 70 \times 70\mu m^2$. The crosstalk between the 1490nm and 1550nm wavelength channels is better than -35dB with on-chip loss of 5-8dB [51]. The high loss was due to the reflection loss at the flat grating facets. By replacing these with DBR-type facets, the on-chip loss could be reduced to 1-2dB. Figure 3.36 plots the measured on-chip transmission spectrum of this PCG demultiplexer with high reflective grating facets.

This FTTH demultiplexer shows that PCGs are a good choice for the fabrication of coarse wavelength filters. As the linear dispersion of these

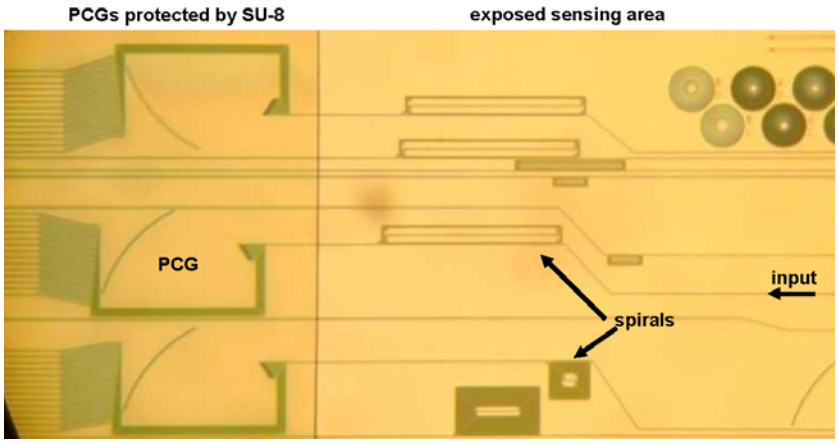


Figure 3.37: Top view of SOI chip for biodiesel sensing. The left part of the chip is protected by a layer of SU-8. The right part, the sensing area is exposed

coarse filters is limited, the device is very compact and this results in good channel isolation values.

3.7.3.4 Biodiesel sensor

In the framework of a master thesis, A. Casas Bedoya showed that these PCGs can also find application in near-infrared spectroscopy. By analyzing the spectral absorbance of biodiesel/diesel blends in the 1650nm wavelength range, it is possible to determine the exact blend level. This is important for automotive applications. The information can be used to adjust the engine management (ignition timing, injection ...) in real-time to optimize fuel consumption and engine performance [52].

For this purpose, a 14-channel PCG demultiplexer was designed around a central wavelength of 1650nm and with a channel spacing of 7nm. DBR-type grating facets were designed to have a high reflectivity in the 1.6-1.7μm wavelength range. The input of the PCG is connected to a centimeters long spiral waveguide which act as the 'sensing area': the evanescent tail of the light in the spiral waveguide feels the presence of the fuel mixture on top of it [52]. Depending on the blend level, the absorption is wavelength dependent and this can be measured using the PCG. Fabricated devices are shown in figure 3.37. On the most right part of the chip, we clearly see the sensing area with the different spiral waveguides. Some of these spirals are connected to the input of a PCG on the left of the chip to measure the

spectral absorption. To fuel has to be in close proximity with the spiral waveguides but we have to avoid that it influences the spectral characteristics of the PCGs. That's why during fabrication, a thick polymer layer (SU-8) is deposited on the chip to protect most of the chip-surface. This protective layer is locally removed above the sensing area. This causes the contrast difference between the left and right part of the chip. Measurement results of these devices can be found in the master thesis of A. Casas Bedoya [53].

3.7.3.5 Cascaded filters

The design and fabrication of cascaded filters (e.g. PCGs + ring resonators) in order to obtain dense wavelength filtering over a broad wavelength range was also part of third generation developments. These filters will be discussed in paragraph 3.9.

3.8 Performance and reproducibility

3.8.1 Introduction

In this paragraph, we will discuss the performance of the PCGs in terms of insertion loss, side lobe level and crosstalk. The insertion loss of our devices has already been discussed earlier, but here, we analyze the contribution of the excess loss. Excess loss, in contrast to diffraction loss and grating reflection loss is mainly caused by fabrication imperfections.

3.8.2 Insertion Loss

In paragraph 3.7.2, we demonstrated a 4×20nm PCG demultiplexer with a minimum on-chip loss of 1.9dB. This value is among the best ever reported for PCG demultiplexers and moreover, this is achieved without the need of metal-coating the backside of the grating. Historically, the commercial applications of PCGs have been hindered in part by their large on-chip losses in comparison with AWGs. If we compare our PCGs with AWGs fabricated in the same material system, we see that the minimal on-chip loss of AWGs with a similar footprint is only slightly lower (1.9dB versus 1.1dB for the SOI AWG) [54].

The average insertion loss over the four channels was 2.4dB and the different contributions were estimated as follows: 1.0dB is due to reflection loss at the DBR facets (taking into account non-verticality), 0.5dB is due to diffraction loss (inherent for the design and calculated using scalar

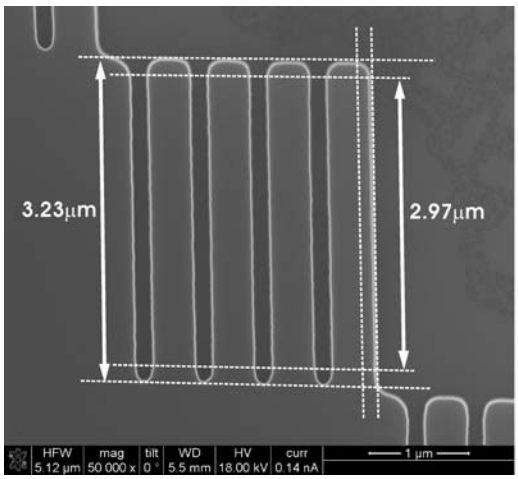


Figure 3.38: SEM picture of a DBR facet to demonstrate corner rounding and roughness

diffraction theory) and 0.9dB is excess loss. The excess loss is mainly caused by grating imperfections: roughness and corner rounding of the grating facets. As the transmission measurements were normalized to a photonic wire waveguide, the waveguide propagation losses and the chip-to-fiber coupling loss are not taken into account here.

Figure 3.38 is a top view SEM-picture of one of the 31 DBR grating facets of this particular PCG. The size of the grating facets around the pole is $\sim 3.23\mu$m and the corners are rounded over a distance of $r \simeq$130nm on each side of the facet. Light will be dispersed by the rounded corners into a wide range of angles and may propagate in the slab waveguide as stray light or unwanted orders that, if intercepted by the output waveguides, contribute to the crosstalk. To estimate the loss penalty due to corner rounding, we replace the width W of each facet by an effective width, $W_{eff} = W - 2r$. In paragraph 3.5, we calculated the diffracted field along the Rowland circle. Equation 3.14 shows us that the diffracted field of one grating facet is proportional to the facet width and a sinc-shaped diffraction envelope:

$$E_{out} \quad \sim \quad W_{eff}\mathrm{sinc}(k\Delta\beta W_{eff}/2) \tag{3.20}$$

For the central wavelength channels, $\Delta\beta \simeq 0$ and the diffracted field is proportional to W_{eff}. After calculating the overlap integral with the mode profiles of the output waveguides, the maximum channel response will be proportional to W_{eff}^2. This makes us conclude that the loss penalty due to

corner rounding for the central facets can be approximated by

$$L_{\text{corner rounding}} = 20log\frac{W_{eff}}{W} \tag{3.21}$$

This might be counter-intuitive (one would expect a 10log dependence) but can be explained by broadening of the diffraction envelope of a single facet for decreasing facet widths. For the channels further away from the center, this formula overestimates the loss penalty due to this broadening. For this particular PCG, the loss penalty due to corner rounding is $\sim$ 0.7dB and is the main contribution to the excess loss. The corner rounding is due to the lithographic resolution limits and the limited accuracy with which the mask pattern can be transferred to the waveguide by etching. Sharper corners can be obtained by a slight modification of the corner shape on the lithography mask (called serifs).

3.8.3 Crosstalk

Crosstalk usually refers to the unwanted signal arriving at a given channel from another channel and is a major issue in wavelength (de)multiplexing devices. Side lobes in the channel transmission spectra will cause crosstalk and are due to distortion of the optical phase and intensity distribution along the focal line. The origin of these phase and intensity distortions are fabrication imperfections of the grating, the slab section and/or the access waveguides.

Figure 3.39 plots the measured side lobe level for the different PCG demultiplexers discussed earlier. It is clear that the coarser the channel spacing and hence the smaller the devices, the lower the side lobe level is. Our FTTH demultiplexer with a channel spacing of 60nm has a sidelobe level better than -30dB, whereas the sidelobe of the fiber Bragg interrogator with a 1nm channel spacing increased to -10/-15dB.

Figure 3.40 illustrates the reproducibility of the spectral response of the various wavelength channels. Similarities and differences between the channels are emphasized by overlapping the channel spectra by shifting them by multiples of 3.2nm, the channel spacing. This device, a 1×30 demultiplexer was discussed earlier. The spectral shapes of the channels overlap very well, including the side lobe structures. These side lobes are nearly independent of the channel number within the same PCG as can be seen, but vary in position and to a smaller extent in strength from chip to chip. This makes us conclude that these side lobes are not due to experimental "white" noise or random scattering background noise but due to fabrication imperfections.

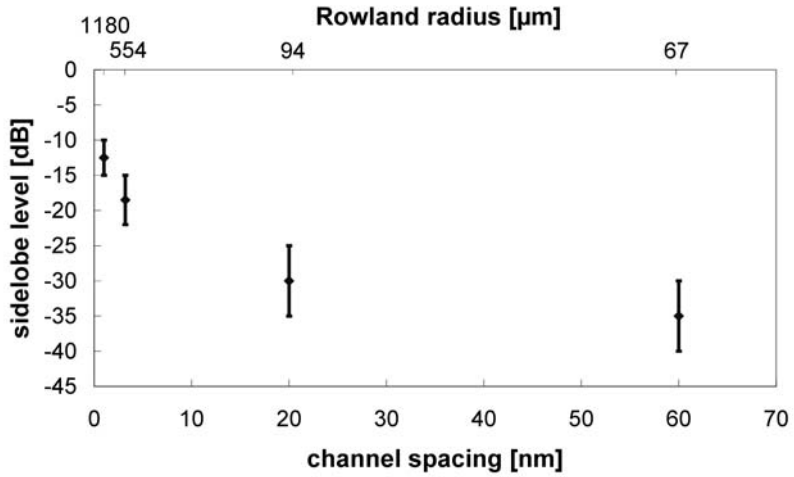


Figure 3.39: Side lobe level of fabricated PCGs with different channel spacings: 1nm, 3.2nm, 20nm and 60nm. The corresponding Rowland radius of the devices are also shown

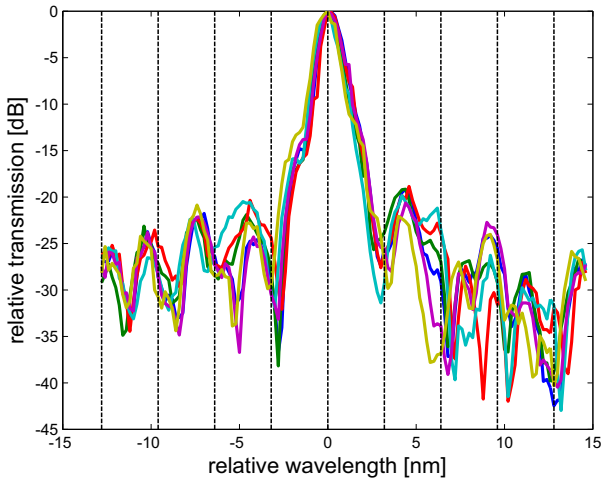


Figure 3.40: Overlapped spectra of 30 channel PCG obtained by normalizing and shifting the spectra of figure 3.27(c) by multiples of the nominal channel spacing, i.e. 3.2nm

3.8.3.1 Fabrication imperfections of the grating

Due to both the lithographic resolution limits and the limited accuracy with which the mask pattern can be transferred to the silicon waveguide layer by etching, the shape and the position of the grating facets deviate from their designed values. The most important grating errors are vertical sidewall tilt, corner rounding, roughness of the grating facets and position offsets caused by mask pixelation.

Mask pixelation A deviation between the designed position of the individual grating facets and the actual, as fabricated position is caused in part by mask pixelation. Deep-UV masks are written using an e-beam machine with a given step size. This means that the different points on the mask are snapped on a grid with a certain grid size. As each grating facet is defined by its two end points, snapping these on a grid will change both the position and the tilt of each facet:

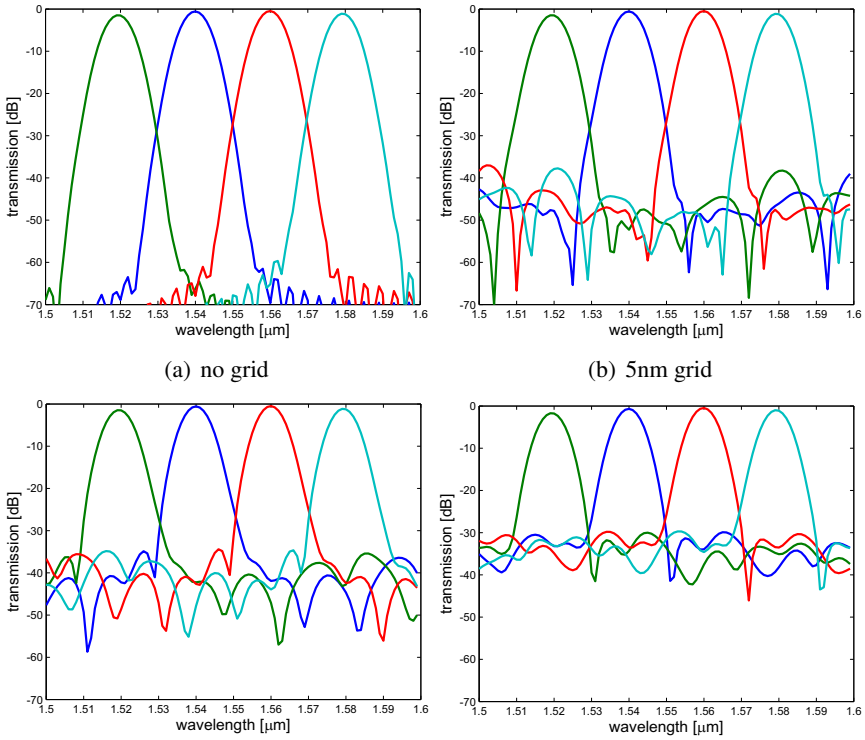
- A shift of the facets δx in the direction of the input waveguide causes a phase error $\delta\phi$:

$$\delta\phi = 2k\delta x = \frac{4\pi}{\lambda} n_{eff}\delta x \tag{3.22}$$

  According to this formula, PCGs fabricated in glass ($n_{eff} \sim 1.5$) have a better tolerance ($\sim$ two times) to errors in facet positions as compared to PCGs fabricated in a nanophotonic SOI ($n_{eff} = 2.83$) or InP/InGaAsP ($n_{eff} \sim 3.2$) material system. When snapping the end points on a 5nm grid, the worst-case phase error $\delta\phi$ for a nanophotonic SOI PCG is equal to $2 \times 2\pi/1550 \times 2.83 \times 2.5\ rad$ = $2\pi/110\ rad$ around a wavelength of 1550nm.

- A rotation (tilt) of the facet on the other hand will cause an amplitude error: the maxima of the sinc-shaped far-field profiles of the facets will no longer coincide at the blaze point.

We simulated the transmission spectrum of our 4×20nm PCG for different step sizes: no grid, 5nm, 10nm and 20nm. This is shown in figure 3.41. Similar results have been published for PCGs fabricated in InP/InGaAsP due similar values of n_{eff} in this material system [20]. We clearly see that side lobe levels increase for increasing grid sizes. Our simulation program allows to assess the influence of phase errors and amplitude errors separately. Simulations show that the contribution of amplitude errors is



(a) no grid (b) 5nm grid

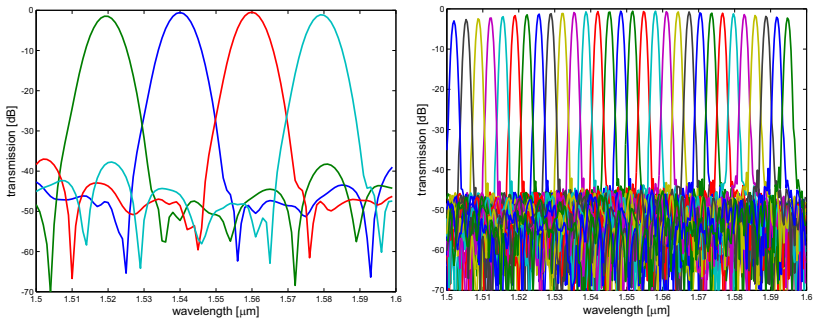
(c) 10nm grid (d) 20nm grid

Figure 3.41: Influence of grid snapping on transmission spectrum of the 4×20nm PCG

negligible as compared to the contribution of phase errors caused by grid snapping for the typical devices presented in this work.

The deep-UV masks we used for lithography were written with a step size of 5nm. In this case, simulations predict a side lobe level between -40 and -50dB as can be seen in figure 3.41(b). Although the tolerance to errors in facet position is twice as bad compared to glass PCGs, mask pixelation does not explain the -25 to -35dB side lobe level we encounter for these devices as shown in figure 3.39.

More simulations demonstrate that the side lobe level as a function of step size is almost unaffected by the size and the design of the PCG. So PCGs with a large Rowland radius and a high number of grating facets for dense wavelength filtering are as sensitive to variations of the facet positions as small PCGs with a reduced number of grating facets for coarse filtering. Figure 3.42 compares the 4-channel demux with 20nm channel spa-



(a) 4×20nm (b) 30×3.2nm

Figure 3.42: Sensitivity to mask pixelation (5nm grid) for the 4×20nm and 30×3.2nm PCG

cing, 31 facets and a 94μm radius with the 30-channel demux with 3.2nm channel spacing, 141 facets and a 554μm radius. Both devices have been described in detail in paragraph 3.7. As can be seen, snapping the end points of the facets on a 5nm grid results in side lobes between -50 and -40dB in both cases.

This is first of all because the effect of amplitude errors caused by grid snapping are negligible compared to the effect of phase errors for the devices studied in this work. The phase errors caused by grid snapping are not depending on the Rowland radius of the PCG, the amplitude errors on the other hand increase for PCGs with larger radii as the far-field profiles will shift over a larger distance along the focal curve for a given facet tilt error. Secondly, the total phase error of the field along the focal line is an average of the individual phase errors caused by grating facet offsets and as a consequence, a larger number of grating facets does not results in stronger side lobes.

By comparing these simulation results with our measurements, we can conclude that mask pixelation with a 5nm grid size is not strongly affecting the side lobe levels of our nanophotonic PCGs. Simulation results of gratings snapped on a 5nm grid predict a side lobe level around -40dB which is not affected by the Rowland radius. This is not in agreement with our measurements in which side lobe levels strongly increase for PCGs with larger radii as show in figure 3.39 and is, in any case, higher than -40dB.

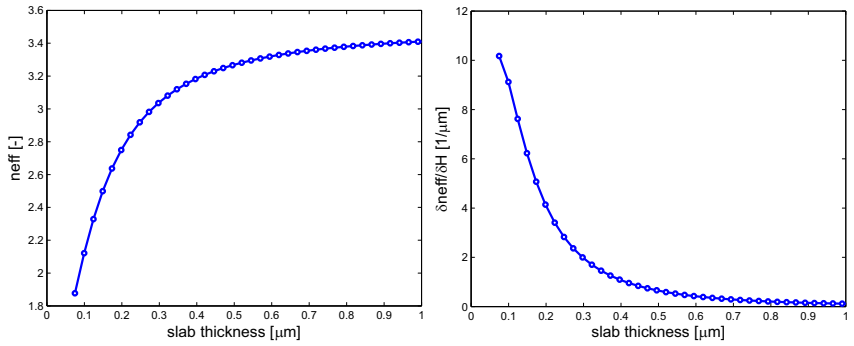
Tilt of grating facets The non-verticality of grating facets can cause reflection loss (see paragraph 3.6.4.2) and deteriorate the crosstalk. This is because the reflected mode does not perfectly couple with the fundamental

slab mode. A part will couple to radiation modes that do not contribute to crosstalk and another part couples to higher order slab modes. As these modes have different effective indices of refraction, multiple images will be formed along the focal line resulting in distinct side lobes (ghost peaks). As mentioned earlier, most material systems have a rather thick waveguide core (>500nm) and as a consequence, the reflection loss and crosstalk critically depends on grating verticality [55]. In [32], the authors estimate the generated crosstalk by assuming that all the light that does not couple to the fundamental slab modes (TE and TM) couples to higher order modes and increases the side lobe level.

As mentioned earlier, our etching process is not optimized to create perfectly vertical grating facets and results in a rather large non-verticality of $\sim 10^{\circ}$. However, due to the thin waveguide layer, these angled sidewalls cause a very small additional loss of only $\sim 0.3dB$ for standard grating facets. As this 220nm thick slab waveguide only supports one guided TE mode and one guided TM mode, the fundamental TE mode cannot couple to higher order modes. We can conclude that for the nanophotonic SOI platform, the grating non-verticality does not affect the level of the side lobes. This is not the case in most other material systems where it can be the main contribution [32, 55].

Corner rounding and facet roughness Due to rough grating surfaces and rounded corners, light is scattered into a wide range of angles and disturbs the far field profile of each grating facet causing both amplitude and phase errors along the focal line. Therefore the channel response will decrease (excess loss) and the background level and side lobe intensities will increase.

A rigorous treatment requiring significant computation power is out of the scope of this work. In [56], the influence of surface roughness on insertion loss was studied for a glass PCG using a method of moment (MoM) simulation technique. In [57], this was done for large core SOI PCGs. Although no simulation results are available for the PCGs we designed, we believe that shape variations of the facets (long range variations, roughness and corner rounding) can deteriorate the crosstalk performance. However, we cannot explain the strong dependence of the crosstalk level on the PCG size as shown in figure 3.39. The excess loss of the large PCG with 3.2nm channel spacing is only ∼1dB higher as compared with the small device with 20nm channel spacing. Moreover, if light is scattered in a certain range of angles, it will be spread over more waveguides for the largest device. In-depth simulations need to be carried out to assess the effects of grating shape variations and fully understand its influence on channel



(a) Effective refractive index

(b) Change of effective refractive index per micrometer of thickness change

Figure 3.43: Properties of the fundamental TE-polarized mode for different thickness of the Si slab waveguide core ($\lambda = 1.55\mu$m)

crosstalk.

3.8.3.2 Imperfections of the slab waveguide

Variations of the Si waveguide layer thickness in the slab region of PCGs cause variations of the effective refractive index of the slab waveguide mode. We discussed earlier the advantages of having a thin waveguide layer: increased tolerance on sidewall non-verticality and no propagation of higher order modes. However, due to this thin waveguide layer, the effective refractive index of the fundamental TE-polarized slab mode strongly depends on the Si thickness. This is shown in figure 3.43. Figure 3.43(a) plots the effective refractive index for $\lambda = 1.55\mu$m as a function of Si thickness, H and figure 3.43(b) is the derivative and plots the change of this index for varying waveguide thickness. As can be seen, the effective index becomes very dependent on the waveguide thickness for thin waveguide layers. For a 220nm thick Si layer, $\delta n_{eff}/\delta H \simeq 0.004nm^{-1}$. These thickness variations cause phase errors that are dependent on the size of the PCG:

$$\delta\phi = \frac{2\pi}{\lambda} L \delta n_{eff} \tag{3.23}$$

where L is the distance from the input waveguide to a grating facet and back to the output waveguide.

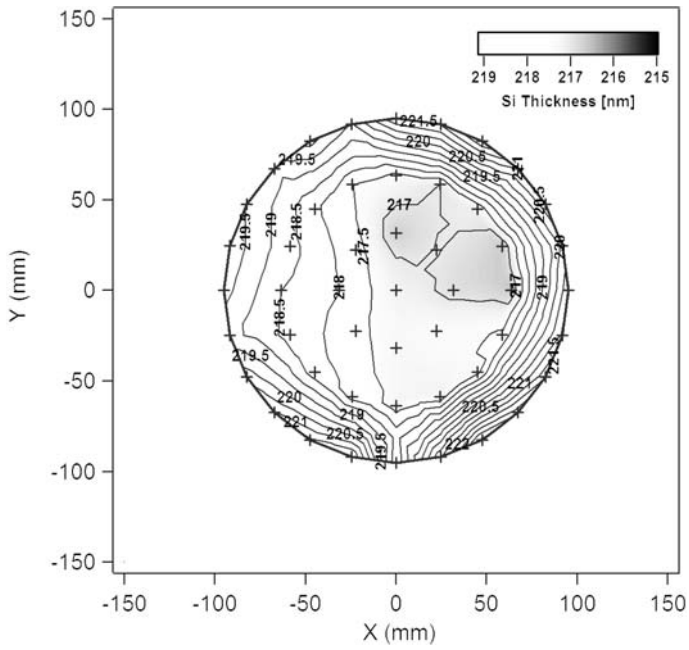


Figure 3.44: Silicon layer thickness map over a 200mm SOI wafer.
Courtesy S.K. Selvaraja [58]

Recently, the thickness variation of the top Si layer over a 200mm wafer was measured using ellipsometry by coworker S.K. Selvaraja [58]. This is shown in figure 3.44. The radial thickness profile (”bull’s eye”) is typical for a chemical mechanical polishing (CMP) process such as the one used in the SOI wafer fabrication process. The mean wafer thickness is 219.1nm (220nm target), the standard deviation is 2nm with a total thickness variation of 7.1nm. Also within a shorter distance range of 10mm, the thickness varies as much as 1nm, which will cause observable non-uniformity within a die. This data is measured over the full wafer after 10mm edge exclusion on a grid with 49×49 data points.

The influence of slab thickness variations on crosstalk level has not been studied in literature to the best of our knowledge because most PCG that have been reported are fabricated in material systems with a thick ($>$500nm) waveguide layer. In these material systems (silica, InP, GaAs, large-core SOI, ...) small variations of H have no major influence on the properties of the fundamental slab mode. Our simulation approach based on scalar diffraction (paragraph 3.5) supposes a uniform slab region and as a consequence a rigorous study of the influence of thickness variations on

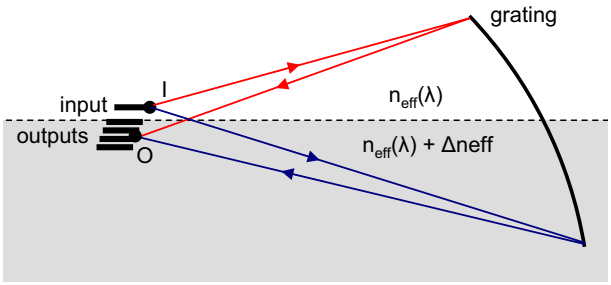


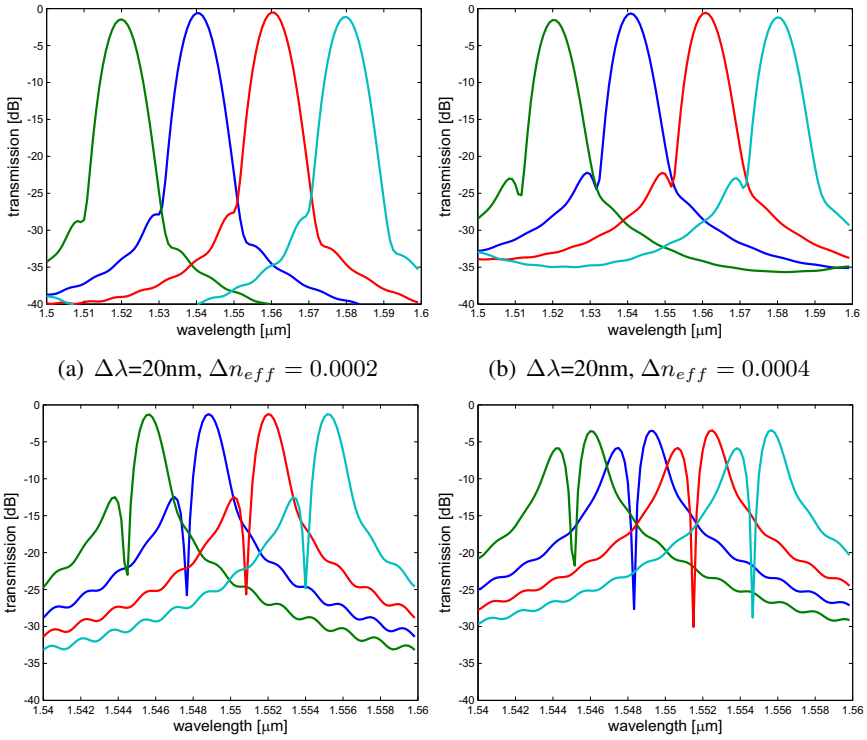
Figure 3.45: Layout of a PCG with a non-uniform slab region consisting of two different slab waveguide thicknesses

the performance cannot be studied.

By means of a simplified simulation example, we show that slab thickness variations are possibly the main cause of side lobes and crosstalk for PCGs fabricated on a nanophotonic SOI platform. Figure 3.45 shows the simulated layout. We divided the slab region and the grating into two equal parts, each corresponding with a different Si thickness and hence a different n_{eff}. We suppose that the incident and diffracted rays on and from the upper half of the grating travel in a uniform slab region with an effective refractive index $n_{eff}(\lambda)$. The rays on the lower half part have an effective index $n_{eff}(\lambda) + \Delta n_{eff}$. We do not take into account reflection and refraction at the horizontal interface between the two slab regions.

Figure shows 3.46 the transmission spectrum of four channels of our standard PCGs with a 20nm and a 3.2nm channel spacing as discussed earlier. The Rowland radius, R of the 20nm channel spacing PCG is 94μm and the PCG with 3.2nm channel spacing is $\sim$6 times as large: $R = 554\mu$m. Two situations were studied: Δn_{eff} = 0.0002 and 0.0004. This corresponds with a very modest thickness variation of $\sim$0.05 and 0.1nm respectively between the upper and lower half part of the slab region. These simulations show that very small variations of the slab thickness can generate very strong side lobes. A modest thickness variation of 0.05nm generates side lobes at a level of -30dB for the PCG with 20nm channel spacing. However, for the larger device with a 3.2nm channel spacing, the side lobe level is much higher (-12dB). When the thickness variation increases to 0.1nm (figure 3.46(b) and 3.46(d)), the side lobes have raised to an unacceptable level, especially for the largest device.

Although the simplified simulation model as presented here is not a rigorous treatment of the problem, it indicates that very small thickness variations can generate strong side lobes. More important, these simulations



(a) $\Delta\lambda$=20nm, $\Delta n_{eff} = 0.0002$

(b) $\Delta\lambda$=20nm, $\Delta n_{eff} = 0.0004$

(c) $\Delta\lambda$=3.2nm, $\Delta n_{eff} = 0.0002$

(d) $\Delta\lambda$=3.2nm, $\Delta n_{eff} = 0.0004$

Figure 3.46: Influence of slab non-uniformity on transmission spectrum

reveal a behavior which is in good agreement with our experimental data. Firstly, there seems to be a strong dependency of the side lobe intensity on the size of the device. Large devices which perform a dense wavelength filtering seem to be very sensitive to these thickness non-uniformities. Secondly, the position of these side lobes within a channel does not change significantly for different channels. To assess this problem in-depth, optical simulations allowing non-uniform slab regions should be carried out in the future. This way, measurement data could be matched to these simulations by means of a map of the slab thickness of the SOI wafer as presented in figure 3.44. We believe that not only the magnitude of the thickness variations, but also the variation range (long/short) and the orientation of the PCG in respect to these variations could play an important role.

When comparing arrayed waveguide gratings (AWGs) with PCGs, we notice that AWGs have, next to slab thickness variations, an additional source of phase errors. In an AWG, the waveguide arms with an increasing delay length replace the grating facets (and the slab section) of a PCG. The relative phase of the light propagating in these different waveguides depends on the geometrical length of the arrayed waveguides, the refractive index and also the waveguide cross-section dimensions. This means that the phase delay in each arm not only depends on the thickness of the Si layer (as is the case for PCGs) but also on the exact waveguide width. The high index contrast, sub-micrometer size waveguides are very sensitive to small width variations as discussed in chapter 2. Phase errors caused by these variations form the largest contribution to AWG crosstalk [16, 27]. Again, the influence of these width variations increases with the size of the arrayed waveguides. These errors are difficult to control in a manufacturing environment but thermal tuning could be employed to compensate for these non-uniformities [59].

3.8.3.3 Fabrication imperfections of the access waveguides

If the access waveguides are well designed, i.e. their spacing is large enough in order to avoid coupling between them, we believe their influence on the crosstalk (due to fabrication imperfections) can be neglected. The channel side lobe level will not be affected by small variations in the position and the width of the waveguide apertures.

The optical mode launched into the slab waveguide should have a well-defined single mode structure as higher order modes could create side lobes near the channel maxima. As mentioned earlier (paragraph 3.6.2) we make use of double (deep+shallow) adiabatic tapers to convert a deeply etched 500nm wide photonic wire waveguide into wider (e.g. 2μm) waveguide

apertures. In a worst case scenario, there could be a misalignment of 50nm between the deep and the shallow taper. Eigenmode expansion simulations show us that in this worst case scenario, excitation of higher order modes and hence the side lobe intensity is negligible.

3.8.4 Conclusion

In this paragraph, we assessed the PCG performance in more detail. We discussed the influence of fabrication imperfections on both insertion loss and crosstalk. First, we analyzed the excess loss due to corner rounding and we concluded that the amount of excess loss can be estimated by replacing the width, W of each facet by an effective width, W_{eff}.

Secondly, we analyzed crosstalk in more detail. Crosstalk is caused by side lobes in the channel transmission spectra. Measurement results reveal that the side lobe level strongly depends on the radius of the device. Devices with a dense spectral channel spacing require a long slab section in order to obtain a large linear dispersion. These devices seem to have stronger side lobes as compared to PCGs with a smaller radius for coarse wavelength filtering. We analyzed the influence of possible fabrication imperfections caused by the grating, the slab section and the access waveguides. We identified variations of the slab waveguide thickness as being probably the most important source of crosstalk. A simplified simulation model shows us that very small slab thickness variations can generate strong side lobes. The intensity of these side lobes is strongly depending on the device size, which is in agreement with experimental data.

3.9 Cascaded filters

3.9.1 Introduction

The ultimate resolution of planar spectrographs like AWGs and PCGs is linked to the number of waveguides and grating facets respectively. The resolving power R of these devices is defined as $R = \lambda/\Delta\lambda$, where $\Delta\lambda$ is the smallest resolvable wavelength difference. One can show that for gratings, $R = m \times N$, where m is the order of diffraction and N is equal to the number of waveguides/facets.

So in order to obtain a higher resolution, on possibility is to increase the number of waveguides or facets for a fixed order of diffraction. To accommodate these, the footprint of the entire spectrograph will get larger: the waveguides of an AWG will get longer and the radius of the slab region of the PCG has to increase to illuminate the additional grating facets. As we

discussed above, this will result in reduced performance due to phase errors that scale with the size (or better length) of the device. For a PCG, these phase errors are caused by slab thickness non-uniformities and for AWGs, there is an additional contribution: next to waveguide thickness variations, also waveguide width variations cause path length dependent phase errors.

Another possibility to increase the resolution is to make use of higher diffraction orders. However, as the free spectral range (FSR) is inversely proportional to m: $FSR \sim \lambda/m$, increasing the order of diffraction limits the FSR and as a consequence, the operational wavelength range of the device.

For spectrometer applications in which a large operational range is needed (e.g. $>$ 100nm) in combination with a high resolution (e.g. $\Delta\lambda <$ 0.5nm), the performance of both nanophotonic SOI AWGs and PCGs will not be satisfactory. In this situation, a small order of diffraction m is needed in combination with a large number of waveguides/facets.

In 2009, we demonstrated for the first time the combination of a PCG and ring resonators in the same device. Using these cascaded filters, a high resolution spectrometer with a large operational range on a nanophotonic SOI platform becomes feasible [60]. Cascading ring resonators and PCGs allows to take advantage of both: on one hand, very narrow spectral filters with 0.2 nm 3dB bandwidth can be implemented on SOI using ring resonators if their FSR is kept sufficiently small ($<$20nm) and on the other hand, PCGs can be used for coarse wavelength filtering with a low insertion loss and high side lobe suppression over a broad wavelength range ($>$100nm). This way, the PCG can be used for a coarse filtering of the input signal (e.g. 10$\times$10nm spaced channels) and ring resonators filter a very narrow peak ($<$0.2nm) out of each channel.

3.9.2 Cascaded echelle grating and ring resonators

A scanning electron microscope image of the device we fabricated is shown in figure 3.47. It consists of a PCG with 5 channels separated by 7nm. The output of each channel is connected to 11 ring resonators in series. Each of the 11 rings has a slightly different circumference in order to drop 11 different wavelengths with a $\sim$1nm spacing from each PCG channel. As each ring drops a wavelength from a PCG channel, the total insertion loss is equal to the sum of the insertion loss of the PCG and the ring resonator. In order to limit the total insertion loss, we designed a PCG with strongly overlapping channels by making the input waveguide 7μm wide. The output waveguides are 2μm wide. The ring resonators have a 3dB bandwidth of 0.3nm with a FSR of $\sim$11nm. The radii changing from 7.6 to 7.7μm and

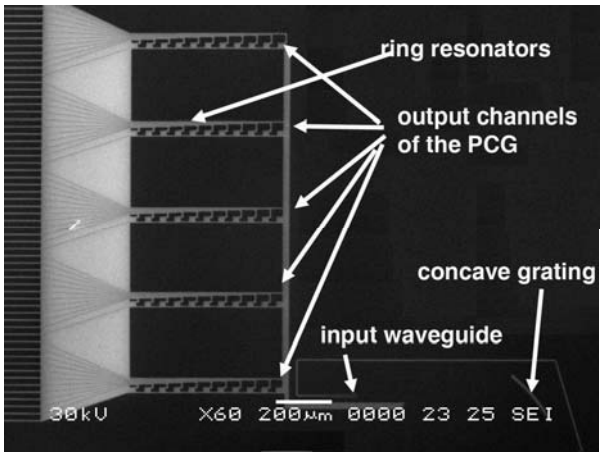
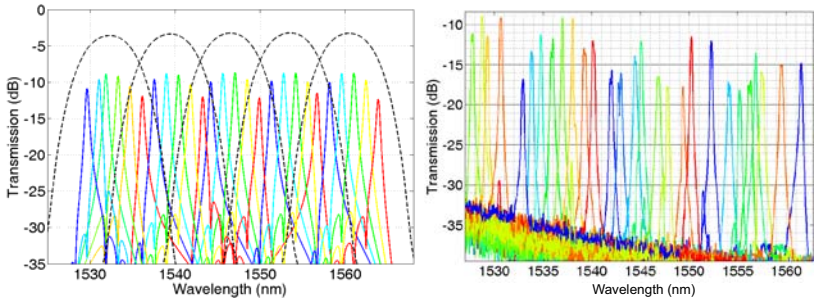


Figure 3.47: Scanning electron microscope image of the cascaded PCG/RR filter

2μm long straight sections are separated from the waveguides by a 200nm gap. In order to select a single peak of the ring resonator spectrum, the FSR of the rings is designed substantially larger than the PCG channel spacing (11nm versus 7nm respectively). As a consequence, a part of the rings on each PCG channel will not be used as these wavelengths will be covered by other rings in other PCG channels. A simulation of the demultiplexer response is shown in figure 3.48(a).

The measured spectral response is given in figure 3.48(b). The insertion loss varies between 9dB and 17dB, which is relatively high for this proof of principle device but could be reduced to $<$5dB in future. The non-uniformity of the channels can be attributed to sensitivity of the coupling coefficient of the ring resonators to small deviations of the gap and the waveguide thicknesses of the rings [61]. The channel spacing is quite uniform around 1nm. The 3dB bandwidths of the peaks range between 0.2 and 0.4nm. 28 out of the 55 channels have been used, discarding the ones with high insertion loss, overlapping peak, and high side lobes.

Another very similar approach reported recently makes use of a single ring resonator at the input of the PCG[62]. The authors connected the drop port of a single ring resonator to the input of the PCG. By tuning the spectrum of the ring, each wavelength can be filtered out of each PCG channel and the resolution is limited by the spectral width of the ring resonator spectrum. This approach needs active tuning but offers a higher flexibility as sweeping the ring spectrum allows to select each wavelength within the PCG channels.



(a) Simulated spectral response (b) Measured spectral response

Figure 3.48: Spectral response of the cascaded PCG/RR filter

The proof of concept device we presented here demonstrates the possibility to obtain high resolution spectral filtering over a broad wavelength range by combining PCGs and ring resonators. Further improvements mainly include decreasing the insertion loss. By making use of PCGs with a flat top channel response, insertion losses of a few dB can be achieved.

3.10 Conclusion

In this chapter, we explained the design and fabrication of PCGs on a nanophotonic SOI platform in detail. We showed that this material systems offers many advantages for the fabrication of PCGs as compared to other low- to medium index contrast material systems: strict fabrication tolerances on facet verticality are strongly relaxed, the footprint can be drastically reduced and there is no propagation of higher order slab modes which possibly deteriorates the performance. Moreover, we demonstrated that by replacing the standard grating facets by Bragg reflectors, the on-chip loss can be reduced to record low values of 1.9dB.

For polarization independent operation, we demonstrated PCGs mounted in a polarization diversity configuration. We also focused on some practical applications: fiber Bragg interrogators, FTTH transceivers and biodiesel sensors. In a next part, we assessed the influence of fabrication imperfections on the performance and identified slab thickness variations as being a major source of crosstalk. Finally, we demonstrated for the first time a very compact high resolution spectrometer based on a cascaded PCG and ring resonators. These CMOS compatible microspectrometers could possibly find application in low cost, on-chip biological and chemical sensors, optical coherence tomography, medical instrumentation, ...

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4

Integration of photodetectors on SOI waveguides

In this chapter, we discuss different materials, technologies and coupling schemes that are suitable for the integration of near-infrared photodetectors on SOI. It serves as an introduction to chapter 5 in which we will discuss the design and fabrication of an integrated InGaAs-on-SOI detector. This chapter is organized as follows. In a first part, we focus on integration technology. In a second part, we discuss various waveguide-to-detector coupling approaches and the last part gives an overview of the state-of-the-art and compares the performance of InGaAs-on-SOI and Ge(germanium)-on-SOI detectors.

4.1 Introduction

Silicon is an excellent material for the fabrication of passive photonic integrated circuits (PICs). The advantages of the nanophotonic SOI platform both in terms of manufacturing and device performance have been discussed in previous chapters. For active functionalities such as photodetection and -generation at near-infrared (NIR) wavelengths, other materials are better suited. Silicon is optically transparent in the NIR wavelength region at which optical telecommunication typically operates (1.31 and 1.55μm). As a consequence, very low loss waveguides can be fabricated but other materials need to be integrated to obtain efficient absorption for NIR photodetector applications. Also, silicon cannot efficiently emit light. This is due to its indirect band gap which makes non-radiative carrier recombination much more probable than radiative combination, which is required for photo-emission. An all silicon electrically pumped laser is a long standing quest in silicon photonics and still needs to be demonstrated [1].

For these active functionalities, III-V compound semiconductors are better suited. The InP/InGaAsP material system has a long standing reputation for the fabrication of NIR sources (laser diodes, LEDs), amplifiers and detectors: most commercially available high speed, high efficiency telecom detectors have an InGaAs photo active layer. While monolithic integration of active and passive functionalities in the InP/InGaAsP material system is commonly done and even commercially available (e.g. Infinera), it has some disadvantages as compared to silicon in terms of achievable integration density, cost and fabrication [2, 3]. This is due to respectively the smaller refractive index contrast, the higher material cost, the smaller wafer size and the CMOS processing incompatibility of the InP/InGaAsP material system as compared to SOI.

In this work, we will focus on the integration of InP/InGaAs for the fabrication of NIR photodetectors on SOI. This is called heterogenous integration: the integration of dissimilar semiconductor materials on a common substrate. Heterogeneous integration allows to combine best of both worlds. One one hand, high density passive waveguide circuits and filters are fabricated on low cost, high quality SOI substrates making use of CMOS compatible tools and on the other hand, other semiconductor materials (III-V compounds in this case) are integrated for the fabrication of efficient active functionalities.

4.2 Materials for photodetection in the near-infrared

In this paragraph, we identify semiconductors which can be integrated on silicon and which allow to obtain efficient photodetection in the near-infrared and more specific, the wavelength windows typically used for optical telecommunication around 1.31 and 1.55μm.

4.2.1 Optical band-to-band absorption

Optical band-to-band absorption is the excitation of an electron from valence band to conduction band by the absorption of a photon having an energy greater than the band gap for direct band gap materials or by the simultaneous absorption of a photon and absorption or emission of a phonon for indirect band gap materials. The energy of a photon is given by

$$E = h\nu \tag{4.1}$$

where h is Planck's constant and ν is the frequency of the light. Absorption leads to an exponential decay of the propagating radiation power density, $P(x)$:

$$P(x) = P(0)e^{-\alpha x} \tag{4.2}$$

The absorption coefficient α is characteristic for the material and is a strong function of wavelength. Figure 4.1 show the absorption coefficient for several indirect (Ge, Si) and direct ($In_{0.53}Ga_{0.47}As$, GaAs) band gap semiconductors. The penetration depth is the inverse of the absorption coefficient and is a measure of how deep the light penetrates into the material. It is defined as the depth at which the intensity of the radiation inside the material falls to 1/e (about 37%) of the original value at the surface.

Direct band gap materials like InP, $In_{0.53}Ga_{0.47}As$ and GaAs are generally more efficient emitters and absorbers of optical energy as compared to indirect band gap materials. In a direct band gap material, an electron can go from one band to the other by simply absorbing a photon of energy close to the direct band gap. In an indirect band gap material, this is not the case. Next to energy, the electron also needs to acquire (or give off) crystal momentum. This can be done by absorbing or emitting a phonon at the same time. Such a three-body collision is statistically unlikely and as results, indirect band gap materials such as Si and Ge are not very efficient absorbers at wavelengths near the (indirect) band gap.

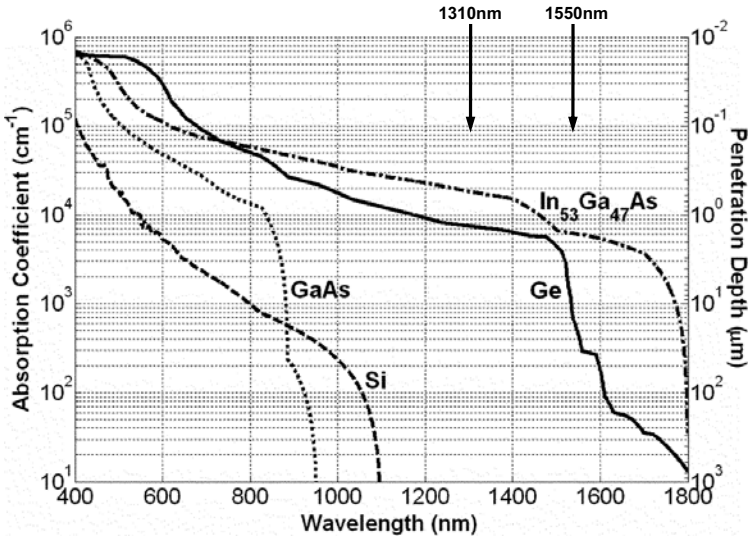


Figure 4.1: Overview of the optical absorption and penetration depth of Si, Ge, GaAs and InGaAs (Taken from [4])

Properties	**Silicon**	**Germanium**	**$In_{0.53}Ga_{0.47}As$**
Lattice constant [nm]	0.5431	0.5658	0.5869
Direct bandgap [eV]	3.3 (0.38μm)	0.8 (1.55μm)	0.75 (1.65μm)
Indirect bandgap [eV]	1.13 (1.1μm)	0.66 (1.88μm)	

Table 4.1: Material properties of Si, Ge, and InGaAs at 300K

To obtain efficient photodetection, two things are needed. First of all, there has to be sufficient absorption to generate electron-hole pairs. Secondly, an electric field needs to be applied across the absorbing layer to separate and collect the photogenerated carriers in order to create a photocurrent. This will be discussed later. For a given semiconductor, the wavelength range in which appreciable photocurrent can be generated is limited. The long wavelength cutoff λ_c is established by the band gap E_g of the semiconductor:

$$\lambda_c = \frac{hc}{E_g} = \frac{1.24}{E_g[eV]}[\mu m] \tag{4.3}$$

For wavelengths longer than λ_c, α is too small to give appreciable absorption. The short wavelength cutoff of the photocurrent on the other hand is caused because the values of α for short wavelength are very large. As a consequence of that, light will be absorbed very close to the surface, where the recombination time is short. The photogenerated carriers thus can recombine before they are collected.

For direct band gap materials, the absorption coefficient increases sharply for wavelengths shorter than λ_c. With indirect band gap materials, a simultaneous interaction between an electron, photon and phonon is needed and the result is that α increases only gradually as the wavelength reduces below cutoff. At even shorter wavelengths, where excitation across the direct bandgap becomes possible, α increases again (3.3eV for Si and 0.8eV for Ge). Table 4.1 gives an overview of the lattice constant and band gaps of Si, Ge and InGaAs.

Suitable materials for photodetection need to have a high absorption coefficient in order to be able to fabricate compact devices which can operate at high frequencies. As can be seen in figure 4.1, silicon becomes transparent for wavelengths above 1.1μm, which corresponds with its indirect band gap, whereas both $In_{0.53}Ga_{0.47}As$ and germanium have a much higher absorption coefficient in the NIR spectral region. These two materials are the most promising at the moment to integrate efficient and reliable NIR photodetectors on silicon.

4.2.2 Germanium

Both germanium and silicon have a diamond cubic crystal structure, are positioned in the fourth column of the periodic table of Mendeleev and are indirect band gap materials. Figure 4.1 shows the coefficient of absorption of bulk silicon and germanium as a function of wavelength. The effect of

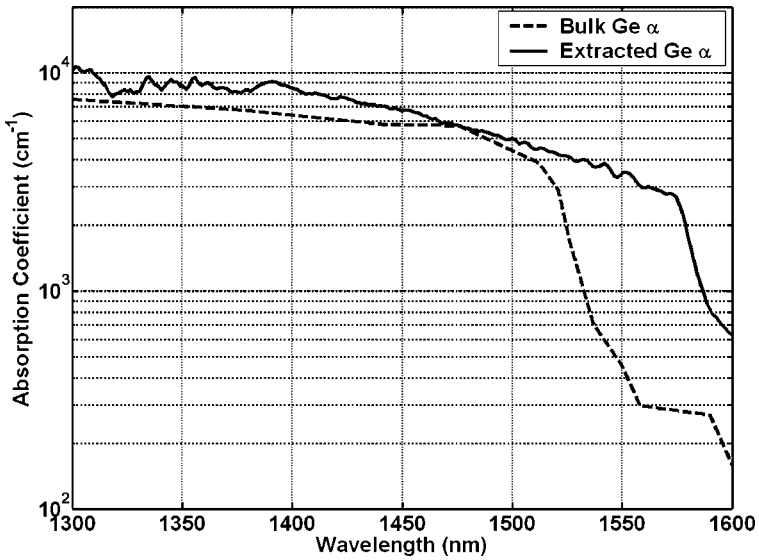


Figure 4.2: Comparison of absorption coefficient of strained Ge and bulk Ge (Taken from [4])

the band gaps of germanium on its absorption coefficient are very clear. For photon energies in between the indirect (0.66eV) and direct (0.8eV) band gap, the absorption is determined by the indirect bandgap and it increases rather slowly for increasing photon energies. At a wavelength of 1.55μm, corresponding with the direct band gap, the absorption coefficient is still relatively small ($\alpha \approx 460cm^{-1}$) and would require thick or long active regions in order to achieve high efficiency, resulting in slow devices. On the other hand, when the photon energy exceeds the direct bandgap energy (0.80eV), the coefficient rapidly increases. At the telecom wavelength window around 1.31μm, it reaches a high value ($> 7000cm^{-1}$) which allows absorption over short distances (a few micrometer) and efficient photodetection.

Today, most leading chip manufacturers already integrate germanium (SiGe) in the CMOS process by heteroepitaxial growth. This way, transistor performance can be increased by creating strained Si. The main problem to integrate germanium on silicon by epitaxial growth is the 4.2% lattice constant mismatch (Table 4.1). This mismatch can drive the introduction of dislocations that harm the performance of photodetectors.

The most successful approach to obtain both a high absorption at 1.55μm, and to avoid the influence of dislocations at the same time has been a two-step epitaxial growth process. First, a thin ($\sim$50nm) Ge buffer layer is

grown at a low temperature. The buffer layer completely relaxes the mismatch strain by insertion of dislocations. Then, a thick Ge layer is grown at a higher temperature [5]. This is done in order to create tensile strain in the Ge layer which narrows the band gap and red-shifts the absorption edge. This is shown in figure 4.2 [4]. By growing a pure Ge film at a temperature of 600°C, the authors succeeded in increasing the absorption coefficient from ($\approx 460cm^{-1}$) at wavelength of 1.55μm - which is not sufficient for efficient photodetection - to $\sim$3500cm^{-1} and even higher absorptions up to 5000 cm^{-1} have been reported elsewhere [6]. Generally, the two-step growth is followed by an annealing step to further reduce the threading dislocation density [4, 7, 8].

Since 2007, efficient Ge detectors integrated with silicon-based waveguides operating at wavelengths of 1.55μm have been reported in literature. An overview will be given in paragraph 4.8.

4.2.3 InGaAs

In optoelectronics, III-V semiconductors are widely used due to their direct band gap, which enables efficient light generation and detection. Figure 4.3 shows the lattice constant and band gap of Si, Ge and several III-V compound semiconductors [9]. Dots represent the binary semiconductors and lines connecting them correspond to ternary compounds. Solid lines represent direct band gap material and dashed lines are ternary compounds with an indirect band gap. The area of a closed polygon corresponds to quaternary compounds such as InGaAsP. Horizontal lines passing through InP and GaAs show lattice-matched compounds.

For optical communication applications with emission wavelengths around 850 and 980nm, GaAs/AlGaAs is typically used while around 1.31 and 1.55μm, the InP/InGaAsP material system is used. As can be seen by the horizontal line passing through InP, the band gap of InP can be reduced considerably by making the quaternary compound $In_{1-x}Ga_xAs_yP_{1-y}$ while the lattice constant remains matched to InP. This makes efficient detection at longer wavelengths possible. The smallest direct band gap of $\sim$0.75eV, corresponding with a wavelength of $\sim$1.65μm can be obtained for $In_{0.53}Ga_{0.47}As$. In order not to overload our text, we will write $In_{0.53}Ga_{0.47}As$ as InGaAs from now on, i.e. the lattice matched compound to InP. For the telecom wavelength windows around 1.31 and 1.55μm, the absorption coefficient of InGaAs is significantly larger as compared to strained and bulk Ge. InGaAs has an absorption coefficient of $7820cm^{-1}$ around a wavelength of 1.55μm [10].

Due to the large lattice mismatch between InGaAs and Si (8.1%), the

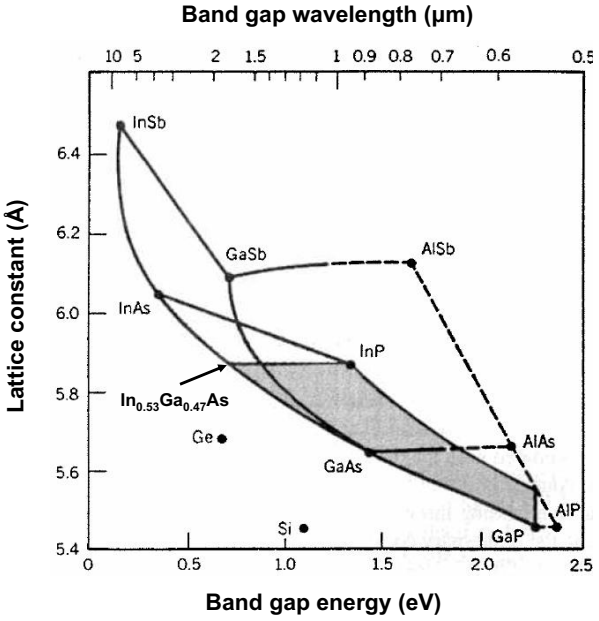


Figure 4.3: Lattice constants and band gap energies of III-V semiconductors, Ge and Si. Shaded areas correspond to possible InGaAsP and AlGaAs structures with a direct band gap. (from [9])

epitaxial growth of InGaAs on Si is even more problematic as compared to the integration of Ge on Si. Different ways to integrate both materials will be discussed in paragraph 4.3.

4.2.4 Conclusion

For the fabrication of SOI waveguide integrated photodetectors that operate in the typical optical communication windows around 1.31 and 1.55μm, both Ge and InGaAs are attractive materials. InGaAs has a long standing reputation in the field of high performance photodetectors for telecom applications at these particular wavelengths due to its ideal electro-optical properties. With a direct band gap wavelength of 1.65μm, efficient detection at these wavelengths is possible.

Whereas the integration of InGaAs in a CMOS fab could possibly raise cross contamination issues, this is not the case for germanium. Chip manufacturers already make use of epitaxially grown Ge for advanced CMOS devices and this same integration technique could be used for the fabrication of on-chip photodetectors. At a wavelength of 1.55μm however, which cor-

responds to the direct band gap of bulk Ge, the absorption is too small to obtain efficient photodetection. In recent years, different research groups (e.g. UPS, LETI, Intel, IBM) have focused on special growth strategies to increase the absorption of Ge by introducing strain and to eliminate the performance degradation due to the presence of dislocations.

In paragraph 4.8, we will give an overview of the state-of-the-art and compare the performance of both technologies: Ge-on-SOI and InGaAs-on-SOI detectors. In this work, we focus on the integration of InP/InGaAs for the fabrication of integrated detectors. This choice will be motivated in paragraph 4.9.

4.3 Heterogeneous integration of III-V active devices

In the previous paragraph, we explained that the integration of III-V semiconductors on SOI PICs allows to combine best of both worlds. Using InP/InGaAsP and InP/InGaAs respectively, very efficient near-infrared sources and detectors can be integrated on very compact silicon waveguide circuits. This heterogeneous integration can be carried out in different ways. In this section, we will briefly discuss different technologies for integrating InP/InGaAs detectors: hybrid integration of preprocessed photodetectors, heteroepitaxial growth of III-V material on silicon and bonding of unprocessed III-V epitaxial material onto the silicon-on-insulator substrate. A schematic overview of these integration approaches is shown in figure 4.4.

4.3.1 Hybrid integration

A first approach is the integration of processed InGaAs detectors or detector arrays on the SOI waveguide substrate using a flip-chip bonding technique. In literature, this approach is often referred to as hybrid integration. Flip-chip integration has been used for many years and, as a result, is a relatively mature process. In electronics, flip-chipping is often used to attach bare CMOS dies onto a printed circuit board. Flip-chip bonding involves mating the surface of detectors with the SOI substrate making use a high accuracy pick-and-place machine and metal bumps or solder bumps to connect the bottom contact of the detector with contact pads on the SOI substrate. The top contact can be connected by a wire bond but more often, the detector is designed so that both contacts are in the same plane. In some cases, the InP substrate is largely removed before bonding.

In [11, 12], the authors flip-chipped InP/InGaAsP laser diodes into a recess, etched into the SOI substrate. Au/Sn solder bumps were used for the electrical, mechanical and thermal contact between the laser diode and

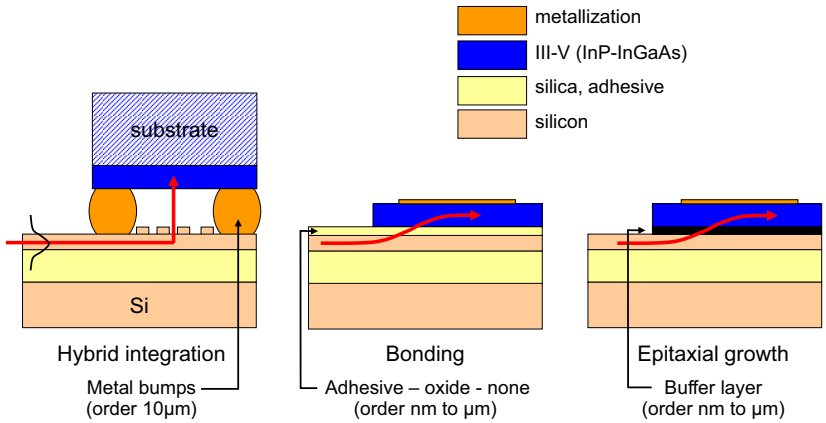
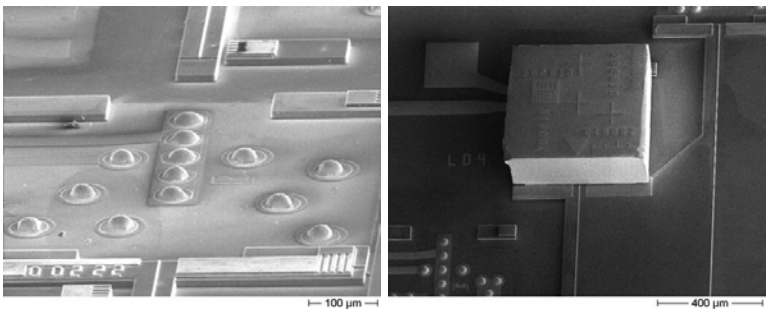


Figure 4.4: Technological approaches for heterogeneous integration InP/InGaAs on SOI. The typical thickness of the intermediate bonding layer (if present) is specified

contact pads on the SOI substrate. Figure 4.5(a) gives a view on the solder bumps on the SOI substrate prior to flip-chipping. Figure 4.5(b) shows the attached laser diode. In [13, 14], InGaAs photodetectors were integrated onto a large-core SOI substrate. There are several ways to couple light between to the SOI waveguide and the integrated detector. A grating or a tilted mirror can be etched into the waveguide to vertically couple out the light into the detector on top of it. Another possibility is to butt-coupled waveguide and detector by mounting the detector into a recess etched into the SOI substrate. Optical coupling approaches will be discussed in detail in paragraph 4.7.

Hybrid integration has some advantages. Flip-chip integration is a relatively mature and reliable process. The active and passive devices can be independently optimized and fabricated. Testing of the devices can be done before integration so that only good working optoelectronic components can be selected. The main drawback of this approach is that the integration is not carried out on a wafer scale level, it is a sequential process of integrating single PD dies (or PD array dies). The alignment of these detectors is critical resulting in a time consuming and costly process. Using a larger detection area will decrease the necessary alignment accuracy but can increase the intrinsic capacitance of the device which might be a limiting factor in high speed applications. In an attempt to overcome the high alignment accuracy needed during pick-and-place, alignment structures (recess, standoffs, ...) can be etched and one can make use of the surface ten-



(a) Sputtered bumps after reflow

(b) A laser die flip-chipped onto the silicon substrate. It emits into the waveguide in front

Figure 4.5: Hybrid integration of a laser diode coupled to an SOI waveguide. Taken from [11]

sion of molten solder bumps [12]. Other drawbacks of this approach are the potentially large coupling loss between the flip-chipped detectors and waveguides and the limited integration density which is determined by the size of the individual discrete detectors or the pitch between detectors in an array.

4.3.2 Heteroepitaxial growth

A different integration approach is the epitaxial growth of III-V materials directly onto the silicon (waveguide) substrate. However, due to large lattice constant mismatch (InP/Si 8.1% mismatch), differing thermal expansion coefficients of III-V compound semiconductors and Si as well as polar-on-nonpolar growth, heteroepitaxial growth will lead to large strain and high misfit dislocation densities, thereby reducing the optical quality of the layers and the performance and reliability of the detector [15]. Much research effort has been spent on different techniques to overcome these problems such as epitaxial lateral overgrowth (ELO) [16], the use of an intermediate buffer ceramic layer [17] and the use of GaAs buffer layers and quantum dot layers [18].

The integration of epitaxially grown InGaAs detectors on silicon has been limited to top-illuminated devices (from a vertical mounted fiber or free-space) [19, 20]. This research was mainly driven by the opportunity to closely integrate these detectors with silicon read-out electronics. As far as we know, no SOI waveguide coupled III-V detectors have been demon-

strated by means of heteroepitaxial growth. This is due to the bad InGaAs material quality and the need for relatively thick buffer layers or advanced growth techniques.

Although the growth of InGaAs layers on silicon has proven to be extremely difficult, successful results have been published in recent years on heteroepitaxial integrated germanium (Ge) detectors onto SOI waveguides. High quality germanium layers have been grown on silicon without the need for thick buffer layers resulting in highly efficient waveguide coupled photodetectors. An overview of Ge-on-SOI detectors will be given in paragraph 4.8. The advantage of epitaxially grown detectors is that these can be fabricated on wafer scale and lithographically aligned to the underlying waveguides.

4.3.3 Bonding of unprocessed III-V dies or wafers

A third method is the heterogeneous integration based on die-to-wafer bonding. This integration method is shown in figure 4.6. It consists of bonding several unprocessed III-V dies (epitaxial layers facing the silicon waveguide substrate) onto a processed SOI wafer. Different bonding methods are possible and will be discussed briefly in the next paragraph. The bonding itself is the only non-wafer scale process within the integration procedure but because the dies are unprocessed, the alignment accuracy required for this step is limited, typically $> 100\mu$m, so a rapid pick-and-place routine can be used. After bonding, the III-V semiconductor substrates are removed (InP substrates in this work), obtaining defect-free epitaxial thin films bonded onto an SOI waveguide wafer. The substrate removal is typically done using a combination of mechanical grinding and chemical etching down to an etch-stop layer. Subsequently, all photodetectors are defined simultaneously using wafer scale processes and lithographically aligned to the underlying SOI waveguides.

Heterogeneous integration based on die-to-wafer bonding combines the advantages of both hybrid integration and heteroepitaxial growth. On one hand, it allows obtaining high quality, defect free epitaxial III-V layers on silicon and on the other hand, a very high device density can be achieved making use of wafer scale processing. In this work, die-to-wafer bonding is studied in more detail and using this technology, we designed and fabricated high efficient InGaAs photodetectors coupled to SOI waveguides. This will be discussed in chapter 5.

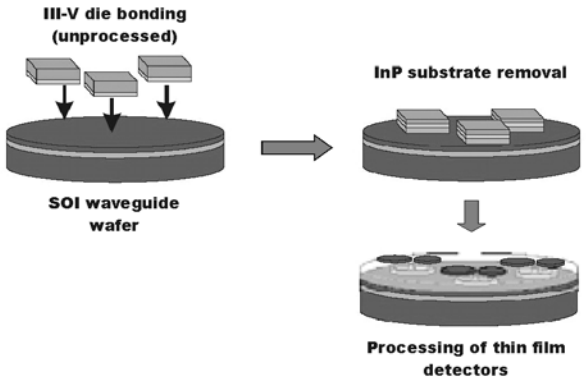


Figure 4.6: Heterogeneous integration based on bonding of unprocessed III-V dies onto an SOI waveguide wafer. After die-to-wafer bonding, the InP substrate is removed and InGaAs detectors are processed making use of wafer scale lithographical techniques

4.3.4 Conclusion

In this section, we reviewed different methods for integrating III-V active optical devices and more specific InP/InGaAs photodetectors on SOI waveguides. We mentioned that the heteroepitaxial growth of III-V on silicon has proven to be extremely difficult but that this technique is nowadays successfully employed for the integration of Ge photodetectors.

Hybrid integration of pre-processed photodetectors based on mature flip-chip technology can be an attractive route for relatively low volume manufacturing in which a large integration density is not needed. However, reaching the required alignment accuracy can be challenging and could result in a cost-ineffective process, especially for larger device densities. Moreover, the interface between waveguides and detectors can potentially exhibit large optical losses.

Integration based on bonding of unprocessed III-V dies offers the potential of very high density integration using wafer scale compatible processing and lithographical alignment. Moreover, this integration techniques allows to transfer a defect-free III-V epitaxial layer on silicon. When using sub-micron thick transparent bonding layers, evanescent, loss-free coupling between waveguides and active devices such as detectors becomes possible.

Table 4.2 summarizes these three different heterogeneous integration approaches with their advantages and disadvantages.

	Hybrid integration	**Heteroepitaxial growth**	**Bonding of unprocessed III-V**
Testing before device integration	**Yes**	No	No
Integration density	Low	High	**High**
Wafer scale processing of active devices	No	Yes	**Yes**
Lithographical alignment of active devices onto waveguides	No	Yes	**Yes**
III-V material quality after integration	High	Low	High
Main technological challenge	**Relatively mature** Alignment accuracy	Material quality	Yield of bonding
InP substrate	Present or (partially) removed	-	Removed
III-V fabrication	Before integration	After integration	After integration
Intermediate bonding material	Metal or adhesive	Buffer layer	Adhesive, oxide or none
Thickness	order 10μm	order nm to μm	order nm to μm

Table 4.2: Comparison between different III-V/Si integration technologies. Some important advantages of hybrid integration and bonding are highlighted

4.4 Die-to-wafer bonding

4.4.1 Introduction

For the bonding of unprocessed III-V dies onto the SOI waveguide substrate, different bonding approaches are possible. As an optical transparent bonding layer is necessary, eutectic or metal bonding [21] can be excluded. The two main candidates for this application are direct wafer bonding with [22, 23] or without [24–26] an intermediate SiO_2 layer and adhesive bonding [27, 28]. We believe adhesive bonding offers some important advantages as compared to direct bonding. Direct bonding is based on Van der Waals attraction forces. This requires a very intimate contact between the surfaces that have to be mated, imposing more severe requirements on flatness, microroughness, cleanliness and chemistry of these surfaces. Using an adhesive as bonding agent (e.g. a polymer, photoresist, polyimide, spin-on-glass) reduces these problems as the spin-coated adhesive planarizes the wafer surface prior to bonding and can compensate for inclusions of small particles between die and wafer.

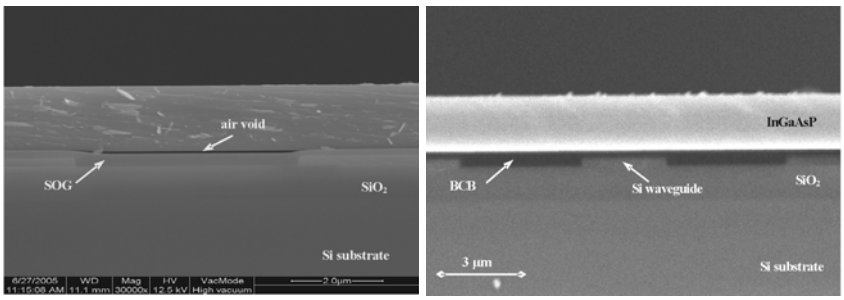
Adhesive bonding is usually performed at relatively low temperatures ($<$450°C). Among different types of adhesives suitable for bonding, BCB

(benzocyclobutene) is often chosen because of its excellent properties: low temperature cure, low moisture absorption, no out-gassing, good planarization, low shrinkage upon cure, high glass transition temperature, ... This results in a high bonding quality and bonding strength [28, 29]. BCB is a heat curable oligomer from Dow Chemicals. It is highly transparent for wavelengths from 450nm to 1550nm [30] and it can be spin coated in a large thickness range from 1μm to 25μm [29]. BCB bonding is well known, clearly described in literature [28, 31, 32] and often used for MEMS (micro electro-mechanical systems) applications. The Photonics Research Group of UGent/IMEC did pioneering research on BCB bonding for photonic applications. The bonding process was developed during the PhD research of I. Christiaens [32] and G. Roelkens [33].

As will be explained later, a thin ($<$300nm) intermediate bonding layer is needed to obtain efficient evanescent coupling between the SOI waveguide and the III-V active device. These layer thicknesses cannot be achieved using commercially available BCB. Spin-on-glass (SOG) on the other hand, which is often used in the electronics industry as interlevel dielectric material, can be spin coated in very thin layers ($\sim$100nm). It also has a higher thermal conductivity (k =0.5W/mK) as compared to BCB (k =0.3W/mK). In [34], the authors used SOG for GaAs on Si wafer-to-wafer bonding. In these experiments, two un-patterned 3-inch wafers were successfully bonded using a 300nm intermediate SOG layer.

4.4.2 Spin-on glass die-to-wafer bonding

For our experiments, we used Accuglass® T-11 from Honeywell. This is a methylsiloxane type of SOG and can be spin coated in thicknesses ranging from 100nm to 400nm. The bonding procedure started with sample cleaning. The unpatterned InP epi-wafer was cleaved into 0.5cm by 0.5cm dies and then cleaned. These dies were bonded both on unprocessed Si samples and structured SOI samples. After spin coating SOG on the Si/SOI samples, they were placed on a hot plate at 150°C for 5 minutes to remove solvents. Then, after cooling down, the InP dies were manually bonded at room temperature. To increase bonding strength, samples were cured in nitrogen ambient for 2 hours at 300°C. After substrate removal, we obtained an epitaxial III-V film bonded on a Si sample without any delamination or interfacial voids. Although we obtained good quality and reproducible bonding on blank Si samples with SOG layer thicknesses down to 100nm, the bonding on structured SOI samples was less successful. Figure 4.7(a) is an SEM cross-section of an InGaAsP epitaxial film (after substrate removal) bonded on a patterned SOI sample. Two silicon waveguides with a



(a) SOG bonded sample (b) BCB bonded sample

Figure 4.7: SEM cross-section of a InGaAsP film (after substrate removal) bonded onto a SOI waveguide substrate

height of 220nm and a spacing of 5μm are clearly visible. The bad planarizing properties of SOG give rise to air voids at the SOG/InGaAsP interface. These weak, unbonded parts of the III-V film tend to crack or delaminate during substrate removal, resulting in a bonding process with a low yield and a bad reproducibility. Planarizing the SOI surface prior to bonding (by means of CMP for example) could possibly solve these problems however, this was not assessed in this work.

A second option to obtain a thin intermediate bonding layer was proposed by G. Roelkens [35]. By diluting the commercially available BCB with mesitylene, bonding of III-V dies on patterned SOI wafers using submicron thick bonding layers was demonstrated. This is the subject of the next section and the method being finally used during this work.

4.4.3 BCB die-to-wafer bonding

Figure 4.7(b) is another cross-section of a bonded InGaAsP film but this time, BCB is used as bonding layer. When comparing the cross-section of the SOG and the BCB bonded sample, it is clear that the planarization of the SOI topography is better when using BCB as a bonding agent. The topography of the SOI samples and the bonding layer thickness in both figures are equal. Due to the better planarization properties among others, BCB bonding of III-V dies on structured SOI substrates has a much higher yield as compared to SOG bonding.

In recent years, the Photonics Research Group of UGent/IMEC has built quite some expertise in the field of III-V/Si heterogeneous integration using BCB bonding [36–39]. The development and optimization of

the die-to-wafer bonding process using both commercially available BCB for thick bonding layers ($>1\mu$m) and diluted BCB for sub-micron bonding layers is described in the PhD thesis of G. Roelkens [33]. Detailed information on bonding technology, development and characterization can be found there. In this work, we optimized the bonding process to reach sub-300nm and even sub-100nm bonding layer thicknesses to allow for evanescent coupling between the active III-V devices and the silicon waveguides. For these very thin BCB bonding layers, the two main points of attention are first of all sample cleaning and secondly, the planarization of the 220nm high topography of the SOI sample. A brief overview of the bonding procedure is given below.

4.4.3.1 Cleaning and sample preparation

A first step in the bonding procedure is the sample preparation. An InP epiwafer is cleaved in square dies with a size ranging from 3×3 to 10×10mm^2. The patterned SOI wafer (without an oxide top cladding) is cleaved into larger samples, with a typical size of a few square centimeters. A crucial step in achieving a high quality bond, especially when using very thin bonding layers as described here, is sample cleaning. Different kinds of contamination and particles are present on the surfaces of the dies. Especially during the cleaving of the samples, many particles are generated. Cleaning and avoiding particles and contamination afterwards is very important in order to obtain a reproducible and high yield bonding. We cleaned the SOI samples using an aceton-IPA-DI solvent clean followed by a Standard Clean 1 (SC-1) for 10-15 minutes. The SC-1 solution of ammonium hydroxide and hydrogen peroxide ($NH_4OH/H_2O_2/H_2O$ 1:1:5) removes organic surface contamination and has shown to be an efficient particle removing agent [40]. The cleaning takes place at a temperature of 75-80°C in a teflon beaker to avoid contamination from ordinary glass.

The most effective way to clean the surface and to remove the particles from the InP dies consists of etching away a protective InP cap layer. This InP layer (typically 50nm) is grown onto an InGaAs layer, which can be a functional layer in the stack (e.g. an absorbing layer in the case of an MSM photodetector) or a sacrificial layer that also needs to be removed. The InP cap layer is selectively removed over the InGaAs layer by means of wet etching in a H_3PO_4/HCl (7:3) solution. During the removal of the cap layer, particles which were present on the InP die surface are lifted-off.

After these cleaning steps, the samples are rinsed with DI water and placed onto a hotplate at 150°C for $\sim$5 minutes for drying. It is very important at this stage to avoid redeposition of particles and contamination.

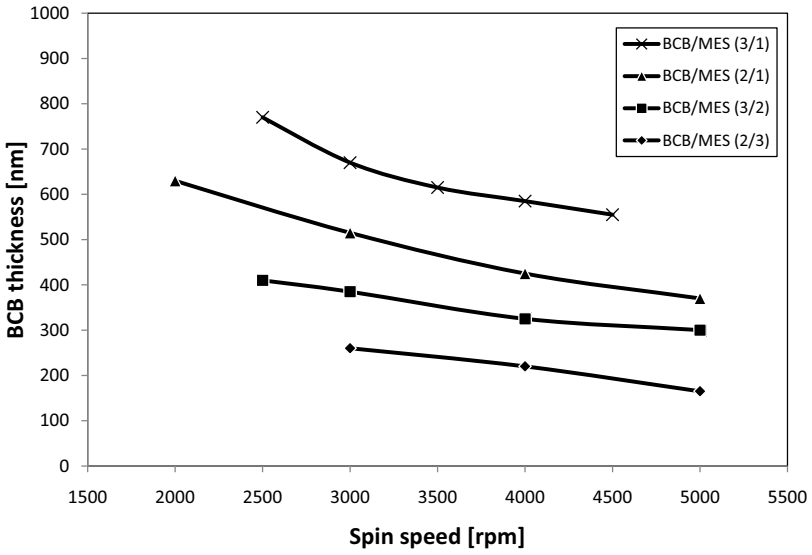


Figure 4.8: Thickness of BCB (after cure) versus spin speed for different CYCLOTENE 3022-35:mesitylene dilutions. Spin time was 40s

This can be achieved by minimizing the time and the number of operations/movements between sample cleaning and bonding. Al our experiments have been carried out in a class 100 cleanroom environment.

4.4.3.2 BCB deposition

After sample preparation and cleaning, a layer of BCB is deposited directly on the SOI sample by spin coating. As mentioned before, commercial BCB is diluted by adding mesitylene to obtain the required bonding layer thickness. Figure 4.8 shows the thickness of a cured BCB film, spun on an unpatterned Si substrate. The BCB used here is CYCLOTENE 3022-35. Without the addition of mesitylene, a 1μm thick layer is obtained for spin speeds of 5000rpm. Spinning BCB:MES(2:3) at 5000rpm during 40s results in a $\sim$150nm thick cured film on a blank Si sample. We used this combination of dilution and spin speed for most of our bonded InGaAs-on-SOI photodetectors. Because we apply a pressure on the III-V die during bonding, the thickness of the BCB layer in between silicon waveguide and the III-V film is further reduced to $\sim$100nm.

4.4.3.3 Pre-bake, bonding and curing

Spin coating already evaporates most of the mesitylene solvent. After spin coating, the SOI sample is placed on a hot plate at 150°C for 1 minute to evaporate the remaining solvents. At 150°C, BCB has it lowest viscosity and this allows the BCB to partially planarize the SOI topography. The bonding is carried out manually using tweezers. When handling the dies during the bonding process, care should be taken in order not to contaminate or damage the surfaces that have to be bonded. This is possible by contacting only the flanks or the backside of the InP dies during handling. This can be done using teflon and vacuum tweezers.

The InP die is bonded while the SOI sample is still on the 150°C hotplate. After 1 minute solvent evaporation at a temperature of 150°C, the BCB is still liquid and has a low viscosity. By manually applying pressure on the InP die, we are able to completely planarize the SOI topography. The trenches are completely filled without the creation of interfacial voids and at the same time, the thickness of the BCB layer between silicon waveguide and III-V die can be very thin. Using BCB:MES(2:3) at 5000rpm, we obtain a $\sim$100nm layer of BCB in between waveguide and III-V film. For stronger diluted mixtures, bonding layer thicknesses down to 50nm have been obtained. After bonding, it is possible that there is an accumulation of BCB at the edges of the sample. This can be removed by dispensing mesitylene on the sample followed by spin-drying. If not removed, these pile ups can give rise to problems during processing of the III-V film afterwards.

After coating, pre-bake and bonding, the BCB film cured in order to obtain its final properties. We used a standard hard cure as described in the CYCLOTENE processing procedures [29]. The sample is put on a hotplate, at a temperature of 250°C for 1h. This results in a degree of polymerization which is higher than 95%. The temperature was ramped from 150°C to 250°C at a rate of 1.6°C/min. Curing is done in a nitrogen environment in order to avoid oxidation of the BCB. During cure, there is no out-gassing and the BCB has a very low shrinkage, which avoids the formation of voids.

4.4.3.4 InP substrate removal

The III-V dies have a total thickness of $\sim$350μm. First of all, the substrate is mechanically grinded down to a thickness of $\sim$ 60μm. The last tens of micrometers are chemically etched using diluted hydrochloric acid. HCl:H_2O (3:1) etches InP quite fast ($\sim$ 1μm/min) and stops on the InGaAs etch-stop layer. Due to the anisotropical etching of InP in HCl, triangular ridges of InP will remain on two of the four sides of the III-V die. The height of these ridges is comparable to the III-V thickness obtained after

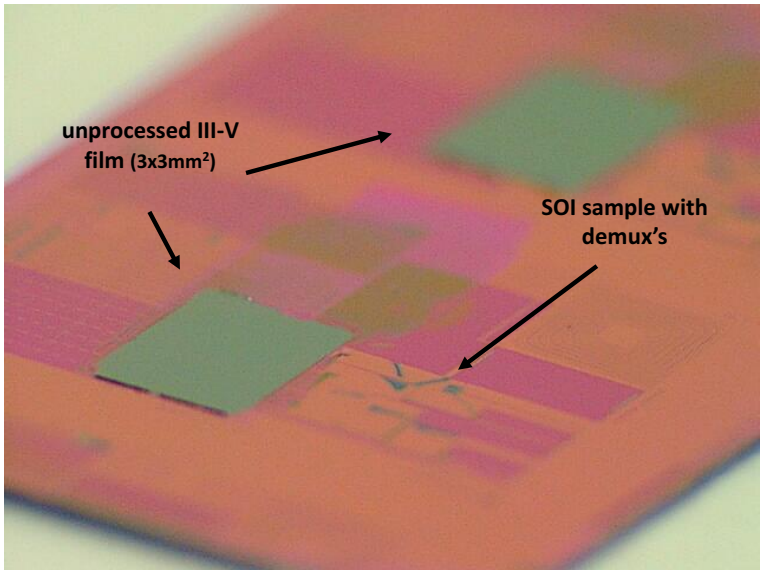


Figure 4.9: Two unprocessed BCB bonded InP-based epitaxial layers ($3\times3\text{mm}^2$) on top of an SOI substrate

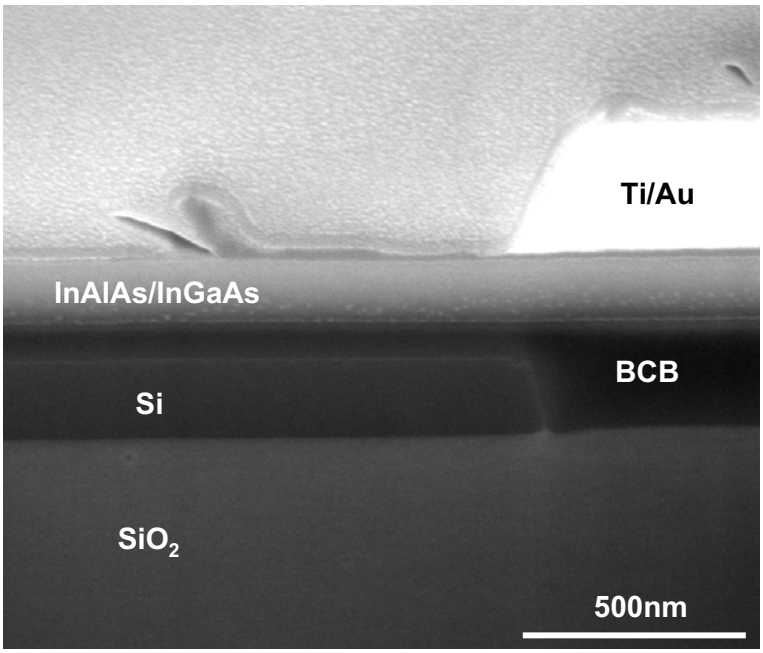


Figure 4.10: Cross-section SEM picture of a III-V film (after substrate removal) bonded on SOI using a 100nm BCB layer

grinding and is typically up to $\sim$60μm. To avoid problems during the next lithography steps, these ridges were manually removed. Another option to remove those ridges, which was not studied in this work, is to make use of an isotropical etch solution. As this solution (e.g. HNO_3:HCl) [33] is not selective for InP and InGaAs, the III-V film has to be protected with photoresist during etching, thereby only exposing the ridges.

4.4.3.5 Multiple die-to-wafer bonding

We also demonstrated multiple die-to-wafer bonding. Figure 4.9 is a picture of two 3$\times$3mm^2 III-V films bonded on an SOI sample. After bonding and curing, the two InP substrates were simultaneously removed by grinding and etching. Figure 4.10 is a SEM cross-section of a III-V film, after removal of the InP substrate and etch-stop layers. The III-V stack has a thickness of only 205nm and is bonded using a 100nm BCB layer.

4.4.3.6 Yield and reproducibility

During this work, we performed hundreds of bonding experiments, both for device processing and bonding optimization. From these experiments, we can conclude that for the bonding of single 3$\times$3mm^2 InP epi-dies on SOI using a 100nm thick intermediate BCB layer, we obtained a yield of 75%. Here, we define the yield as the percentage of dies for which the bonding is perfect over the complete surface of the die. This means that for three out of four bondings we performed, we obtained a perfect III-V film after substrate removal without any delaminations and cracks.

Bonding InP dies on transparent pyrex samples allows us to visually inspect the bonding interface and to analyze what causes delaminations. It turns out that the three main causes of delamination are (not necessarily in this order) particle inclusion, trapped air bubbles and puncturing of the BCB layer.

Particle inclusions As mentioned before, very thin bonding layers are much more sensitive to particles present on the sample surfaces as compared to thick bonding layers. This is because a bonding layer will be able to accommodate a particle as long as the diameter of the particle is smaller as compared to the bonding layer thickness. Large particles pinned on the surface give rise to unbonded areas which will finally delaminate during substrate removal.

Although bonding experiments are done in a class 100 cleanroom environment, particles will always be present. After cleaning, airborne par-

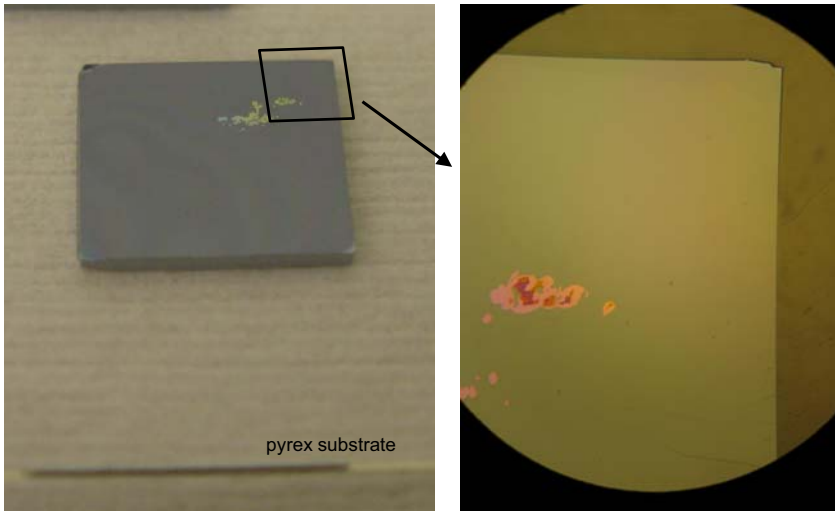


Figure 4.11: Photographs of an InP die (0.5 $\times$ 0.5 cm^2) bonded on a pyrex substrate. Pictures are taken from the backside, through the pyrex substrate to visualize the quality of the bonding interface. Some air inclusions are visible on the top right corner

ticles can fall on the sample surfaces. Also, during handling, samples can get contaminated and particles can be generated. To minimize the particles and contamination during these steps, care should be taken during handling, thereby never touching the surfaces that have to be bonded. Also, the time and the number of handlings should be minimized between sample cleaning and bonding.

The cleaning methods as described above effectively remove particles which are present on the sample surfaces. However, depending on the quality, epitaxial III-V wafers often have particles that are incorporated in the layer stack during epitaxial growth. These cannot be removed by standard cleaning methods and these parts of the wafers have to be identified and trashed before bonding.

Air inclusions A second cause of film delamination is the inclusion of air bubbles. Figure 4.11 shows two photographs of a 5$\times$5mm^2 InP die bonding onto a pyrex substrate. By looking through the pyrex substrate, the bonding interface becomes visible. On the top right corner of the die, some air inclusions are clearly visible. During substrate removal and subsequent processing of the III-V film, these parts of the film will delaminate.

As the bonding is not carried out in a vacuum environment, the inclu-

sion of small air bubbles as shown in figure 4.11 is difficult to control and to avoid. However, by applying pressure on the sample during bonding while the BCB has a low viscosity, larger air bubbles can be easily squeezed out. Carrying out this bonding on a (semi-)automated setup in a vacuum environment could solve this problem by avoiding the creation of interfacial air bubbles and voids.

Puncturing of the BCB layer When applying a too large and non-uniform pressure during bonding, the very thin BCB layer can get punctured. In this case, a part of the edge of the InP die directly touches the SOI substrate, thereby locally reducing the thickness of the BCB layer down to a few nanometers. Although this does not necessarily lead to large delaminated areas, this problem demonstrates that manual bonding results does not allow to obtain a reproducible bonding layer thickness. In [33], this problem was solved by partially curing the BCB layer before bonding. This increases the rigidity of the bonding layer and avoids puncturing during bonding. However, to reach bonding layer thicknesses in the order of 100nm, this approach is not possible. In this case, the 220nm high topography can only be planarized if the BCB is still liquid so it can reflow to fill the trenches by applying pressure.

4.4.4 Conclusion

In the previous section, we described a bonding process that allows to obtain epitaxial III-V films on an SOI substrate with a very thin intermediate BCB bonding layer. Using a BCB:MES(2:3) diluted mixture, spun at 5000rpm, we obtained a 100nm BCB layer between the silicon waveguide and the III-V film, without the need for planarizing the SOI before bonding. By manually applying pressure on the InP die during bonding, the BCB (which is still liquid) reflows and completely planarizes the 220nm high topography of the SOI sample. By making use of stronger diluted mixtures, bonding layer thicknesses down to 50nm have been obtained. During this work, many hundreds of bondings have been performed and from this, we conclude that the bonding of $3\times3\text{mm}^2$ InP dies on patterned SOI samples using a 100nm thin bonding layer has a yield of $\sim$75%. To demonstrate the high quality of the bonded III-V films, we processed arrays of up to one hundred waveguide coupled InGaAs photodetectors on a pitch of 25μm without any failure. This will be described in chapter 5 and 6. In recent years, results on a wide range of active devices bonded on SOI have been published by the Photonics Research Group of UGent/IMEC: lasers [41, 42], PIN detectors [42–44], MSM detectors [37, 45], resonant detec-

tors [46], cavities [47], microdisk lasers [48–50], modulators [49], WDM receivers [51] and multiwavelength lasers [50]. Most of these devices rely on evanescent coupling by making use of a very thin BCB bonding layer.

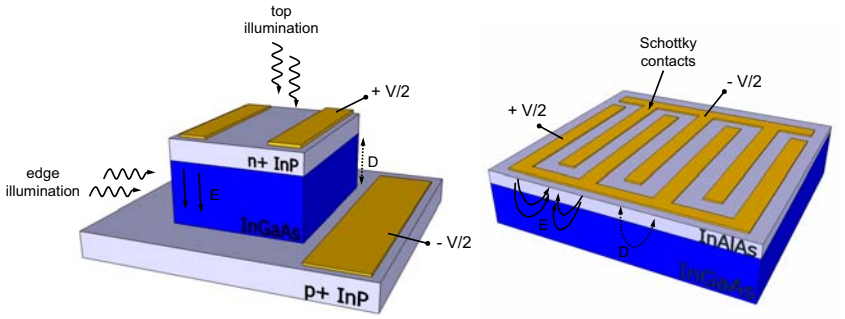
As mentioned above, the bonding procedure is fully manual and carried out on a sample scale, in ambient air. This manual procedure results in a low reproducibility of the bonding layer thickness and a limited alignment accuracy. We believe that these issues can be solved by making use of a (semi-)automated tool in which the sample attachment and bonding is done in a vacuum environment, applying a well controlled pressure. Moreover, this way, puncturing of the BCB layer and trapping of air bubbles can be avoided.

Most of our bonding experiments have been carried out on a sample scale in which a single (or a few) InP dies were bonded onto a larger SOI sample. However, the ultimate goal of heterogeneous integration based on die-to-wafer bonding is to obtain a 200mm SOI wafer on which multiple III-V thin films are bonded. In a next step, the active devices can be simultaneously processed, on a 200mm wafer scale and lithographically aligned to the underlying SOI waveguides. One integration method to achieve this goal is by aligning and temporary bonding multiple III-V dies (epitaxial layers facing up) on a carrier wafer using a flip-chip bonder. For this, e.g. thermal release tape could be used. Again, as the dies are not processed, a strict alignment is not needed and a fast pick and place procedure can be used. After collective cleaning the populated carrier wafer and an SOI waveguide wafer, BCB can be applied and both wafers can be bonded in a (semi-)automated wafer bonder. After curing, the carrier wafer can be released and subsequent substrate removal and III-V processing can be carried out on an SOI wafer-scale. This topic was not studied in this work, but is the subject of the PhD research of Stevan Stankovic.

4.5 Different types of photodetectors

In the first part of this chapter, we focused on different technologies for heterogeneous integration of semiconductors that are suitable for NIR photodetection on a SOI waveguide substrate. The following part of the chapter is about the design of the detector itself. Which types of photodetectors are commonly used? What is their performance? How can we efficiently couple light from the SOI waveguide in the detector? These question will be answered and an overview of the state-of-the-art will also be given in the following part of this chapter.

The most commonly used photodetectors are p-i-n diodes (PIN) and interdigitated metal-semiconductor-metal (MSM) Schottky barrier diodes as



(a) PIN detector (b) MSM detector

Figure 4.12: Simplified schematic layout of typical PIN and MSM detectors in the InP/InGaAs material system. Bias voltages V, Electric field lines E and carrier transit lengths D are also shown

shown in figure 4.12. These structures utilize an absorbing layer to generate electron-hole pairs and electrode materials to apply an electric field across the absorbing layer to separate and collect the electron and holes in order to create a photocurrent. The electrode materials are doped semiconductors in the PIN case and Schottky metals in the case of an MSM detector. Other types of detectors, which are intended to operate with internal gain include avalanche detectors, photoconductors and phototransistors.

4.5.1 PIN detectors

The PIN photodiode is one of the most common photodetectors. It consists of a PN junction separated by an intermediate, undoped absorbing layer as can be seen in figure 4.12(a). This is a heterojunction detector with an InGaAs absorbing layer and transparent P- and N-doped InP cladding layers. A highly P-doped InGaAs contact layer (which is not shown) is usually inserted in between the P-type contact and the P-InP cladding layer. The band diagram under reverse bias conditions is shown in figure 4.13. Even without an external bias voltage, an electric field which separates the photogenerated electron-hole pairs is present in the intrinsic region due to the alignment of the Fermi levels of the P- and N-doped regions ($E_{F,P}$ and $E_{F,N}$ respectively.

The I/V characteristics of a PIN photodetector are also shown in figure 4.13. When the detector is not illuminated, the current is given by the well-know Shockley equation which predicts a low leakage current for inverse bias voltages and an exponential increase for forward bias voltages. When

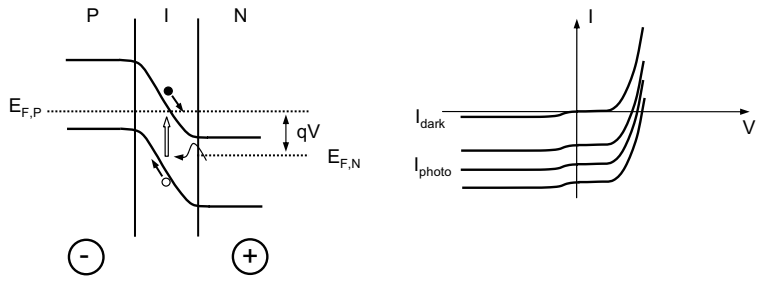


Figure 4.13: Schematic representation of the band diagram and I/V characteristics of a PIN photodetector

illuminated, the characteristics shift by a constant current I_{photo}, which is proportional to the incident optical power.

In normal operation conditions, PIN photodiodes are reversely biased with a relatively large bias voltage. This minimizes the carrier transit time across the intrinsic region, completely depletes the region where absorption occurs and results in a photocurrent which is (in approximation) not dependent on small bias voltage variations. For a detailed description of the current mechanisms in PIN devices, we refer to [52].

4.5.2 MSM detectors

A metal-semiconductor-metal (MSM) detector as shown in figure 4.12(b) consists of an absorbing semiconductor layer on which two interdigitated electrodes have been deposited to form back-to-back contacted Schottky diodes. MSM detectors have some advantages. Due to their planar structure and coplanar Schottky contacts, the device is easier to fabricate and has a lower capacitance per unit area as compared to PIN detectors. Due to their low capacitance, MSM detectors can have a very high bandwidth, and thus, are excellent candidates for high-speed optical receivers (see chapter 5). A disadvantage as compared to PIN detectors is the electrode shadowing that results in a poor responsivity of vertical illuminated devices. However, this can be solved by back-illumination, the use of transparent Schottky contacts or waveguide integrated MSM detectors as will be explained in detail in chapter 5.

The one-dimensional approximated band diagram and the typical I/V characteristics are presented in figure 4.14. When the two back-to-back Schottky diodes are not biased, the MSM structure is symmetrical and the electric field in the center is zero. The photoexcited electrons are trapped in

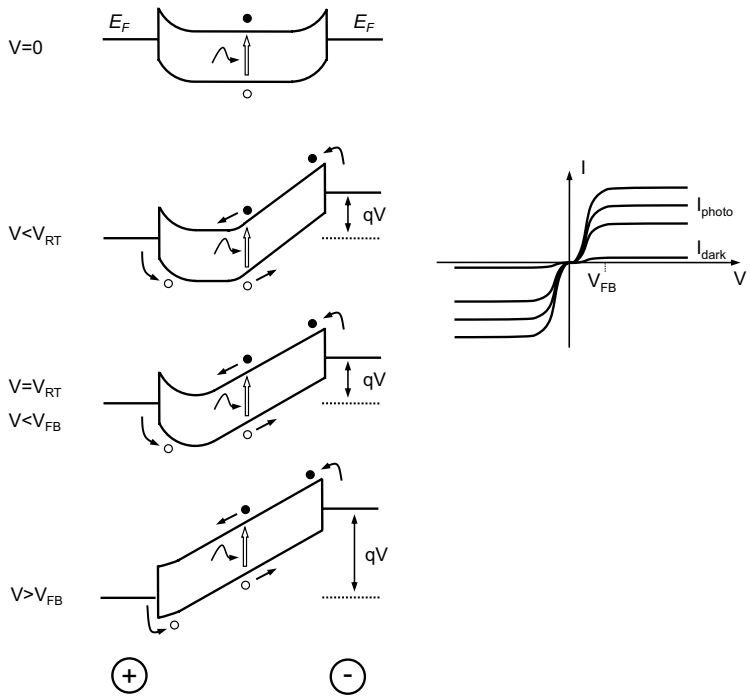


Figure 4.14: Schematic representation of the band diagram and I/V characteristics of an MSM photodetector

the potential well and the photocurrent is zero. When a positive voltage is applied to the left contact with respect to the right contact as shown in figure 4.14, the left Schottky diode is forward biased, the right one is reversely biased, the sum of the depletion widths at both contacts increases with increasing voltages and an electric field is present between the electrodes. Due to the remaining potential barrier at the forward biased electrode, the majority of the photoexcited electrons is trapped in the potential well. The photoexcited holes cannot leave the active region due to the charge of the trapped electrons. The photocurrent is very small. At a certain voltage, called the reach-through voltage V_{RT}, the two depletion regions at the two contacts touch each other and the structure is entirely depleted. The electric field will be continuous and will vary linearly between the contacts while going through zero somewhere in between. As the voltage increases further, a point is reached at which the electric field at the forward biased Schottky contact (left contact in figure 4.14) becomes zero and the energy band becomes flat. This is the flat-band condition with the corresponding flat-band voltage V_{FB}. At this point, the potential barrier for the generated electrons disappears, the electric field has the same direction over the entire structure and the photocurrent saturates. The flat-band voltage is given by

$$V_{FB} = \frac{qN_dL^2}{2\epsilon} \tag{4.4}$$

where q is the elementary charge, N_d the doping level, ϵ the permittivity of the semiconductor and L the electrode spacing [53].

As the MSM structure is symmetric, the I/V characteristics are also symmetric as can be seen in figure 4.14. The dark current of an MSM detector is mainly determined by the electron and hole Schottky barrier height. The Schottky barrier height on InGaAs(n-) is very low (approximately 0.2eV). This means that direct deposition of the electrode on the InGaAs absorption layer would result in an excessive dark current. To solve this, a thin layer of semiconductor material with a higher barrier height is grown on top of the InGaAs absorption layer as can be seen in figure 4.12(b). This layer is called a Schottky barrier enhancement layer (SBEL) and will be discussed in detail in chapter 5

For a detailed description of the current mechanisms in MSM devices, we refer to [53, 54].

4.6 Detector performance criteria

Responsivity and quantum efficiency The PIN and MSM detector in figure 4.12 can be illuminated either perpendicular (top or bottom illuminated) or parallel (edge illumination) to the absorber/electrode interface. As these photodetectors are intended to operate without internal gain, the photocurrent I_{photo} in milliamperes generated by an incident optical power $P_{incident}$ in milliwats can be written as:

$$\begin{aligned} I_{photo} &= q \frac{\sharp \text{ collected electron-hole pairs}}{\Delta t} \\ &= q\,\eta \frac{\sharp \text{ incident photons}}{\Delta t} \\ &= \eta \frac{q}{h\nu} P_{incident} = \eta \frac{q\lambda}{hc} P_{incident} \\ &= \eta \frac{\lambda[\mu m]}{1.24} P_{incident} \end{aligned} \tag{4.5}$$

where q is the elementary charge, ν is the frequency of the light, λ is the optical wavelength in micrometers, h is Planck's constant, c is the speed of light in vacuum and $P_{incident}$ is the incident optical power in milliwatts.

The quantum efficiency η is the number of electron-hole pairs generated per incident photon that contribute to the photocurrent and can we written as:

$$\begin{aligned} \eta &= \frac{\sharp \text{ collected e-h pairs}}{\sharp \text{ incident photons}} \\ &= \frac{I_{photo}}{q} \frac{h\nu}{P_{incident}} \end{aligned} \tag{4.6}$$

The quantum efficiency depends both on the optical and electrical performance of the detector. From an optical point of view, the ratio between absorbed and incident photons should be as large as possible. A good electrical behavior means that most of the generated carriers are collected by the contacts without being lost (by recombination for example). A related figure of merit is the responsivity, which is the ratio of the photocurrent to the optical power:

$$R = \frac{I_{photo}}{P_{incident}} = \eta \frac{q}{h\nu} = \eta \frac{\lambda[\mu m]}{1.24} \text{ A/W} \tag{4.7}$$

Therefore, for a given quantum efficiency, the responsivity increases linearly with wavelength. For an ideal photodetector ($\eta = 1$), $R = \lambda/1.24$ [A/W], where λ is expressed in micrometer.

The quantum efficiency η, for discrete detectors which are top- or bottom illuminated, is typically determined by the thickness D and the absorption coefficient α of the absorbing layer. In absence of reflections, the quantum efficiency is:

$$\eta = 1 - e^{-\alpha D} \tag{4.8}$$

For example, for a typical absorption of $\alpha = 1\mu m^{-1}$, an absorber thickness $L > 1\mu m$ is needed to obtain quantum efficiencies above 63%.

Dark current The dark current is the leakage current that flows when the photodetector is not illuminated and a (reverse) bias voltage is applied. The dark current is temperature dependent and generates shot noise. Next to thermal noise, shot noise is a fundamental noise mechanism responsible for current fluctuations in optical receivers. Thermal noise is generated by the load resistor in the front end of an optical receiver. Shot noise on the other hand is a manifestation of the fact that an electric current consists of a stream of electrons that are generated at random times [9]. If we only consider shot noise, then the current generated by the detector in response to a constant optical signal can be written as:

$$I(t) = I_{photo} + i_{shot}(t) \tag{4.9}$$

where $I_{photo} = RP_{inc}$ is the average photocurrent with R being the detector responsivity and P_{inc} the incident optical power and $i_{shot}(t)$ is the current fluctuation related to shot noise. We can write the shot noise variance as [9]:

$$\sigma_{shot} =< i_{shot}^2(t) >= 2q(I_{photo} + I_{dark})\Delta f \tag{4.10}$$

Here q is the electron charge and Δf is the effective noise bandwidth of the receiver.

The shot noise might be a limiting factor of the signal-to-noise ratio (SNR) of a receiver. For a more detailed analysis, we refer to [9] and [52]. In any way, the dark current should be kept as low as possible in order to reduce the shot noise as much as possible. This will increase the SNR and sensitivity of receivers for which shot-noise is the most important contribution to the total noise in the system.

Bandwidth and response speed For certain applications like high speed data transmission, a large detector bandwidth is necessary. The bandwidth of a photodetector is determined by the speed with which it responds to variations in the incident optical power. The main factors which limit the speed of response are the RC time constant of the detector and load and the transit time resulting from the drift of carriers across the depletion layer. The bandwidth will be determined by the slowest component. Also, care should be taken in order to avoid carrier generation in low electric field regions where the slow, diffusion limited transit time can reduce the detector bandwidth.

The bias voltage applied to the detectors of figure 4.12 should be sufficient in order to fully deplete the InGaAs absorbing layer and to avoid slow carrier diffusion. The capacitance of the detector can be reduced by increasing the distance D between the electrodes. This however will increase the carrier transit time as the carriers need to travel further before being collected at the electrodes. So there is a trade-off between detector capacitance and carrier transit time and an optimum value for the electrode spacing exists which maximizes the detector bandwidth.

If the detectors of figure 4.12 are vertically illuminated, there is another important trade-off. As explained previously, the detector quantum efficiency can be increased by increasing the InGaAs absorber thickness. In the case of both PIN and MSM detectors, the increased absorber thickness will result in carriers being generated further from the electrodes. So there is a trade-off between transit time limited bandwidth and quantum efficiency. For a typical material absorption of $0.5\mu\text{m}^{-1}$, a thickness $> 2\mu$m is necessary to obtain a high efficiency. This typically limits the electrical bandwidth to 15GHz as will be calculated in chapter 5. One way to avoid this trade-off consists of illuminating the detectors of figure 4.12 from the edge. This way, the optical absorption path is independent of the carrier transit length.

In chapter 5, we give a detailed analysis of the bandwidth of a heterogeneous integrated InGaAs-on-SOI detector which is edge-illuminated.

4.7 Coupling schemes

In this paragraph, we will discuss three interesting coupling approaches that can be used for the integration of near-IR photodetectors onto SOI waveguides. It is not our intention to give an exhaustive overview of the different configurations that exist to couple between dissimilar materials or geometries. A more general discussion on coupling mechanisms from a nanophotonic silicon waveguide to different types of materials added on

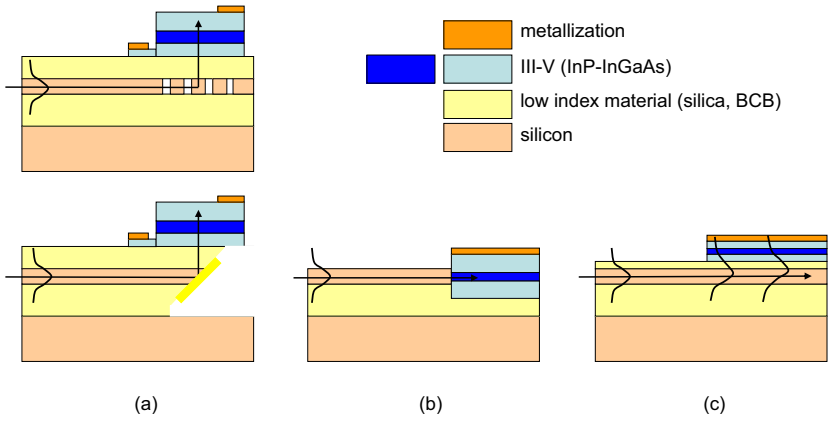


Figure 4.15: Overview of different coupling mechanisms between dissimilar materials: (a), vertical coupling, (b), butt-coupling and (c), evanescent coupling

top of these waveguides can be found here [55].

At this moment, the type of photodetector (PIN or MSM) and the semiconductor material (Ge or InGaAs) used in this detector are of no importance. However, it will become clear that from a technological point of view, certain integration techniques rule out certain coupling mechanisms. The coupling schemes that will be discussed are vertical coupling, butt-coupling and evanescent coupling. A schematic overview is given in figure 4.15.

Description of the simulation environment Each coupling scheme will be evaluated and studied by CAMFR simulations of simplified 2-D structures. This means that a photodetector is represented by a layer of InGaAs, no metal contacts are included and the silicon waveguide is a slab waveguide (no lateral confinement).

The SOI substrate consists of a 220nm thick silicon top layer on a 1μm thick buried silica layer on a silicon substrate. The TE-polarized fundamental slab mode will be excited from the left of the structure and we will calculate the absorbed power in the detector. The indices of refraction of the different materials can be found in table 4.3. In the remainder of the text, lattice-matched $In_{0.53}Ga_{0.47}$ will be written as InGaAs.

To calculate the absorbed power, we make use of the following formula

Material	**index of refraction[-]** $n_r - jn_i$	**absorption coeff.**[cm^{-1}] α
Silicon	3.48	0
Silica	1.44	0
BCB	1.54	0
$In_{0.53}Ga_{0.47}As$ $\lambda_0 = 1.55\mu m$	$3.60 - 0.0965j$	7820

Table 4.3: Index of refraction and coefficient of absorption ($\alpha = \frac{4\pi}{\lambda_0} n_i$) of the materials used in the simulations

[56]:

$$P_{abs} = -2k\sqrt{\frac{\epsilon_o}{\mu_o}} \int\int n_r n_i |E^2| dydz \tag{4.11}$$

with $k = \frac{2\pi}{\lambda_o}$, n_r and n_i the real and imaginary part of the refractive index of the semiconductor material and $|E|$ the modulus of the electric field. The area of integration is a longitudinal cross-section and can be restricted to the InGaAs layer as this is the only material in which $n_i \neq 0$.

4.7.1 Vertical coupling

A straightforward way to couple light from a silicon waveguide into a detector on top of it is to etch a diffractive structure in the waveguide to couple light vertically out of the waveguide, into a detector on top of it. This coupling approach could also be referred to as diffractive coupling or grating-assisted coupling. By etching a diagonal mirror into the waveguide, vertical coupling is also possible (Figure 4.15a). From a technological point of view, the detector could be integrated using a bump bonding process or a wafer bonding process.

4.7.1.1 Simulation example

Consider the following one-dimensional structure (Figure 4.16). A layer of InGaAs, with a thickness d is bonded on top of a 1-D shallow grating etched in an SOI waveguide with a 1μm thick layer of DVS-BCB. The grating discussed here is optimized for coupling to a standard single mode fiber at a wavelength around 1.55μm. It has a period of 630nm, a fill-factor of 0.5 and is etched 70nm deep. There are 24.5 grating periods (25 trenches). The length of the detector L is equal to the length of the grating.

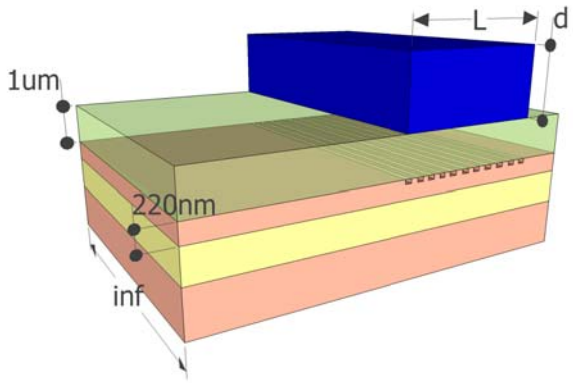


Figure 4.16: A layer of detector material is bonded by means of a 1μm thick DVS-BCB layer on top of a grating. The grating is a standard fiber coupler used for fiber-to-chip coupling (drawing not on scale)

Figure 4.17 shows the fraction of the absorbed power as a function of the thickness d of the InGaAs layer. The dots represent the simulation result. On the same graph, we also plotted a theoretical model which represents the absorbed power fraction or quantum efficiency for discrete detectors which are top- or bottom illuminated with a thickness L and absorption coefficient α. The model takes into account multiple reflections at the top and bottom of the detector:

$$\begin{aligned} P_{abs} &= 0.67(1-e^{-\alpha d}) \\ &\quad (1 + R_{air}e^{-\alpha d} + R_{air}R_{bcb}e^{-2\alpha d} + R_{air}R_{bcb}R_{air}e^{-3\alpha d} + ...) \\ &= 0.67(1-e^{-\alpha d})\frac{1+R_{air}e^{-\alpha d}}{1-R_{air}R_{bcb}e^{-2\alpha d}} \end{aligned} \tag{4.12}$$

With R_{air} (~ 0.32) being the power reflectivity at the InGaAs/air interface and R_{bcb} (~ 0.16) the reflectivity at the InGaAs/BCB interface. The scaling factor 0.67 was obtained by fitting the theoretical model to the simulated values. This means that for this particular configuration, the net power that is diffracted upwards by the grating is approximately 67%.

The oscillations in the simulation results are caused by additional interference effects due to reflections at other interfaces and multiple diffractions at the grating. Figure 4.18 plots the electric field distribution in the grating.

The silicon diffraction grating itself is positioned inside a cavity which is formed by the BCB/InGaAs interface at the top and the silica/silicon sub-

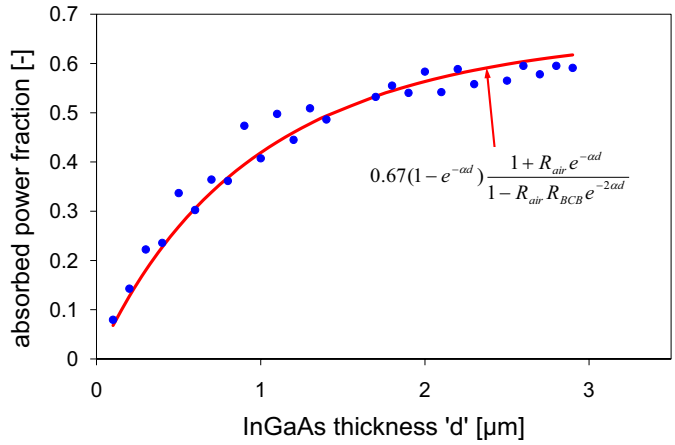


Figure 4.17: Influence of thickness of the InGaAs layer on the absorbed power fraction (dots). The DVS-BCB layer is 1μm thick. A theoretical approximation is also plotted (solid line)

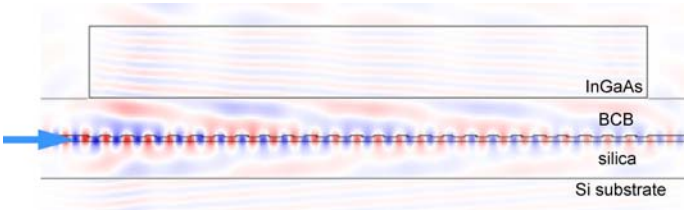
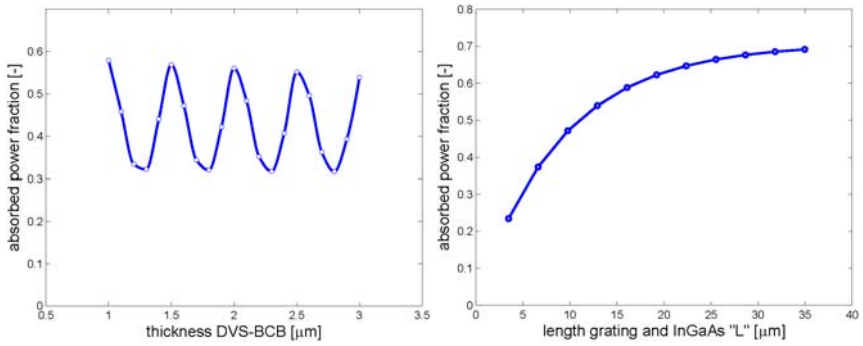


Figure 4.18: Distribution of the transversal field component (E_y) in a vertical coupled detector. Both grating and detector are 15.5μm long



(a) (b)

Figure 4.19: (a) Influence of thickness of the DVS-BCB layer on the absorbed power fraction. The InGaAs layer is 2μm thick and (b) influence of length of the detector and the InGaAs layer (L) on the absorbed power fraction. The InGaAs layer is 2μm thick, the DVS-BCB layer 1μm

strate interface at the bottom. The vertical position of the grating inside this cavity determines the directionality of the grating (ratio of power diffracted upwards to the total diffracted power) and to a smaller extent also the total diffracted power. Figure 4.19(a) shows the absorbed power fraction as a function of the thickness of the DVS-BCB bonding layer for a 15.5μm long grating/InGaAs layer and a 1μm thick silica layer. For this particular configuration, a 1μm thick bonding layer is optimal, but other local maxima exists as can be seen in figure 4.19(a). An anti-reflection coating in between the bonding layer and absorption layer can smooth down the oscillations by avoiding the formation of a cavity.

The total diffracted power is mainly determined by the length of the grating. Figure 4.19(b) again plots the absorbed power, but in this case versus the length of the grating ($L = 0.63\mu$m$\times$number of periods) and InGaAs layer. For long gratings, the maximum detectable power ratio saturates at a value of 70%.

4.7.1.2 Conclusions

- The power diffracted upwards determines the maximum detectable power. So a good grating design with a high directionality is advantageous. Different ways to increase the directionality of a grating have been shown in literature: adding a gold mirror [57] or a DBR [58] underneath the grating or adding a silicon overlay on top of the

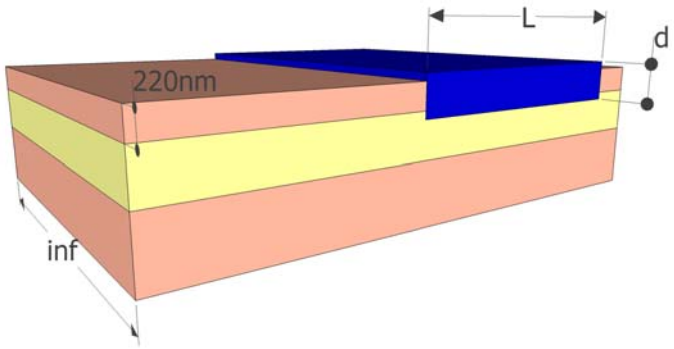


Figure 4.20: A layer of detector material is butt-coupled to the 220nm thick silicon layer. The centers of the silicon waveguide and InGaAs layer are centered. Both the length L end thickness d of the InGaAs layer will be changed

grating [59].

- The thicker the absorbing layer, the higher the efficiency. So highly efficient detectors in this configuration need a thick absorbing layer. This thickness is determined by the penetration depth of the light at a particular wavelength in this material.

4.7.2 Butt-coupling

An alternative way to couple light from waveguide to detector is to etch a recess in the waveguide and to butt-couple detector and waveguide in more or less the same vertical plane (Figure 4.15(b). This could technologically be achieved by both a bump bonding process or epitaxial growth. In the case of a bump bonding process, the facets of the waveguide and the pre-processed detector are aligned in respect with each other. An important point of attention here is the alignment tolerance. Strict tolerances (e.g. due to a small photodetector active area) could result in a time consuming and costly process.

Butt-coupled epitaxially grown germanium detectors have been reported. The advantage in comparison with bump bonded devices is that the alignment of the detectors is done during processing and can be carried out with a very high accuracy which is determined by the lithography tools.

Obtaining butt-coupling using a wafer bonding approach is more difficult, but not impossible as will be explained in paragraph 4.8.2.2.

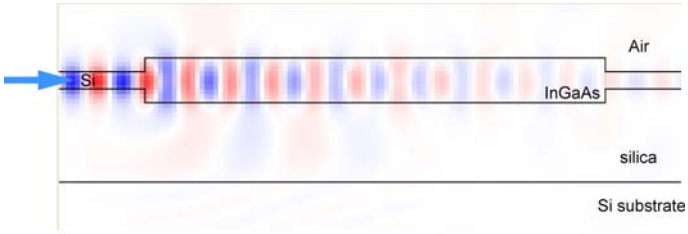
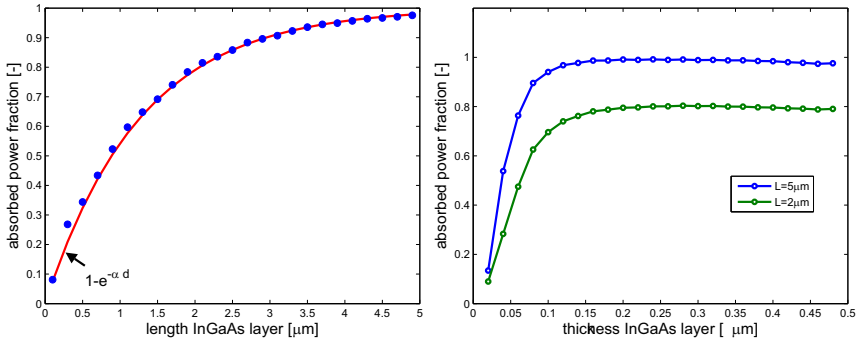


Figure 4.21: Field distribution (E_y) in a butt-coupled detector. The InGaAs layer is 5μm long and 500nm thick



(a) (b)

Figure 4.22: (a)Influence of length of the InGaAs layer on the absorbed power fraction. The absorption layer is 500nm thick. A theoretical approximation is also plotted. (b) Absorbed power fraction as a function of the thickness of the InGaAs layer for a 2μm and 5μm long detector

4.7.2.1 Simulation example

Consider the following conceptual 1D structure (Figure 4.20). A layer of InGaAs, with a thickness d and a length L is placed into a recess etched into the SOI structure. The centers of both the waveguide and InGaAs layer are vertically aligned.

Figure 4.21 shows a typical field distribution in a butt-coupling configuration obtained from CAMFR simulations. In this case, the InGaAs layer is 500nm thick and 5μm long and light enters from the left.

Figure 4.22(a) is a simulation of the power absorption as a function of the length of the absorption layers (blue dots). On the same graph, we also plotted the theoretical model of an exponential decay of a plane wave in an absorbing medium. As we can see, there is a good correspondence between

the simulation and the model. This is because first of all, the reflection at the interface waveguide/detector is very small and secondly, the overlap between the SOI waveguide mode and the InGaAs layer is very high. The reflection at the interface is very small because the refractive indices of silicon and InGaAs are similar. A butt-coupling configuration in which light falls onto the InGaAs layer from a polymer waveguide (low index of refraction) will be less efficient as the reflection at the interface will be higher.

Figure 4.22(b) plots the power absorption as a function of the thickness d of the InGaAs layer. If the absorbing layer is too thin, the overlap between the guided SOI mode and the absorbing layer is too small. As can be seen, the efficiency saturates for an absorbing layer thickness $d \sim 220$nm, which corresponds to the Si waveguide layer thickness. These calculations do not take into account metal contacts which might be present on top of the InGaAs layer. If this layer is too thin, the metal contacts can be in too close proximity with the optical mode resulting in excessive metal absorption loss.

4.7.2.2 Conclusions

- A very high efficiency can be obtained if the reflections at the interface between waveguide and detector are small.
- The overlap between the guided waveguide mode and the absorbing layer should be large enough.
- The necessary length of the detector is determined by the penetration depth in the material and can be very small.

4.7.3 Evanescent coupling

If the detector material can be brought sufficiently close to the silicon waveguide, evanescent coupling can be used as shown in figure 4.15(c). This can be done through either wafer bonding using a thin intermediate bonding layer or direct epitaxial growth. Evanescent coupling is not possible when using a standard bump bonding process because in this case, the distance between silicon layer and detector material is typically several micrometer.

4.7.3.1 Simulation example

Again, consider the following 1D structure (Figure 4.23). A layer of InGaAs, with a thickness d and a length L is bonded with a thin layer of

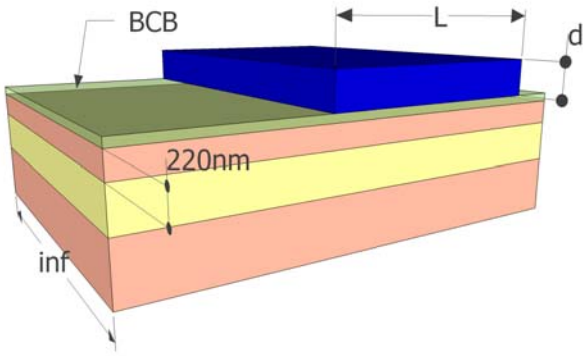


Figure 4.23: A layer of detector material is bonded by means of an intermediate DVS-BCB layer on the silicon waveguide. Both the length L and thickness d of the InGaAs layer will be changed

DVS-BCB on top of the silicon layer. If the bonding layer is sufficient thin, the evanescent field will feel the presence of the InGaAs layer, and absorption will occur.

This is shown in figure 4.24. Here, we plot the power absorption as a function of thickness of the absorbing layer for different bonding layer thicknesses. The length of the detector is fixed at 10μm. In contrast with vertical coupling and butt-coupling, a thicker absorbing layer will not always result in a higher power absorption. For certain thicknesses, the absorption reaches a maximum and the power is efficiently coupled from the waveguide to the detector. By decreasing the bonding layer thickness, the oscillations can be suppressed and higher efficiencies are obtained as can be seen in figure 4.24. The oscillations occur when there is phase-matching between the mode in the silicon waveguide and the InGaAs waveguide. We can also notice that for longer detectors, the oscillation amplitude will decrease, reducing the tolerances on absorbing layer thickness

Figure 4.25 is a plot of the real part of the effective refractive index of the modes of the decoupled silicon slab waveguide and detector slab waveguide as a function of the absorber thickness d. The decoupled Si slab waveguide consists of the silicon core, a DVS-BCB top- and a silica bottom cladding. This waveguide has one guided TE-polarized mode and one guide TM mode, which we will not take into account. The effective index, N_{eff} of the TE-mode is 2.86 (horizontal line in figure 4.25). The detector waveguide consist of an InGaAs core, an air top- and a DVS-BCB bottom cladding layer. Again, we are only interested in TE-polarization. As the

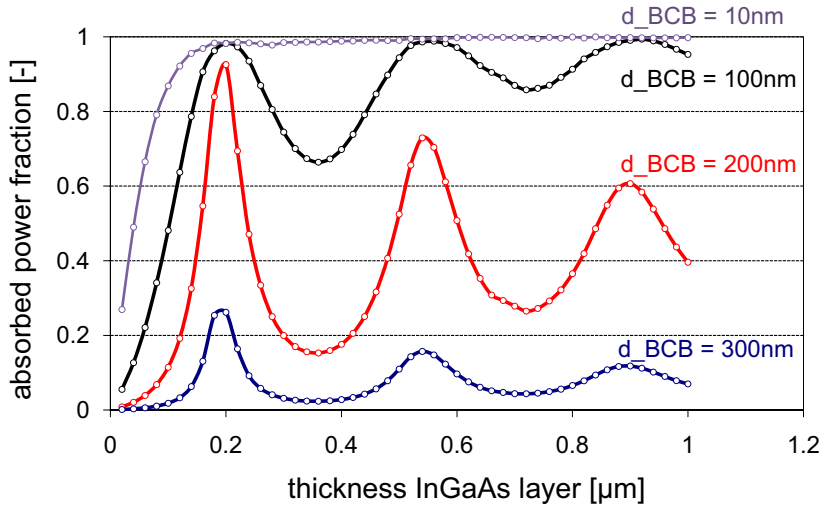


Figure 4.24: The influence of thickness of the absorbing layer on the absorbed power in an evanescently coupled detector for different bonding layer thicknesses. The length of the absorber, $L = 10\mu$m

thickness of the absorbing layer increases, the real part of the effective index also increases, and for certain values, there is phase-matching between one of the modes in the detector waveguide and the mode in the silicon waveguide. This happens for thicknesses of $\sim$200nm, 540nm and 900nm. The corresponding detector waveguide modes are fundamental, first and second order TE-modes.

Figure 4.26 shows electric field distributions for different configurations. In each configuration, there is a 200nm bonding layer and the detector has a length of 10μm. The top configuration has an absorber thickness of 200nm. In this case, there is perfect phase matching with the fundamental TE-mode of the decoupled detector waveguide (figure 4.25) and efficient coupling and photodetection (93% absorption) will occur. For a 360nm thick absorbing layer (middle configuration), there is no phase-matching and a large part of the power remains in the silicon waveguide resulting in a low power absorption (15%). For the bottom configuration (560nm absorbing layer), there is phase-matching with the first order detector waveguide mode and again, efficient photodetection is possible. The corresponding absorbed power fractions can also be seen in figure 4.24.

Simulations show us that by replacing the InGaAs layer with a layer of Ge, the amplitude of the oscillations increases due to the different optical

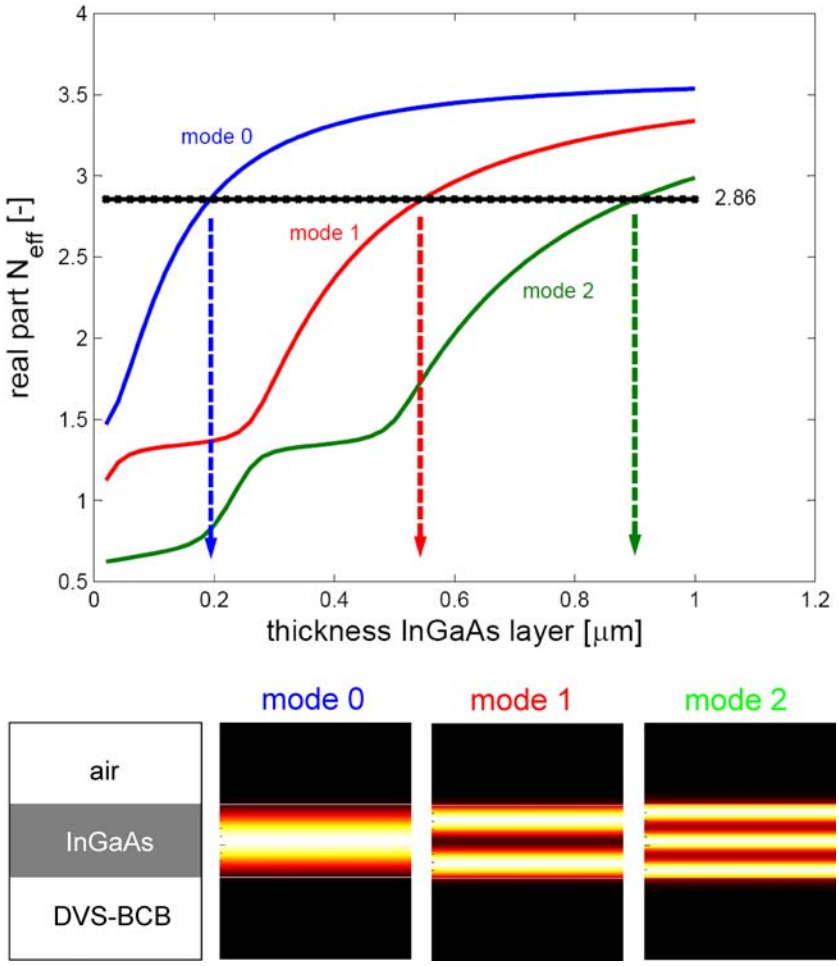


Figure 4.25: Real part of effective refractive index (N_{eff}) of the TE-polarized modes in detector- and silicon waveguide. Mode profiles in the detector waveguide (bottom) are also shown

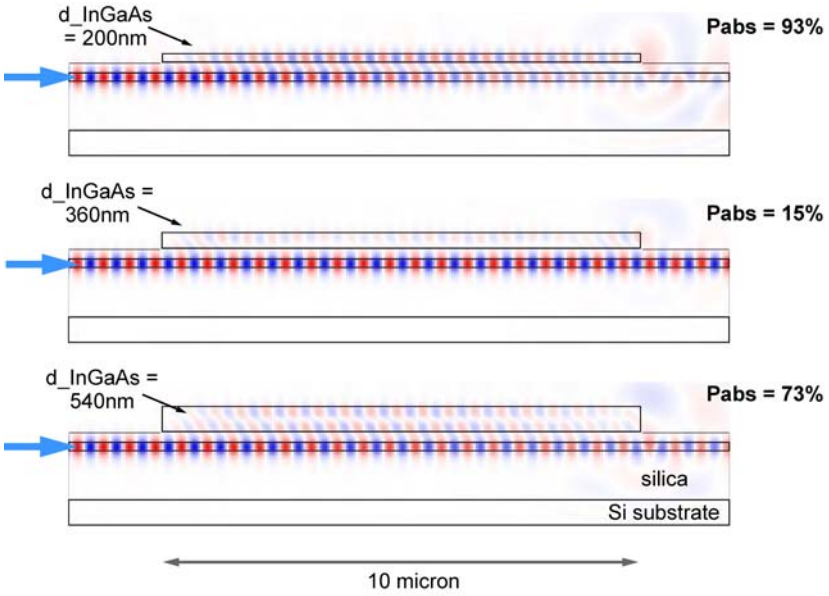


Figure 4.26: Comparison of the field distribution (E_y) in an evanescently coupled detector. The absorbing layer is 10μm long, the DVS-BCB thickness is 200nm. Three designs with a different absorbing layer thickness are shown: 200nm (top), 360nm (middle) and 540nm (bottom)

properties. However, in the case of epitaxial grown Ge on top of the SOI waveguide, there is no low index material in between the waveguide and the detector and as a result, the oscillations are damped again (but still present).

For a scan of the absorbed power fraction as a function of detector length, we refer to chapter 5. In this chapter, we discuss the design and fabrication of an evanescently coupled InGaAs MSM photodetector.

4.7.3.2 Conclusions

- In an evanescently coupled configuration, very high efficiencies (100%) can be obtained in theory.
- The thinner the bonding layer, the higher the efficiency for a given detector length and absorbing layer thickness. Thin bonding layers allow very short detector lengths (=low capacitance).
- For very thin bonding layers, the need for phase matching vanishes.

4.7.4 Conclusion

In this paragraph, we gave an overview of the main coupling schemes that are used to couple light from a silicon waveguide into a photodetector (with preferably InGaAs or Ge as active material). By means of a simplified detector structure, we explained the influences of the waveguide and detector geometry on the power absorption.

Also, as mentioned earlier, certain integration techniques rule out certain coupling mechanisms. Table 4.4 gives an overview of the most used coupling approaches for each integration technique. Due to the typical large and not well controllable vertical distance between detector and the waveguide, hybrid integration by means of bump bonding rules out evanescent coupling. Epitaxial growth and wafer bonding on the other hand allow to bring the detector in close proximity ($<$500nm) to the waveguide and evanescent coupling becomes possible. In the case of epitaxial grown active material, vertical coupling using a grating could be possible, but this would result in a trade-off between bandwidth and efficiency. Butt-coupling to the Si waveguide using wafer bonding is not possible due to the intermediate bonding layer. However, butt-coupling to a polymer waveguide, which on its turn is coupled to the SOI waveguide, is also an option. This can be seen as an indirect butt-coupling approach and will be discussed later.

	vertical coupling	butt-coupling	evanescent coupling
hybrid integration	X	X	
epitaxial growth		X	X
wafer bonding	X		X

Table 4.4: Heterogeneous integration technologies and their corresponding coupling approaches

4.8 Literature overview

This paragraph is a literature overview of different near-IR photodetectors integrated on SOI waveguides. The reported approaches can be classified in different ways (type of material, integration technology, type of photodetector or optical coupling approach). In this paragraph, we will classify the detectors based on the semiconductor material they are made of. After all, the material determines the integration technologies that can be used and these on their turn determine to a large extent the possible optical coupling approaches.

4.8.1 Ge-on-SOI detectors

In recent years, a huge progress has been made in the field of heteroepitaxial growth of pure germanium (Ge) onto silicon by making use of a two-step growth process as discussed earlier. Since 2007, first Si waveguide integrated Ge detectors have been reported by several groups. This were both PIN [7, 8, 60, 61] and MSM [6, 62–64] detectors. In 2007, Vivien and coworkers reported a MSM detector with a high responsivity of 1A/W at a wavelength of 1.55μm (QE$\sim$80%) and an optical bandwidth of 25GHz [6]. The Ge was selectively grown in a recess etched in the silicon waveguide to achieve butt-coupling. The high responsivity was obtained due to firstly a limited reflection at the interface between the waveguide and the detector caused by the small refractive index difference between Ge (n$\sim$4.3) and Si (n$\sim$3.45) and secondly a large overlap between the SOI waveguide mode and the Ge layer. However, the dark current of this device was large (130μA at 1V bias) and was caused by the low Schottky barrier height and dislocations in the Ge layer.

Similar responsivities and bandwidths but lower dark currents in the order of microamperes have been obtained using PIN detectors. Both homojunction PIN detectors [60] where the two contacts are placed on the Ge layer and heterojunction detectors [7] where one or two Ohmic contacts are placed on the silicon layer have recently been reported. Due to further opti-

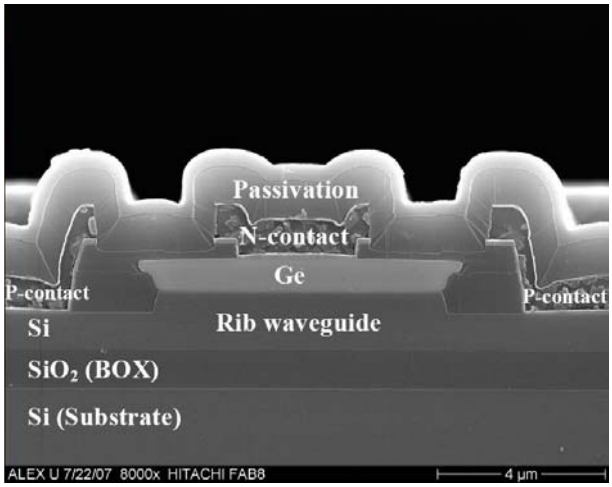


Figure 4.27: Cross-section of a Ge detector integrated on a SOI rib waveguide. Courtesy of Intel [8]

mization of the quality of the Ge layer, dark currents could be even further reduced to the nanoampere range. In [8], researchers of Intel report on an evanescently coupled PIN detector with a responsivity of 1A/W, an optical bandwidth of 31GHz and a dark current of 169nA. A cross section of the device is shown in figure 4.27. As contributions of dark current can come from both the bulk and the sidewalls, both have been dealt with in this work to get a low value. Growth and annealing conditions were optimized to reduce the former component, passivation and doping implantation location were used for the later [8].

Recently, a PIN detector with a 42GHz (optical) bandwidth and a very low dark current of 18nA was reported by UPS-LETI [61, 65]. Other recent results of Si waveguide integrated Ge detectors include avalanche Ge/Si detectors [66, 67], a 40GHz PIN detector [68] and direct bonded Ge detectors instead of epitaxially grown detectors [63, 64]. In [69], the authors study the compatibility of integrated Ge detectors with a standard CMOS process flow. To conclude, table 4.5 gives an overview of some important results in this field.

	Evanescent MSM UPS-LETI 2007 [6]	**Evanescent MSM APD IBM 2010 [67]**
junction	Schottky contacts	Schottky contacts
responsivity	>1A/W(1.55 μm)	0.14A/W(1.5 μm, M=1)
bandwidth (opt.)	25GHz	$\sim$30GHz (M=10)
dark current	130μA (1V)	50μA
detector length	$10\mu m$	20μm
Si waveguide thickness	380nm	$\sim$200nm
	Evanescent PIN MIT 2007 [7]	**Evanescent PIN Intel 2007 [8]**
junction	heterojunction	heterojunction
responsivity	1.08A/W(1.55 μm)	0.89A/W (1.55 μm)
bandwidth (opt.)	7.2GHz	31.3GHz
dark current	$<$ 1μA (-1V)	169nA (-2V)
detector length	$10\mu m$	50μm
Si waveguide thickness	SiON(900nm) or SiN(400nm)	1.5μm
	Evanescent PIN Luxtera 2008 [60]	**Butt-coupled PIN UPS-LETI 2008,2009 [61, 65]**
junction	homojunction	heterojunction
responsivity	0.85A/W (1.55 μm)	1A/W (1.55μm)
bandwidth (opt.)	>20GHz	42GHz
dark current	3μA (-1V)	18nA (-1V)
detector length	-	15μm
Si waveguide thickness	-	380nm

Table 4.5: Overview of the characteristics of heterogeneously integrated Ge detectors

4.8.2 InGaAs-on-SOI detectors

4.8.2.1 Hybridized PIN detectors

When integrating preprocessed photodetectors onto an SOI chip, mostly vertical coupling or butt-coupling approaches will be used. To obtain vertical coupling, a diffraction grating or a turning mirror can be used to couple the light out of the waveguide, into the detector. Butt-coupling can be achieved by flip chipping the detector in an etched recess or by attaching a detector(array) to the edge of the chip.

In [14], two approaches were studied to hybridize a PIN photodetector onto an SOI waveguide substrate. In a first approach, the detector is attached to the edge of the waveguide chip and the waveguide facet can be almost in direct contact with the detector surface. The detector to waveguide alignment can be relatively simple in this case because the detection area can be a few times larger than the waveguide mode size. The authors mention that the main disadvantage of this particular approach is that the waveguide facets need to be polished which can possibly compromise low-cost and high volume manufacturing. The second approach, which was studied in this paper is to flip-chip the processed detector onto the silicon chip surface, where an etched mirror redirects the beam to the detector surface.

In [70] and [11], the hybrid integration of InP laserdiodes was demonstrated using a butt-coupling approach. The same technique could also be used for butt-coupling to detectors. Hybrid integration of lasers onto SOI is more widespread as it is for detectors because at this moment, III-V semiconductors remain the only viable solution for the integration of electrically pumped laserdiodes on silicon. In [71], hybrid detectors which are butt-coupled to silica waveguides were reported.

4.8.2.2 Heterogeneously integrated PIN detectors

Bonding unprocessed III-V dies (using either an adhesive or molecular bonding approach) and subsequent processing makes it possible to bring the detector epitaxial material in close proximity with the SOI waveguide. In this case, evanescent coupling becomes possible. If the bonding layer is too thick, a grating can be used to couple the light out of the waveguide.

In many of these examples, the PIN detector is in fact a reverse biased laser diode [72–74]. In other cases, it is a dedicated detector design [44, 75, 76]. As will be shown in this paragraph, the dedicated detector design often show the best performances (responsivity, size, dark current, complexity) but the reverse biased laser diodes have the advantage that both

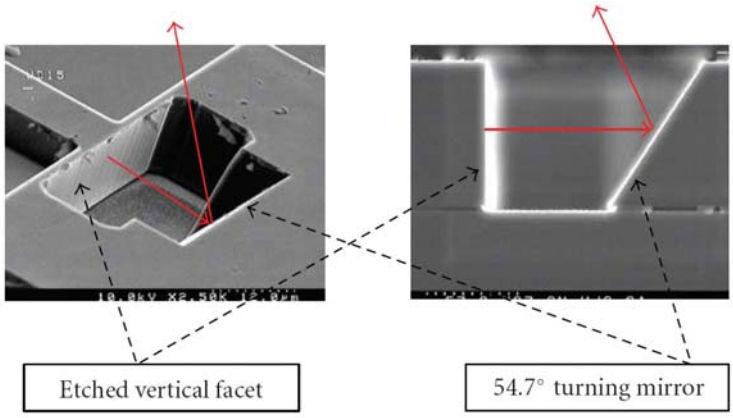


Figure 4.28: SEM picture of an etched waveguide facet and turning mirror [14]

laser diodes and detectors can be processed with exactly the same processing steps, using the same III-V epitaxial structure. This means bonding only one die per chip instead of two different dies which is beneficial for the yield and the cost of the fabrication.

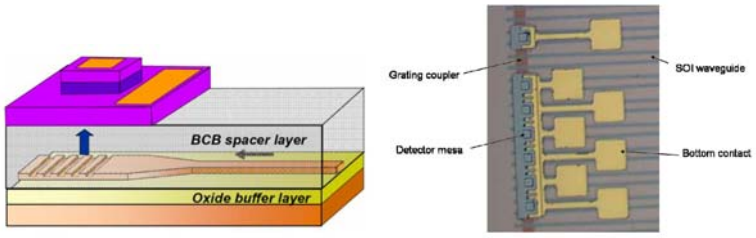
In [75], we bonded a PIN detector on top of a diffraction grating by means of a 3μm thick DVS-BCB bonding layer as can be seen in figure 4.29(a). The SOI substrate consisted of a 220nm silicon waveguide layer and a 1μm thick silica buffer layer. A 10μm long grating (grating period 610nm, duty cycle 50% and 50nm etch depth) was defined in the silicon using 248nm deep-UV lithography. The epitaxial layer structure consisted of a $1\mu m$ thick InP bottom cladding layer, a 120nm thick InGaAsP absorption layer (1.55μm band gap wavelength) and a 1.8μm p-doped InP top cladding. After bonding and subsequent substrate removal, the mesa was etched through the absorbing layer and a AuGeNi n-type contact was deposited. After applying a DVS-BCB insulation layer, top windows were opened and a TiAu p-type contact was evaporated. Figure 4.29(b) show a few devices before the definition of the top contact. The size of the detectors was 10μm $\times$ 10μm. The measured responsivity, referenced to the SOI waveguide power was 0.022A/W at a wavelength of 1.55μm and the dark current was 0.3nA at a reverse bias of 1V. The responsivity was low due to the non-optimized absorption layer thickness and device length. However, simulation results show that by using a 2μm absorption layer thickness, a detector and grating coupler length of 50μm and an optimized bonding layer thickness, efficiencies of 60% are possible.

In [76], a PIN detector was integrated on a 220nm $\times$ 500nm Si photonic wire. The integration was done using molecular die-to-wafer bonding with a 300nm intermediate oxide layer. Light from the silicon wire was coupled into the detector structure by means of an InP membrane input waveguide as schematically shown in figure 4.30. The two waveguides act as a vertical directional coupler which couples the light from the Si wire into the transparent InP waveguide. This InP waveguide is a highly n-doped layer which also acts as bottom cladding material for the PIN detector. The detector structure consists of a 700nm InGaAs absorption layer sandwiched between a p-doped InGaAs contact layer and the n-doped waveguide layer. In order to efficiently couple between waveguide and detector, a rather tight control of the coupler length and the bonding layer thickness is needed. Responsivities of 0.45A/W (1575nm) and an electrical bandwidth of 33GHz have been reported.

In [72], a SOI waveguide coupled Fabry-Pérot laser diode was reported. In this case, the laser diode was butt-coupled to a polyimide waveguide. Coupling between the SOI waveguide and the polymer waveguide was done using an inverted taper, which adiabatically transforms the SOI waveguide mode to the fundamental mode of the polymer waveguide. When reverse biased, the laser diode operates as a photodetector and a responsivities of 0.23A/W ($\lambda = 1.555\mu$m) was reported.

Another example of a photodetector which is compatible with laser diode processing is reported in [74]. In this case, the III-V structure was transferred to the patterned silicon wafer through a low temperature oxygen plasma assisted wafer bonding process. This means that there is no intermediate bonding layer and light is evanescently coupled between the SOI waveguide and the III-V layers. After substrate removal, a laser diode, a directional coupler and photodetectors were simultaneously processed. The chip layout is shown in figure 4.32. The laser is a racetrack ring resonator. On the bottom, a directional coupler is used to collect the laser power into two 440 μm long photodetectors. These detectors have the same waveguide architecture as the laser, the only difference being that they are reversely biased to collect photogenerated carriers. These detectors have a responsivity of 1.1A/W at $\lambda = 1.58\mu$m and a dark current of 200μA.

A very similar photodetector was reported in [73] and the compatibility with laser/amplifier processing was demonstrated by processing an amplifier in front of the photodetector [77]. A schematic drawing of this device is shown in figure 4.33. This $400\mu m$ long detector has a responsivity of 1.1 A/W ($\lambda = 1.58\mu$m), a 50nA to 200nA dark current and a bandwidth of 467MHz. This bandwidth is RC limited by the large capacitance of the long detector.



(a) Schematic drawing

(b) Top view of the fabricated structure before top contact definition

Figure 4.29: Vertically coupled PIN detector [75]

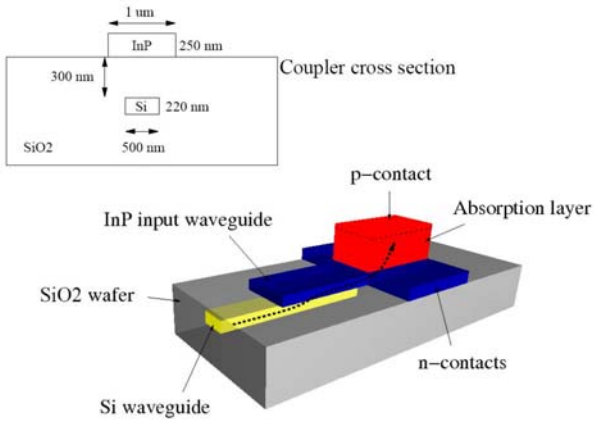


Figure 4.30: Schematic drawing of the evanescently coupled PIN detector as reported in [76]

Very recently, in 2010, our group reported on a 40μm long evanescently coupled PIN detector with a responsivity of 1.1A/W at a wavelength of 1.55μm and a dark current as low as 10pA [44] at 0.5V bias.

4.8.2.3 Heterogeneously integrated MSM detectors

The detector design investigated in this work is an evanescently coupled MSM detector and will be discussed in detail in chapter 5. The detector material (InAlAs/InGaAs) is bonded by means of a thin (<300nm) DVS-BCB bonding layer on top of an SOI waveguide substrate. The main performance parameters are given in table 4.6. We demonstrated detectors with

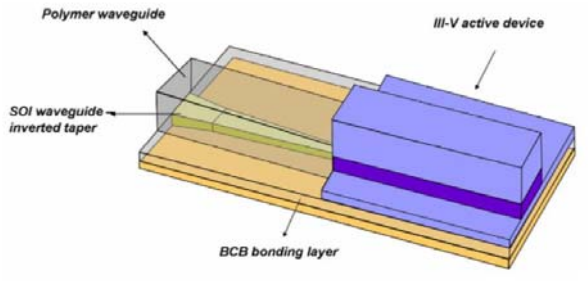


Figure 4.31: Schematic drawing of a butt-coupled PIN detector [72]

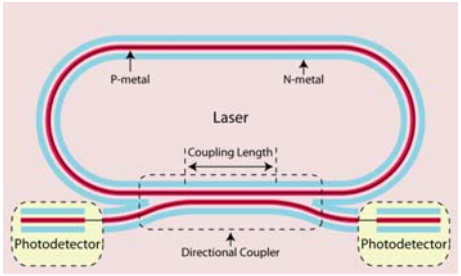


Figure 4.32: Schematic drawing of an evanescently coupled racetrack laser and PIN photodetector [74]

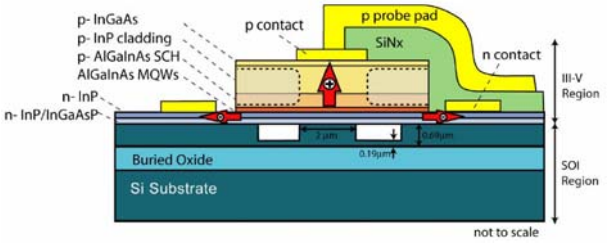


Figure 4.33: Schematic drawing of an evanescent PIN photodetector [73]

	Vertical PIN [75] UGent-IMEC	**Butt PIN [72] UGent-IMEC**
responsivity	0.02A/W (1.55 μm)	0.23A/W (1.555μm)
bandwidth	-	-
dark current	$0.3nA(-1V)$	$50nA(-2V)$
compatible with laserdiode	No	Yes
detector length	10μm	50μm
Si waveguide thickness	220nm	220nm
	Evanescent PIN [74] Intel	**Evanescent PIN [73] Intel**
responsivity	1.1A/W (1.58μm)	1.1A/W (1.55μm)
bandwidth	-	500MHz
dark current	$200\mu A(-5V)$	$200nA(-4V)$
compatible with laserdiode	Yes	Yes
detector length	440μm	400μm
Si waveguide thickness	690nm	690nm
	Evanescent PIN [76] Tu/e	**Evanescent MSM [78] UGent-IMEC**
responsivity [A/W]	0.45A/W(1.575μm)	1.0A/W(1.55μm)
bandwidth	$33GHz$	-
dark current	$1.6nA(-4V)$	$4.5nA(5V)$
compatible with laserdiode	No	No
detector length	10μm	30μm
Si waveguide thickness	220nm	220nm

Table 4.6: Overview of the characteristics of heterogeneously integrated InGaAs detectors

a length of 30μm, a dark current of 4.5nA at 5V bias and a responsivity of 1.0A/W at a wavelength of 1.55μm [78].

Figure 4.34 gives an overview of responsivity and dark current of reported thin-film III-V on SOI detectors.

4.9 Conclusions

In this chapter, we gave an overview of the possibilities to integrate near-infrared photodetectors on SOI waveguides. In a first part, we discussed the two most promising approaches which exist today to fabricate these detectors on a SOI wafer scale: epitaxial grown Ge-on-SOI detectors and heterogeneously integrated InGaAs-on-SOI detectors by means of die-to-wafer bonding. We studied adhesive die-to-wafer bonding in more detail and we described the developed integration process based on manual bonding of III-V dies on SOI using a sub-300nm intermediate BCB bonding

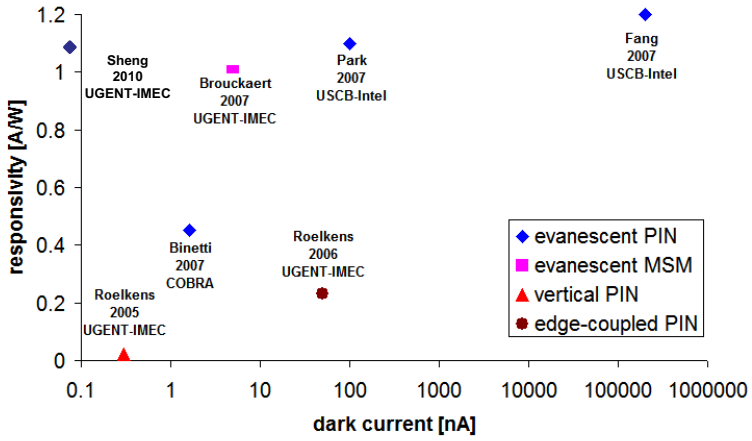


Figure 4.34: Performance of reported thin film III-V on SOI detectors

layer. We demonstrated a high bonding yield and multiple die-to-wafer bonding. However, we also pointed out that an automated die-to-wafer bonding approach is needed in order to obtain a mature fabrication process that is suitable for commercial applications. Also, additional development is needed in order to get to a reproducible, high yield III-V processing on an 8 inch SOI wafer, populated with hundreds of thin III-V films.

In a second part, we studied various waveguide-to-detector coupling approaches and finally we gave an overview of the state-of-the-art of both InGaAs-on-SOI and Ge-on-SOI detectors. First waveguide integrated Ge detectors suffered from a high dark current which was due partly by the large dislocation density in the epitaxial grown germanium. At the time of writing, Ge-on-SOI detectors have closed the performance gap that existed as compared to InGaAs-on-SOI detectors. Dark currents have been reduced to the level of tens of nanoamperes which is only slightly higher as compared to dark currents reported for InGaAs-on-SOI detectors. Also avalanche Ge-on-SOI detectors have been reported. In terms of bandwidth, the level of 40GHz was recently crossed for a Ge-on-SOI detector. These bandwidths have not yet been reported for InGaAs-on-SOI detectors. However, this is more a matter of research effort and not a fundamental issue.

The main reason why research- and even commercial interest is oriented more towards Ge-on-SOI detectors is because fairly standard CMOS processes can be used for their fabrication: germanium is already used by most leading chip manufacturers and Luxtera already commercializes SOI photonic IC's with integrated Ge detectors. Even if InGaAs would be the preferable material due to its direct bandgap structure and optimal energy

gap for wavelengths used for telecommunications (1.31 and 1.55μm), the integration in Si technology is more complicated. The die-to-wafer bonding used for integrating InGaAs detectors still suffers from yield and reproducibility issues which need to be solved and moreover, the integration of these detectors (typically with gold contacts) in a CMOS process might be complicated by cross contamination concerns.

We believe that for different applications, InGaAs-on-SOI detectors are still an attractive alternative for Ge-on-SOI detectors. Firstly, for the fabrication of on-chip lasers, integration of III-V material is the only viable solution at the moment and detectors and sources could be fabricated in the same processing steps, using the same wafer scale III-V technologies. Secondly, for prototyping and research purposes, smaller investments are needed for die-to-wafer bonding as compared to the expensive equipment needed for heteroepitaxial growth. Third, for spectroscopy applications in the 1.65-1.7μm wavelength range, the absorption of (strained-)Ge is too low for efficient photodetection [61]. Due to it's lower direct band gap, efficient detection is still possible using InGaAs detectors [79]. Last and maybe most important, the heterogeneous integration based on die-to-wafer bonding in combination with the developed coupling schemes is very generic. By bonding other semiconductors materials for example such as InAs quantum dots or InAsSb, the bandgap can be further reduced and long wavelength detection becomes possible.

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5

Evanescently coupled MSM photodetector

In the previous chapter, we focused on the technology and the coupling mechanisms that are needed to integrate InGaAs detectors on nanophotonic SOI waveguides. In this chapter, we present a highly efficient and very compact evanescently coupled InGaAs metal-semiconductor-metal photodetector, integrated on SOI by means of BCB die-to-wafer bonding. In a first part, we discuss the design of the detector. In a second part, we present the fabrication and the characterization.

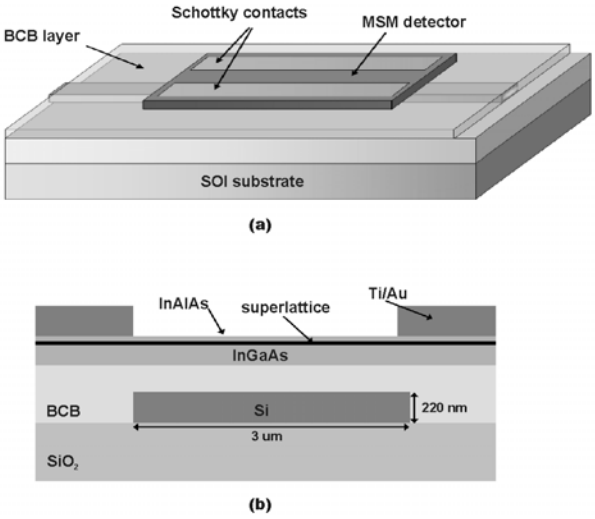


Figure 5.1: (a) Three dimensional- and (b) cross section view of waveguide integrated MSM detector

5.1 Introduction

As mentioned in chapter 4, the quantum efficiency of vertically illuminated photodetectors will increase if a thicker InGaAs absorbing layer is used. To maintain high efficiency, relatively thick absorbing layers are needed. This implies a tradeoff between detector quantum efficiency and the transit time limited bandwidth which is inherent for most top- or bottom illuminated detectors [1, 2]. This tradeoff can be circumvented by using edge illumination and guided-wave detectors because in these cases, the optical absorption path length is independent of the carrier transit length. The integrated detector described in this section is a guided-wave detector, and thus offers the potential for efficient, high bandwidth operation.

5.2 Design and simulations

A schematic picture of the design we propose is shown in figure 5.1 (a). A guided-wave metal-semiconductor-metal (MSM) detector with two coplanar Schottky contacts is bonded on top of a 3μm wide deeply etched SOI waveguide. Lateral confinement in the detector waveguide is obtained by the two Ti/Au Schottky electrodes as will be explained later. The design is based on the principle of coupled mode theory. By using a thin bonding

layer (<300nm) and by proper design to obtain phase-matching between the optical mode in the SOI waveguide and the detector waveguide mode, optical coupling between guide and detector will occur [3].

To obtain phase-matching between the two fundamental modes, the height of the detector layer stack will be close to the height of the silicon waveguides (220nm) because refractive indices of silicon and InGaAs are comparable in magnitude. This thin detector layer stack could have a negative influence on efficiency because the top metal contact of a standard PIN detector would be in close proximity with the detector mode, thereby introducing excessive loss. We solved this by designing a guided-wave MSM detector with two coplanar Schottky contacts. As the detector waveguide mode is confined in between the two coplanar metal contacts on top of the detector layer stack, the optical absorption in these contacts can be largely avoided.

A schematic cross section is shown in figure 5.1(b). The material structure of the detector consists of a 40nm InAlAs Schottky barrier enhancement layer, 20nm InAlAs/InGaAs superlattice layer and a 145nm InGaAs absorption layer. The superlattice softens the bandgap discontinuity between InAlAs and InGaAs as will be explained in the next section. Two Schottky electrodes (Ti/Au, 20nm/200nm) are deposited on top, with the same spacing as the SOI waveguide. The SOI waveguide has a thickness of 220nm and is deeply etched. The detector layer stack is bonded with a BCB adhesive layer onto the SOI waveguide substrate.

5.2.1 Detector epilayer design

5.2.1.1 General layer structure

The layer structure of the detector wafer is shown in table 5.1. All layers are epitaxially grown on a semi-insulating InP substrate, are not-intentionally doped and lattice matched to InP. This fixes the exact composition of InGaAs : $In_{0.53}Ga_{0.47}As$ and InAlAs : $In_{0.52}Al_{0.48}As$. Next to the functional MSM detector layers as mentioned above, there is a cap layer, an etch-stop layer, a sacrificial layer and a buffer layer. Layers that are closest to the substrate will be closest to the top of the final thin film detector because the III-V dies are bonded onto the SOI wafer with the epitaxial layer stack facing down (InP substrate facing up).

5.2.1.2 Sacrificial layers

A first layer that is grown is an InP buffer layer. On top, there is a 200nm thick InGaAs etch-stop layer, followed by a 50nm thick InP sacrificial layer.

material	thickness [nm]	doping	function	remarks
i-InP	50	n.i.d.	cap layer	
i-InGaAs	145	n.i.d.	absorbing layer	background doping as low as possible $N_B < 10^{15} cm^{-3}$
i-InGaAs	4	n.i.d.	superlattice layer	idem
i-InAlAs	1	n.i.d.	superlattice layer	idem
i-InGaAs	3	n.i.d.	superlattice layer	idem
i-InAlAs	2	n.i.d.	superlattice layer	idem
i-InGaAs	2	n.i.d.	superlattice layer	idem
i-InAlAs	3	n.i.d.	superlattice layer	idem
i-InGaAs	1	n.i.d.	superlattice layer	idem
i-InAlAs	4	n.i.d.	superlattice layer	idem
i-InAlAs	40	n.i.d.	SBEL	idem
i-InP	50	n.i.d.	sacrificial layer	
i-InGaAs	200	n.i.d.	etch-stop layer	
i-InP		n.i.d.	buffer layer	
InP substrate			substrate	semi-insulating

Table 5.1: Epitaxial layer structure of the InGaAs/InAlAs MSM detector wafer

These two layers are necessary for the InP substrate removal after BCB bonding. This will be explained in paragraph 5.3. The top layer of the wafer is a 50nm thick InP cap layer. Prior to bonding, this layer will be selectively removed over the InGaAs absorbing layer. The cap layer serves as a protective layer: by removing this cap layer, particles which are present on the wafer surface will lift-off, resulting in a clean, 'bonding-ready' wafer surface.

5.2.1.3 Schottky contacts for InGaAs MSM detectors

A representative band diagram of an MSM detector under normal operation conditions is shown in figure 5.2. In this mode of operation, one of the Schottky contacts is forward biased (anode), the other is reverse biased (cathode) and the semiconductor is fully depleted. This means the applied bias is greater than the flatband voltage. In figure 5.2, ϕ_{n1} is the electron barrier height at the cathode, ϕ_{p2} is the hole barrier height at the anode and $\Delta\phi$ is the bias dependent barrier lowering due to image force. By assuming that first the dark current is primarily due to thermionic emission, second the applied bias is greater than the flatband voltage and third breakdown effects and surface state transport can be neglected, then the dark current can be written as:

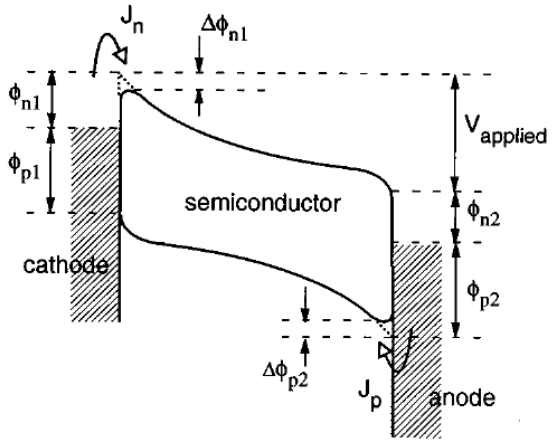


Figure 5.2: Energy band diagram of an MSM detector under normal operating conditions. $V_{applied}$ is the bias voltage. The anode is the forward biased Schottky contact, the cathode the reverse biased contact [4]

$$\begin{aligned} J &= A_n^* T^2 exp(\frac{-q(\phi_{n1} - \Delta\phi_{n1})}{kT}) \\ &\quad + A_p^* T^2 exp(\frac{-q(\phi_{p2} - \Delta\phi_{p2})}{kT}) \end{aligned} \tag{5.1}$$

where T is the temperature and A_n^* and A_p^* are the effective Richardson constants for electron and holes [4–6]. The electron current is due to thermionic emission of electrons from the cathode, the hole current comes about because of the thermionic emission of holes from the anode. From this equation, we can conclude that the dark current can be reduced by increasing the electron barrier height ϕ_{n1} and hole barrier height ϕ_{p2}. If the same metallization is used for both the anode and cathode, which is most often the case, then these cannot be varied independently because $\phi_{n1} + \phi_{p2} = E_g$, with E_g being the bandgap of the semiconductor.

Low dark current MSM detectors on GaAs can be made by directly metallizing the absorption layer. This is due to its relatively large bandgap (E_g=1.42eV) and large barrier heights on GaAs. For InGaAs (E_g=0.75eV) on the other hand, this is not the case. The relatively low Schottky barrier height on n^--InGaAs (0.2eV) results in an excessive dark current [7]. To reduce the dark current to reasonable levels, a thin high band gap material between the InGaAs absorption layer and the Schottky contacts is required.

This layer effectively increases the Schottky barrier height and is called a Schottky Barrier Enhancement Layer (SBEL). Different types of Schottky barrier enhancement layers on InGaAs have been reported in literature: Fe-doped InP [8, 9], undoped InP [10–12], InAlAs [7, 13–24], GaAs [25] and AlGaAs [26].

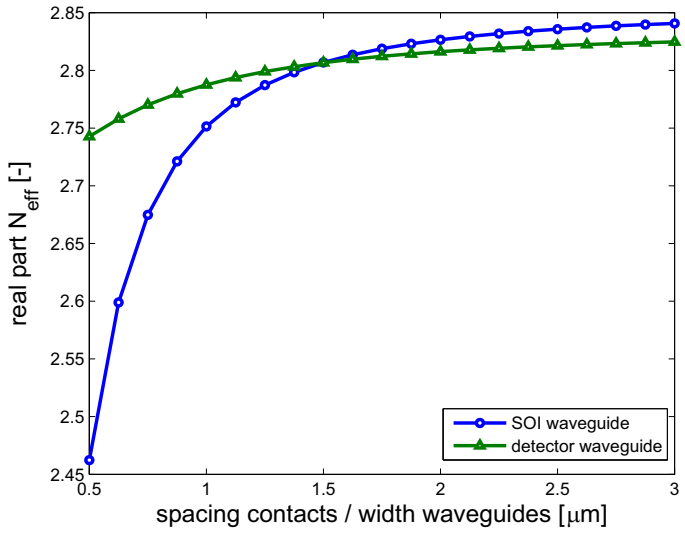
A detailed study of SBELs on InGaAs was not within the scope of this work. Based on the literature study above, we concluded that very good photodetector performance (low dark current, short impulse response, linear behavior) can be achieved by making use of a layer stack consisting of a thin layer of undoped, lattice matched InAlAs (E_g=1.46eV), followed by a graded InAlGaAs layer and finally the InGaAs absorbing layer [7, 14–24]. The graded region minimizes the charge pileup due to the large band discontinuity at the InAlAs/InGaAs heterointerface. Charge pileup at the heterointerface has been shown to degrade the photodetector performance: long impulse response, the presence of low frequency gain and a high flat band voltage [17–19]. Both compositional graded layers and graded superlattice layer were reported to improve the detector performance. We have chosen a 40nm thick InAlAs SBEL in combination with a 20nm digitally graded InAlGaAs superlattice consisting of four 5nm thick periods of InGaAs and InAlAs. The first period (starting from the top of the layer stack) is composed of 4nm of InAlAs and 1nm of InGaAs and the last period is reversed with 1nm of InAlAs and 4nm of InGaAs. The intermediate layers vary linearly between these two endpoints (see table 5.1).

5.2.2 Optical simulations

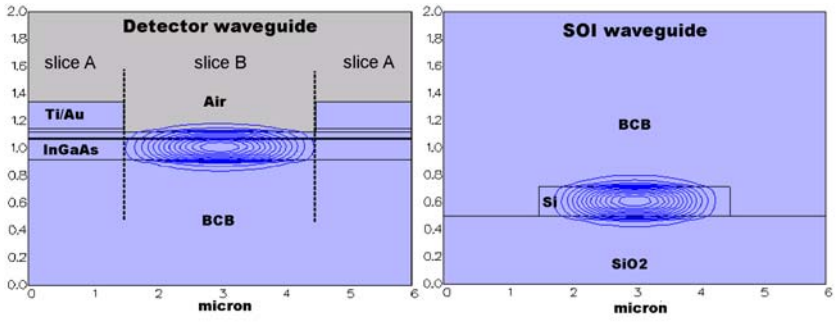
As mentioned earlier, the functioning of this evanescently coupled photodetector is based on the principle of coupled mode theory. Very efficient coupling from SOI waveguide to the detector will occur if firstly, there is phase matching between the modes in the SOI waveguide and the detector waveguide and secondly, the intermediate BCB bonding layer is as thin as possible. An overview of the refractive indices of the materials used in the simulations is shown in table 5.2.

5.2.2.1 Confinement and mode properties

Lateral confinement of the detector waveguide mode is obtained by the two Ti/Au Schottky electrodes. The large imaginary part of the refractive indices of Ti (4.62) and Au (9.81) at 1.55μm lowers the effective refractive index of the fundamental slab mode of slices A as compared to slice B and this causes lateral confinement as can be seen in figure 5.3(b). This figure



(a) Real part of the effective refractive index of the TE ground modes of the decoupled detector waveguide and decoupled SOI waveguide as a function of contact spacing and waveguide width respectively



(b) Corresponding mode profiles

Figure 5.3: Mode profiles of the decoupled detector waveguide and SOI waveguide and their index

Material	Refractive index	Absorption coeff.[cm^{-1}]	Reference
Si	3.476	-	
SiO_2	1.444	-	
BCB	1.54	-	
$In_{0.53}Ga_{0.47}As$	3.595 - 0.096j	7820	[27]
$In_{0.52}Al_{0.48}As$	3.202	-	
Ti	3.69 - 4.62j	374560	[28]
Au	0.559 - 9.81j	795330	[29]

Table 5.2: Refractive indices of materials at $\lambda = 1.55\mu$m used in the simulations

plots the profiles of the fundamental TE-modes of the decoupled detector waveguide and SOI waveguide. As the Schottky contacts provide lateral confinement, the absorption loss in the Ti/Au electrodes is small and on top of that, no waveguide ridge has to be defined, strongly simplifying the processing.

Figure 5.3(a) shows the (real part of the) effective refractive index (N_{eff}) of the TE ground modes of the decoupled detector- and SOI waveguide as a function of respectively Schottky contact spacing and waveguide width. Corresponding mode profiles are shown in 5.3(b). Using deep-UV lithography, contact spacings down to 200nm are easily obtainable but here we limited ourselves to 1μm, which is compatible with standard optical contact lithography. Phase-mismatch of the decoupled waveguide modes smaller than 1.3% can be obtained with spacings/widths from 1μm to 3μm using the layer structure described above. As absorption resonances occur when the (real) propagation constants of the fundamental modes of the decoupled waveguides coincide, the smaller the phase-mismatch, the higher the detector absorption per unity of length.

5.2.2.2 Absorbed power vs. length and vs. bonding layer thickness

Fimmwave, a fully vectorial 3D simulation tool based on eigenmode expansion has been used to calculate the absorbed power as a function of the detector length (figure 5.4). The simulated structure has a contact spacing and waveguide width of 3μm. When having a 200nm thick BCB bonding layer between the SOI waveguide and the detector, 95% of the power is absorbed for detector lengths as short as 11μm. It is well known from coupled mode theory that when the spacing between the two waveguides increases, the couple length will also increase. As a consequence of that, the detector efficiency for a given length will decrease for increasing bonding layer thickness as can be seen in figure 5.4. BCB bonding layer thicknesses down

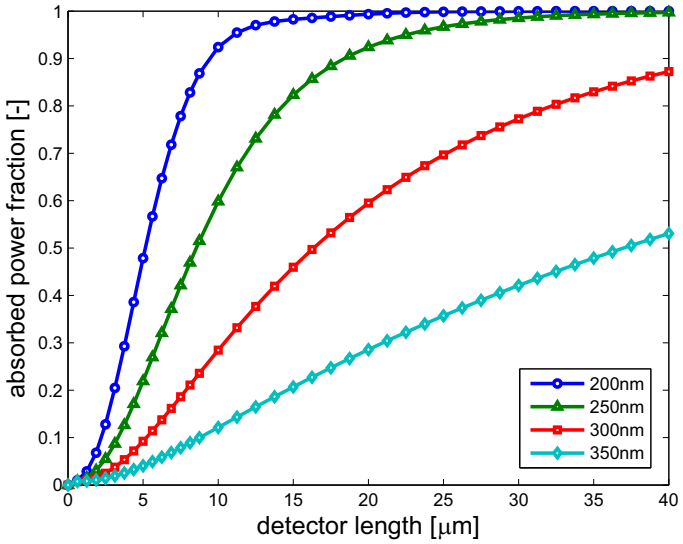


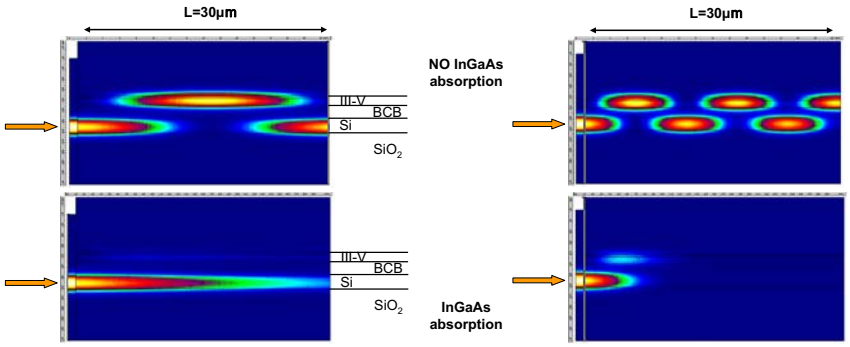
Figure 5.4: Absorption as a function of detector length for different bonding layer thicknesses

to 50nm have been demonstrated as mentioned in chapter 4.3.

Figure 5.5 shows the intensity profile along a longitudinal cross section. The cross sections on the top of this figure are simulation results of the structure without taking into account absorption in the InGaAs layer. The pictures on the bottom are simulation results of the real structure. Figure 5.5(a) is a detector structure with a 400nm thick BCB bonding layer. The use of a relatively thick bonding layer results in a coupling length in the order of 15μm. When decreasing the bonding layer thickness to 200nm, the coupling length decreases to approximately 6μm and as a consequence, light is absorbed over a shorter distance.

5.2.2.3 Metal absorption loss

To estimate the loss due to absorption in the Ti/Au Schottky contacts, we calculated the absorbed power as a function of detector length for both the real structure and the structure where we do only take into account absorption in the Schottky contacts and no absorption in the InGaAs layers. This is an approximation because setting the imaginary part of the refractive index (n_i) of InGaAs to zero slightly influences the field profile. However, this approximation is acceptable because n_i of InGaAs is almost two orders of magnitude smaller as compared to n_i of Ti and Au. The results are



(a) 400nm BCB (b) 200nm BCB

Figure 5.5: Simulated intensity profile along a longitudinal cross section. Pictures on the top do not take into account absorption in the InGaAs layer. Pictures on the bottom are simulation results of the real structure

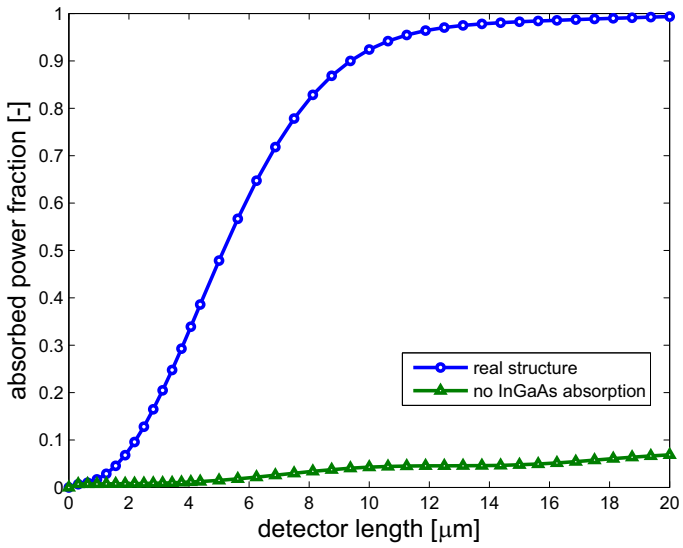


Figure 5.6: Influence of optical absorption in the Schottky contacts (Ti/Au). One curve represents the real structure. The other takes only metal absorption into account and no absorption in the InGaAs layers

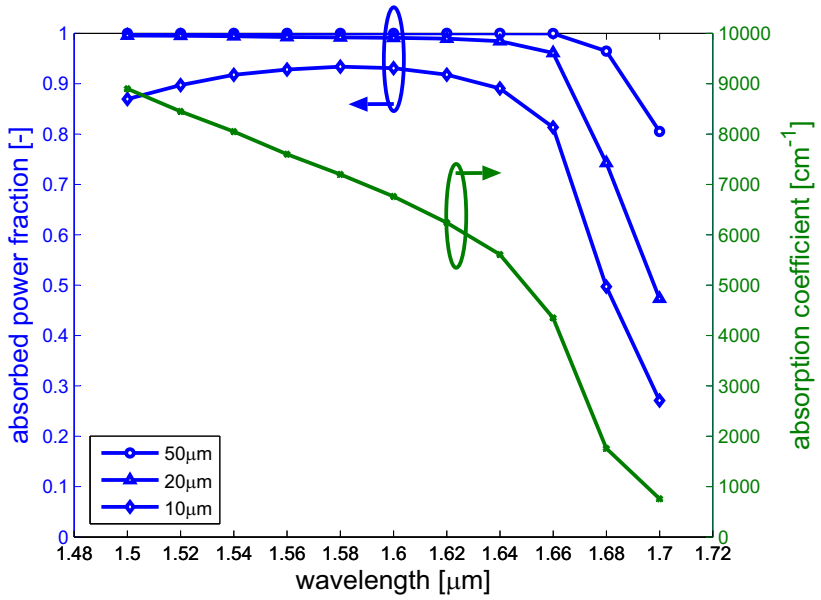


Figure 5.7: Absorption coefficient of InGaAs and spectral bandwidth of the MSM detector, parameter is detector length

shown in figure 5.6. When we only consider absorption in the Schottky contacts, power in the structure is lost, but at a very slow pace. From these calculations, we can conclude that loss due to absorption in the Schottky contacts is limited (smaller than 10% of the total absorbed power). This is caused by the fact that the contacts are used to obtain lateral waveguide confinement as explained earlier in this paragraph.

5.2.2.4 Spectral response

In figure 5.7, the absorbed power as a function of the wavelength is shown for detectors with a length of 10, 20 and 50μm and with a 3μm contact spacing and SOI waveguide. Dispersion relations of all the materials were taken into account in this simulation; however the main contribution is due to the lower absorption coefficient of InGaAs at larger wavelengths [27] as can be seen in figure 5.7. There is a sharp drop in absorbed power around 1.65μm, which corresponds with the bandgap of InGaAs lattice matched to InP. By increasing the detector length the spectral bandwidth can be improved, however, detector capacitance and dark current will rise. The efficiency of the 10μm long detector increases for longer wavelengths be-

fore the sharp drop at 1.65μm as can be seen in figure 5.7. This can be explained by the fact that phase-matching is more perfect at slightly higher wavelengths and so, the effect of the lower absorption coefficient is canceled.

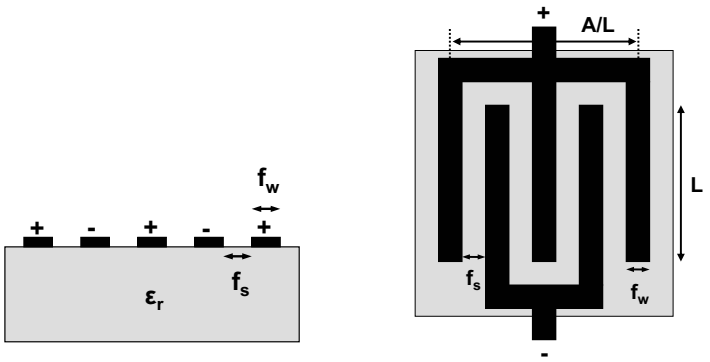
5.2.3 Bandwidth and electro-optical simulations

In this paragraph, we give an overview of important design considerations and parameters that affect the bandwidth (frequency response) of MSM detectors. In a first part, a simplified 1-D model will be discussed to assess the bandwidth and in a second part, we show some simulation results of impulse response and carrier movement using the commercial simulation tool APSYS. This is a 2D/3D finite element solver (Crosslight software Inc., [30]).

5.2.3.1 Introduction

For certain applications (on-chip optical interconnects, receivers,...) a high speed response is necessary. For other applications like spectrometry, it is of less importance. The bandwidth of a photodetector is determined by the speed with which it responds to variations in the incident optical power. There are three major factors which influence the speed of response: the RC time constant of the detector and load, the transit time resulting from the drift of carriers across the depleted regions and the delay resulting from the diffusion of carriers generated outside the depleted regions. Under normal operating conditions, the bias voltage of MSM detectors is high enough to fully deplete the regions where optical absorbance occurs. This way, carrier diffusion can be neglected.

Due to their planar structure, MSM detectors have a very low capacitance per unit area. For example, a detector with a 50μm $\times 50\mu$m active area, 1μm wide electrodes and 2μm electrode spacings - a typical design for vertical coupling from an optical fiber - has a capacitance of $\sim$ 40fF (paragraph 5.2.3.2). This corresponds with an RC time constant of 2ps into a 50Ω load. The average transit time on the other hand will be in the order of $(electrodespacing)/2(saturationvelocity)$ which is $\sim$ 17ps. As the bandwidth is limited by the slowest component, the carrier transit time will limit the speed of response in this case. This will continue to be the case for moderate increases in load resistance or active area. The thin film MSM detector we designed is even smaller (40μm long, 7.5μm wide electrodes and $1-3\mu$m electrode spacing) and has only got two electrodes, resulting in a capacitance of $\sim 5-3$fF in combination of a 50Ω load. This means that in



(a) (b)

Figure 5.8: Schematic drawing of the generic interdigitated MSM structure, in cross section (a) and top view (b)

this case, the speed will also be limited by carrier transit times (paragraph 5.2.3.4).

5.2.3.2 Capacitance of an MSM structure and RC time constant

The capacitance of an MSM structure on an undoped and semi-infinite semiconductor as shown in figure 5.8 is given by [7, 31]:

$$\begin{aligned} C &= \frac{K(k)}{K(k')}\epsilon_0(1+\epsilon_r)\frac{A}{f_s+f_w} \\ &= \frac{K(k)}{K(k')}\epsilon_0(1+\epsilon_r)(N-1)L \end{aligned} \tag{5.2}$$

In this formula, ϵ_0 is the dielectric constant of free space, ϵ_r is the relative dielectric constant of the semiconductor, A is the total detector active area, L is the active detector length, N is the number of interdigitated electrodes (fingers), f_s is the finger spacing and f_w is the finger width. $K(k)$ is defined as the complete elliptical integral of the first kind,

$$K(k) = \int_0^{\pi/2} \frac{1}{\sqrt{(1-k^2 sin^2\phi)}} d\phi \tag{5.3}$$

We define k and k' as follows [7]:

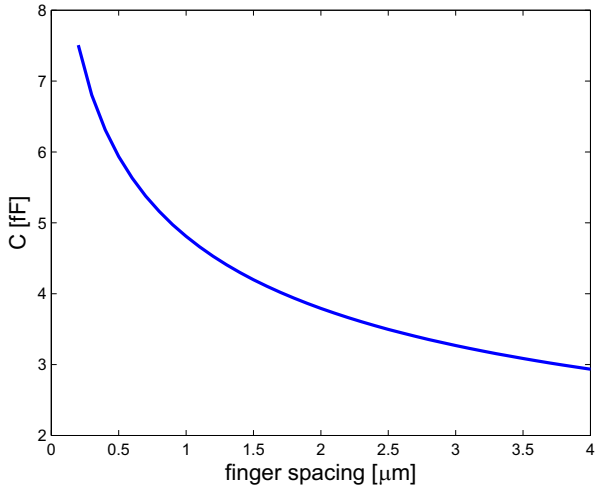
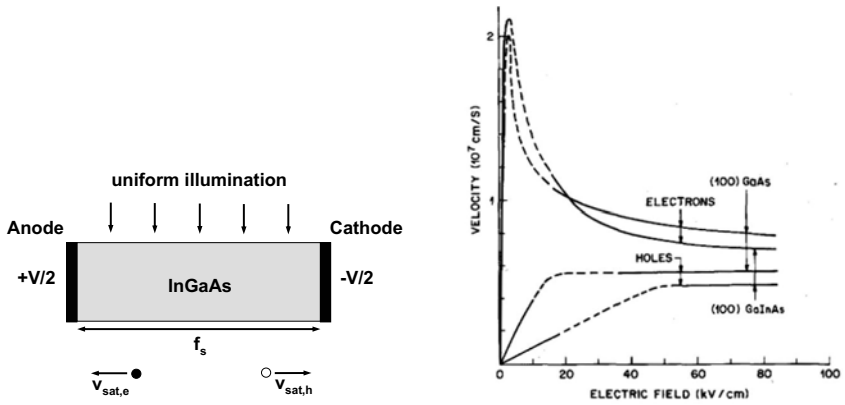


Figure 5.9: Capacitance of the designed MSM detector versus finger spacing. The detector has a length of 40μm and each contact has a width of 7.5μm

$$k = tan^2[\frac{\pi f_w}{4(f_w + f_s)}] \text{ and } k' = \sqrt{1 - k^2} \tag{5.4}$$

Figure 5.9 plots the capacitance of our designed MSM detector as a function of finger spacing (f_s). The detector has two fingers, a length of 40μm and each finger has a width of 7.5μm. The capacitance is calculated using equation 5.2 by setting $N = 2$. Due to the compact detector size, its capacitance is very low. A detector with 1μm spaced contacts has a capacitance of $\sim$5fF. For a fixed contact width and spacing, the capacitance scales linearly with detector length. For these calculations, we took into account the relative dielectric constant of InGaAs ($\epsilon_r = 3.595^2$).

The front end of a receiver consists of a photodetector, followed by a preamplifier. Following a step change in the photogenerated current, the preamplifier voltage will rise or fall exponentially with a time constant RC. If we make abstraction of parasitics and input capacitance of the preamplifier, the RC time constant of our 40μm long MSM detector with 1μm contact spacing (C=5fF), in combination with a 50Ω load is only $\sim$0.25ps.



(a) (b)

Figure 5.10: (a) One-dimensional approximation: parallel plate geometry and (b), carrier velocity versus electric field for InGaAs and GaAs. Taken from [1]

5.2.3.3 Transit time of photogenerated carriers

When the detector is illuminated, carriers are generated in the InGaAs absorption layer and these will drift towards the electrodes under influence of the applied electric field. As mentioned before, diffusion currents can be neglected under normal operation conditions. The high crystal quality of the InGaAs/InAlAs detector allows us also to neglect recombination and charge trapping. The photocurrent induced in the external circuit due to the moving charges is given by Ramo's theorem [32, 33]. For point charges moving in a homogeneous medium, the instantaneous current is given by

$$i_{photo} = \sum q\vec{v}(\vec{r})\frac{\vec{E}(\vec{r})}{V} \tag{5.5}$$

where q, $\vec{v}(\vec{r})$ and $\vec{r}$ are the charge, the velocity and the position of the carriers respectively, $\vec{E}(\vec{r})$ is the electric field due to the electrodes in absence of volume charges and V is the potential difference between the electrodes. The summation is done over all particles (electrons and holes) in the system.

To calculate the impulse response, we approximate the MSM detector as a one-dimensional structure in which we have a homogeneous InGaAs absorption layer in between two electrodes. This parallel plate geometry is shown in figure 5.10(a). For detectors with 'thick' ($> 1\mu$m) absorbing

layers and relative small finger spacings ($< 3\mu$m), this one-dimensional approximation is not sufficient and a 2-D or even 3-D carrier motion analysis is required. For our thin film device, with a 205nm thick detector layer stack, the 1-D model is a good approximation to get an idea of carrier transit times.

The parallel plate geometry strongly simplifies Ramo's theorem since $\vec{E}(\vec{r}) = V/f_s$. If we consider that the initial charge distribution in between the two parallel electrodes is uniform, Ramo's theorem (5.5) predicts an impulse response, which is the summation of the linearly decreasing hole and electron current:

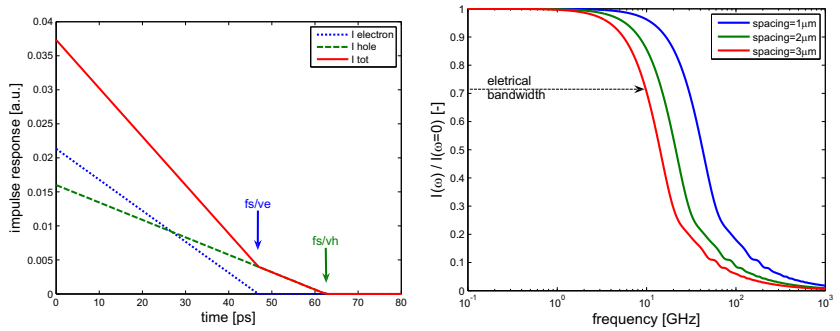
$$h(t) = \frac{1 - \frac{t}{\tau_e}}{\tau_e}(u(t) - u(t - \tau_e)) + \frac{1 - \frac{t}{\tau_h}}{\tau_h}(u(t) - u(t - \tau_h)) \qquad (5.6)$$

where τ_e and τ_h are the transit time of electrons and holes respectively and $u(t)$ is the unit step function. If we suppose that the electric field is high enough (>5V/μm) so that the carriers reach their saturation velocity, then $\tau_e = f_s/v_{sat,e}$ and $\tau_h = f_s/v_{sat,h}$. The carrier velocity as a function of electric field is shown in figure 5.10(b). The saturation velocities of electrons and holes respectively are [1]:

$$\begin{aligned} v_{sat,e} &= 6.5 \times 10^4 m/s \\ v_{sat,h} &= 4.8 \times 10^4 m/s \end{aligned} \qquad (5.7)$$

Under influence of the external electric field, the photogenerated holes will drift towards the cathode. For increasing time, the number of holes in movement decreases linearly as they are collected at the cathode. This results in a linearly decreasing hole current. At $t = \tau_h$, the holes which were generated at the edge of the anode will also reach the cathode and the hole current becomes zero. The same reasoning can be made for the electrons that drift towards the anode. Figure 5.11(a) plots the calculated impulse response for an MSM detector with a finger spacing $f_s = 3\mu$m.

To obtain the frequency response, we take the Fourier transform of the impulse response. This is plotted in figure 5.11(b). If we only take into account one type of carrier, the 3dB point occurs when $\omega\tau = 3.48$. When taking into account both electrons and holes, the same formula is a good approximation if we replace τ with the average transit time for electrons and holes. This is the 3dB electrical frequency, i.e. the frequency where the photocurrent has decreased by $\sqrt{2}$. One could also calculate the 3dB optical frequency (i.e. the frequency where the current has decreased by a factor



(a) Impulse response for a detector with 3μm finger spacing

(b) Frequency response for detectors with 1μm, 2μm and 3μm finger spacing

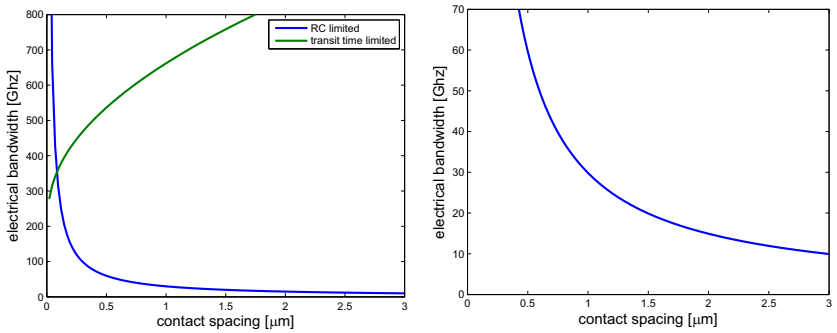
Figure 5.11: Simulated impulse and frequency response of an MSM detector in a one-dimensional approximation

2). The calculated transit time limited electrical bandwidth for detectors with 1, 2 and respectively 3μm finger spacing is $\sim$30, $\sim$15 and $\sim$10GHz.

5.2.3.4 Bandwidth of an MSM photodetector

The RC time constant of the detector and load, the transit time but also other parasitic effects due to the mounting and the measurement system influence the response. The slowest component will determine the bandwidth. The RC time constant and the parasitic elements represent a linear passive network in which the electrodes are embedded and is completely specified by its impulse response. Thus, if we assume that the carrier motion is given and does not depend on the electrode voltage then the impulse response of the photodetector is given by the convolution of the transit time limited response and the network response.

Figure 5.12 plots the electrical bandwidth versus contact spacing of the designed MSM detector (two fingers, length=40μm and finger width=7.5μm). Parasitic effects are not included. The green curve plots the RC limited bandwidth taking into account a 50Ω load and the blue curve plots the transit time limited bandwidth. For decreasing finger spacing, the capacitance increases resulting in a lower RC limited bandwidth but at the same time, the transit time of the carriers decreases. It is clear that for electrodes that are defined using standard contact lithography ($f_s > 1\mu$m), the bandwidth is limited by the carrier transit time and decreasing the electrode spacing results in higher bandwidths.



(a) (b)

Figure 5.12: Electrical bandwidth of an MSM detector versus contact spacing. The device has two coplanar contacts, a length of 40μm and the width of each contact is 7.5μm. Figure (b) is a more detailed plot of the bandwidth region up to 70GHz

5.2.3.5 2-D finite element electro-optical simulations

To obtain a more accurate estimation of the speed of response, we also carried out two-dimensional finite element simulations using APSYS [30]. The main differences (improvements) as compared with the 1-D model are:

- Two-dimensional finite element simulations of the MSM cross section
- The InAlAs SBEL and InAlGaAs graded layers are included in the MSM detector structure
- Non-uniform carrier generation according to the mode profile in detector waveguide
- Electrical field dependence of drift velocity is taken into account
- Besides drift, also diffusion is taken into account
- Thermionic emission and tunneling at the metal-semiconductor interface is taken into account

To model the behavior of the carriers that are generated by an optical pulse under the influence of drift and diffusion forces, Poisson's equation (equation 5.8) and the electron and hole current continuity equations (equations 5.9, 5.10) are solved in two spatial dimensions. The basic equations

used in the simulations are:

$$\epsilon_0 \epsilon_r \nabla^2 \Phi = -q(p - n + N_D - N_A) \tag{5.8}$$

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q} \nabla \vec{J_n} \tag{5.9}$$

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{q} \nabla \vec{J_p} \tag{5.10}$$

where Φ is the electrostatic potential, n and p are the electron and hole carrier concentrations, $N_{D,A}$ are the donor and acceptor concentrations, $\vec{J_{n,p}}$ are the electron and hole currents and $R_{n,p}$ and $G_{n,p}$ are the recombination and generation rates for electrons and holes. The photocurrent in each point of the cross section is the sum of three contributions: the hole current, $\vec{J_p}$, the electron current, $\vec{J_n}$ and the displacement current, $\vec{J_D}$:

$$\vec{J_{total}} = \vec{J_p} + \vec{J_n} + \vec{J_D} \tag{5.11}$$

$$\vec{J_n} = q\mu_n n\vec{E} + qD_n \nabla n \tag{5.12}$$

$$\vec{J_p} = q\mu_p p\vec{E} - qD_p \nabla p \tag{5.13}$$

$$\vec{J_D} = \epsilon_0 \epsilon_r \frac{\partial \vec{E}}{\partial t} \tag{5.14}$$

where $\mu_{n,p}$ and $D_{n,p}$ are the electron and hole mobilities and diffusion coefficients. The displacement current is caused by the changing electrical field in the semiconductor due to the photogenerated carriers and disappears under stationary conditions.

Using the above formulas, the response to an optical pulse can be calculated. To study the speed of response of the MSM detector and the influence of bias voltage and contact spacing, the detector is illuminated with a very short (10 femtoseconds) pulse. This pulse generates electron-hole pairs. The initial spatial distribution of the photocarriers is determined by the intensity profile of the fundamental TE polarized mode of the detector waveguide. This is shown in figure 5.13.

Under the influence of the electric field, the electrons move to the anode, the holes move to the cathode and the changing electric field generates a displacement current. These three current contributions are integrated over a cross section of the detector to calculate the photoresponse. Figure 5.14 plots these different currents over a vertical cross section, located on the right side of the left contact. These calculations are for a device with a 1μm contact spacing. As can be seen, the electron current rapidly falls to

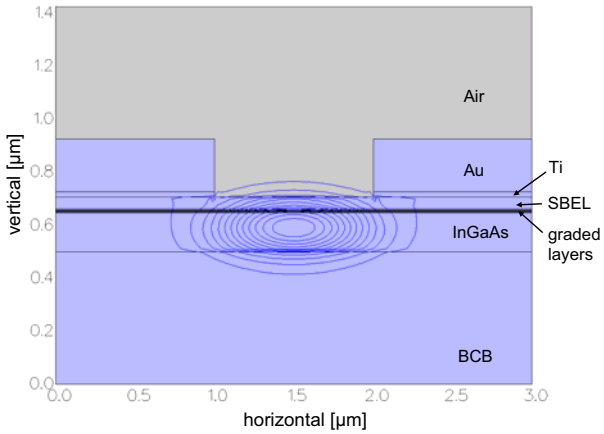


Figure 5.13: Mode profile (intensity) of the fundamental TE mode of the detector waveguide

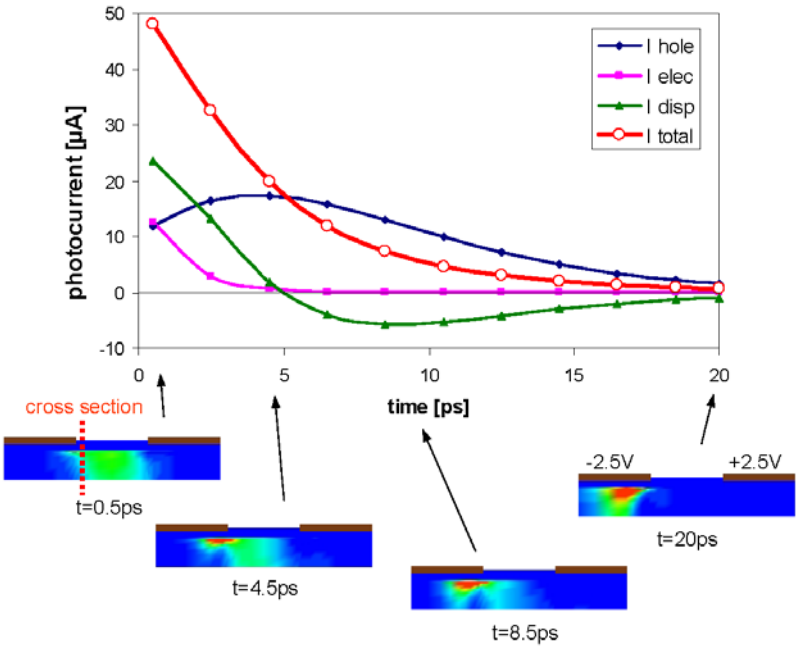
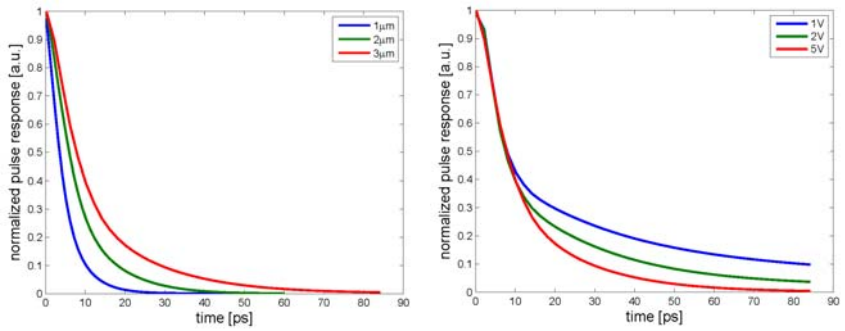


Figure 5.14: Impulse response of the thin film MSM detector with a contact width and a contact spacing of 1μm under 5V bias and the hole concentration at different moments



(a) Influence of contact spacing at 5V bias (b) Influence of bias voltage for 3μm contact spacing

Figure 5.15: Simulated impulse response

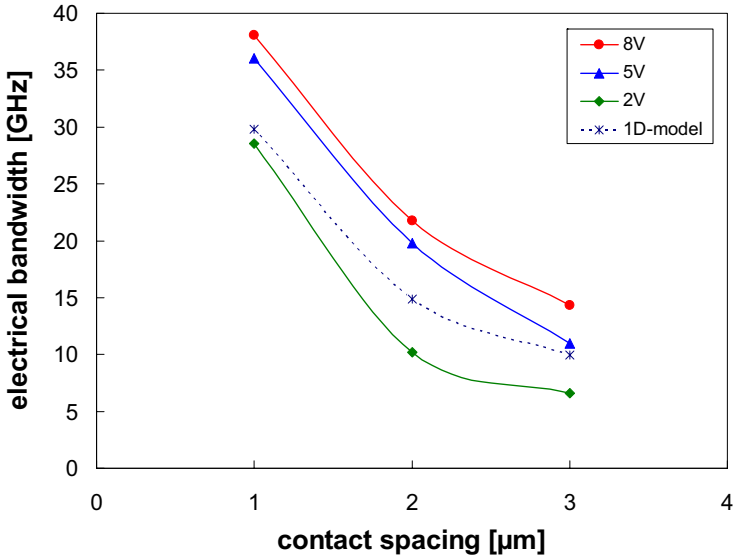


Figure 5.16: Simulated electrical bandwidth versus contact spacing for different bias voltages. The dashed line represent the simplified 1-D simulations

zero over this cross section as the electrons travel to the anode (contact on the right).

Figure 5.15(a) plots the normalized response to the short pulse (impulse response) at a bias voltage of 5V for different contact spacings. These simulations also take into account the RC time constant due to the detector capacitance and a 50Ω load. However, due to the low capacitance, the speed of response is transit time limited. This means that a smaller contact spacing results in shorter impulse response. Figure 5.15(b) plots the influence of the bias voltage on the time response of a MSM detector with 3μm contact spacing. The impulse response consists of a rapidly decaying electron current component and a longer tail caused by the hole current, which is in agreement with our simplified one-dimensional model.

The electrical bandwidth can be calculated by taking the Fourier transform of the impulse response. This is plotted in figure 5.16 for different bias voltages. The dashed line represents the bandwidth calculated using the one-dimensional model. The 1-D model slightly underestimates the bandwidth at higher bias voltages. This is mainly caused by the electron current contribution. When comparing the impulse responses from both models (figure 5.11(a) versus figure 5.15(a)), we see that for a 3μm contact spacing, the electron transit time is in the order of $\sim$45ps for the 1-D model versus $\sim$30ps for the 2-D model.

5.2.3.6 Conclusion

From the 1-D and 2-D models presented in this chapter, we can conclude that for contact spacings that are easily obtainable using contact lithography ($f_s \geq 1\mu m$), the bandwidth is transit time limited. Decreasing the contact spacing and SOI waveguide width to 1μm results in a simulated electrical bandwidth of 30-35GHz. Due to the evanescent coupling to the guided wave MSM detector, there is no severe trade-off between efficiency and bandwidth. Experimental results show that detectors with contact spacings and SOI waveguide widths from 1 to 3μm have the same quantum efficiency. This will be discussed in paragraph 5.4.

Very high-speed operation (>50GHz), could be obtained by patterning transverse finger contacts with sub-μm width and spacing. This could be done by means of e-beam lithography. In [8], the authors fabricated a waveguide coupled InGaAs MSM detector on an InP substrate with transverse fingers, spaced by only 300nm. They demonstrated a bandwidth of 65GHz. The device is shown in figure 5.17.

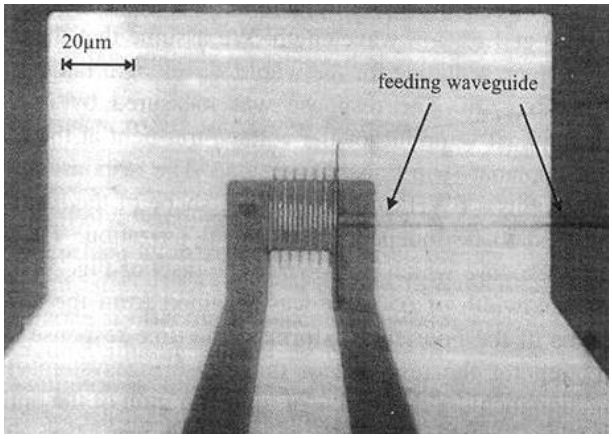


Figure 5.17: MSM detector with 300nm spaced transverse fingers [8]

5.3 Fabrication

5.3.1 Introduction

Figure 5.18 is a schematic overview of the different processing steps. These steps are:

1. Sample preparation (cleaving/dicing)
2. Sample cleaning + removal of cap layer
3. BCB bonding and curing
4. InP substrate removal
5. Removal of sacrificial layers
6. Detector mesa etching
7. BCB insulation
8. Opening of the contact windows
9. Metallization
10. Post-processing

In the next paragraph, we discuss the different steps in more detail.

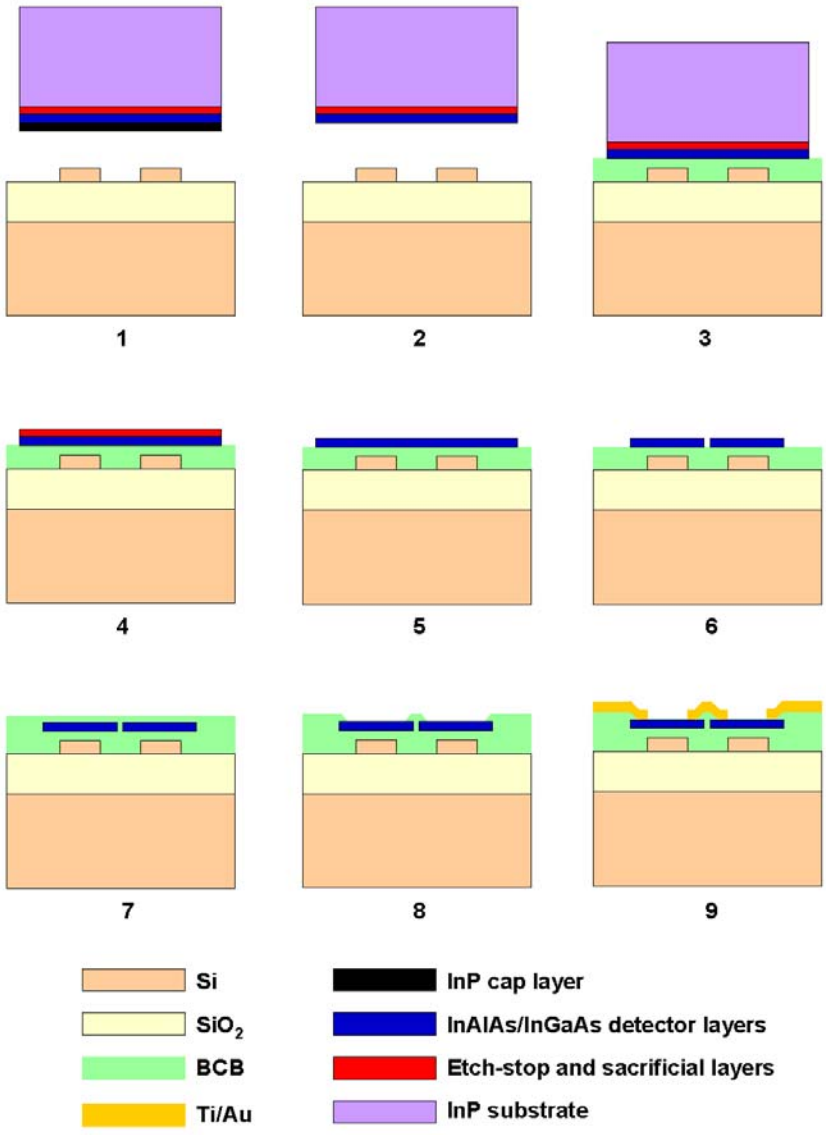


Figure 5.18: Schematic representation of the different processing steps for the fabrication of a thin film bonded MSM detector

5.3.2 Sample preparation, cleaning, bonding and substrate removal

The first processing steps include sample preparation, sample cleaning, BCB bonding and removal of the InP substrate, etch-stop layers and sacrificial layer. The bonding procedure has been described in detail in chapter 4.

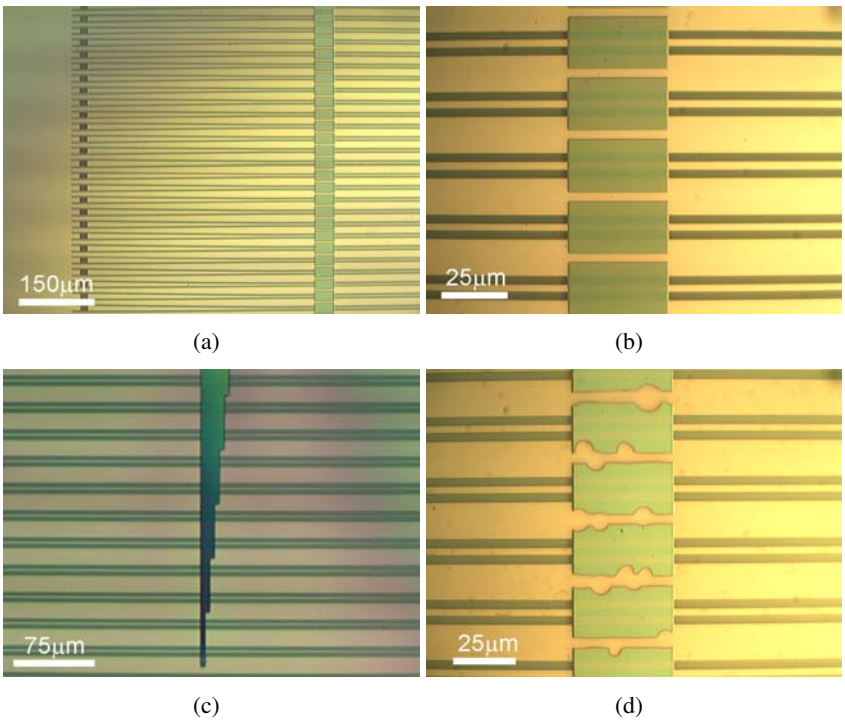
After the removal of the InP substrate using a combination of grinding and chemical etching in HCl:H_2O (3:1), we selectively etch the 200nm thick InGaAs etch-stop layer over the InP sacrificial layer. For this, we use a sulfuric acid based solution (H_2SO_4/H_2O_2/H_2O 1:1:18). This solution etches InGaAs at a rate of $\sim$500nm/min and is very selective to InP. The InP sacrificial layer was incorporated in the MSM layer structure because it is easier to selectively remove InP over InAlAs as compared to InGaAs over InAlAs [34, 35]. The acetic acid based solution
HCL/H_3PO_4/CH_3COOH (1:1:2) etches InP at a rate of 386nm/min and InAlAs with a speed of 4.5nm/min and this results in a selectivity of 85 [35]. This selectivity is not as high as for etching InP over InGaAs using HCl for example so more care should be taken. Etching two times 30s with intermediate rinsing completely removes the InP layer.

5.3.3 Processing after bonding

After sample preparation, bonding and removal of the substrate and sacrificial layers, we obtain an unprocessed 205nm thick InAlAs/InGaAs stack bonded with a thin intermediate BCB layer onto a processed SOI waveguide wafer. The remaining processing steps include definition of the detector mesas, insulation, contact window opening and metallization.

5.3.3.1 Detector mesa etching

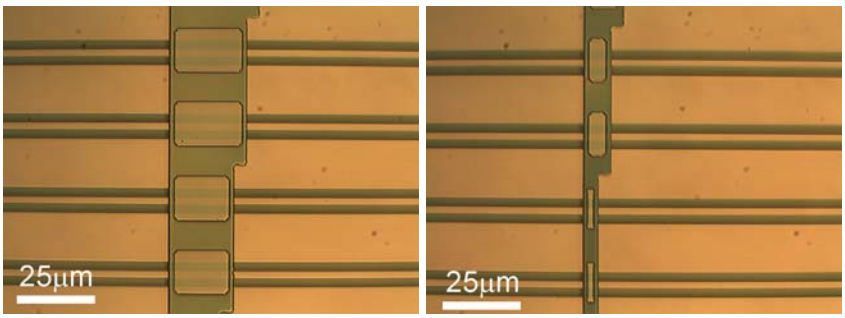
Non-selective wet etching of InGaAs and InAlAs with a H_3PO_4/H_2O_2/H_2O (1:1:20) solution was used to etch the detector mesa down to the BCB bonding layer. Figure 5.19(a) and 5.19(b) are top view pictures of a linear array of 100 detector mesas on a 25μm pitch. Each mesa has a size of 40μm$\times$23μm. A 2μm trench was etched between neighboring mesas in order to electrically insulate them. Figure 5.19(c) shows detector mesas with different lengths from 5μm to 30μm. These mesas were defined using contact lithography with AZ5214 photoresist. Figure 5.19(d) reveals underetching problems caused by bad photoresist adhesion. This problem occurs sometimes but can be avoided by using a dedicated adhesion promotor.



(a) (b)

(c) (d)

Figure 5.19: Top view picture of detector mesas after wet etching



(a) (b)

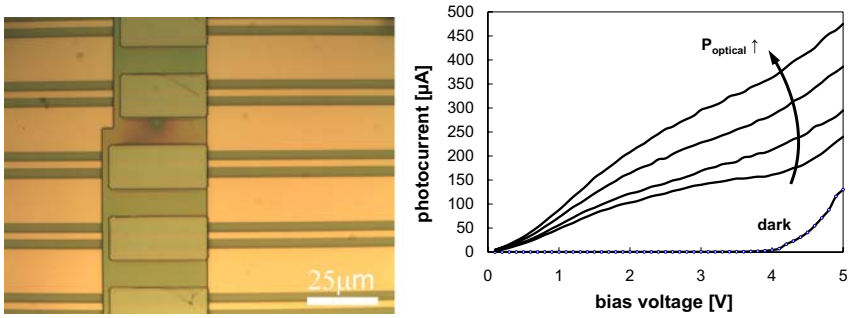
Figure 5.20: Top view picture of the contact windows after plasma etching

5.3.3.2 BCB insulation and contact window opening

In a next step, a BCB insulation layer is spun and a contact window is opened using plasma etching (PE) with a CF_4/O_2 gas mixture. The BCB insulation layers cover the sidewalls of the mesas and contact windows are opened on top of the InAlAs Schottky barrier enhancement layer. Figure 5.20 shows some contact windows on detectors with different lengths.

The opening of the contact window is one of the most critical steps in the detector fabrication process in terms of alignment accuracy during contact lithography. The BCB insulation layer covers the sidewalls of the mesa so that the Schottky metallization, which will be evaporated in a next step, only makes contact with the top InAlAs layer. If the contact window is too large or misaligned as can be seen in figure 5.21(a), the sidewalls are exposed and the metallization will make contact with the InGaAs absorption layer. Due to the small barrier height on InGaAs (paragraph 5.2.1), this will result in an excessive dark current. Also, the ohmic behavior of these contacts on InGaAs will result in photoconductor like current/voltage (I/V) characteristics. In this case, the photocurrent increases linearly with increasing bias voltage without saturating. The higher the optical power, the larger the slope of the I/V curves. It is obvious that this has to be avoided for photodetector operation.

Figure 5.21(b) shows an I/V measurement of a detector that suffers from this problem due to misalignment. The dark current is in the order of μA's instead of nA's and the photoconductor I/V characteristics are clearly present. The photocurrent does not saturate for increasing bias voltages.



(a) (b)

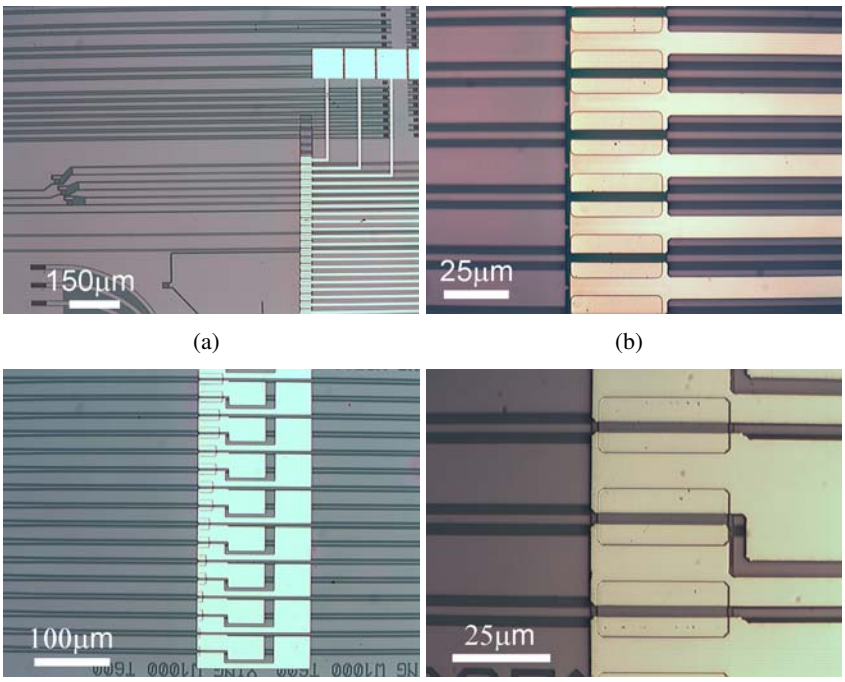
Figure 5.21: (a) Top view picture of misaligned contact windows and (b), corresponding I/V characteristics for different waveguide powers. A large dark current and photoconductor like behavior are present

5.3.3.3 Metallization

The last essential step in the process (before eventual plating and passivation) is the definition of the two coplanar Schottky contacts on each detector. The metallization for these contacts consists of a 20nm Ti and a 200-300nm Au layer which are deposited by means of thermal evaporation followed by a lift-off process. Figure 5.22 shows some top view pictures of two different contact layouts. The detectors are processed on 3μm wide waveguides and have a pitch of 25μm. In order to reduce the total chip area, each Ti/Au contact is a common contact of two neighboring detectors as can be seen. Other layouts (in which all detectors have a common ground contact for example) are also possible. In figure 5.22(a) and 5.22(b), each contact ends in a large $150 \times 150 \mu m^2$ contact pad which allows for wire-bonding. In figure 5.22(c) and 5.22(d), a more compact metallization schema is demonstrated.

It is known that the quality of Schottky contacts on InAlAs is strongly dependent on the surface quality of the InAlAs layer [36]. Prior to the metallization, we treated the surface with NH_4OH/H_2O (1:10) for 20s [37] to remove the native oxide layer. Other treatments such as buffered HF [38] and succinic acid [36, 39] etch have also been reported.

Figure 5.23 is a focused ion beam (FIB) cross section of the right half part of the detector after metallization. The right Ti/Au contact, the 205nm thick epilayer stack, the 100nm thick BCB bonding layer and the 220nm high SOI waveguide are clearly visible.



(a) (b)

(c) (d)

Figure 5.22: Top view picture of arrays of MSM detectors after metallization

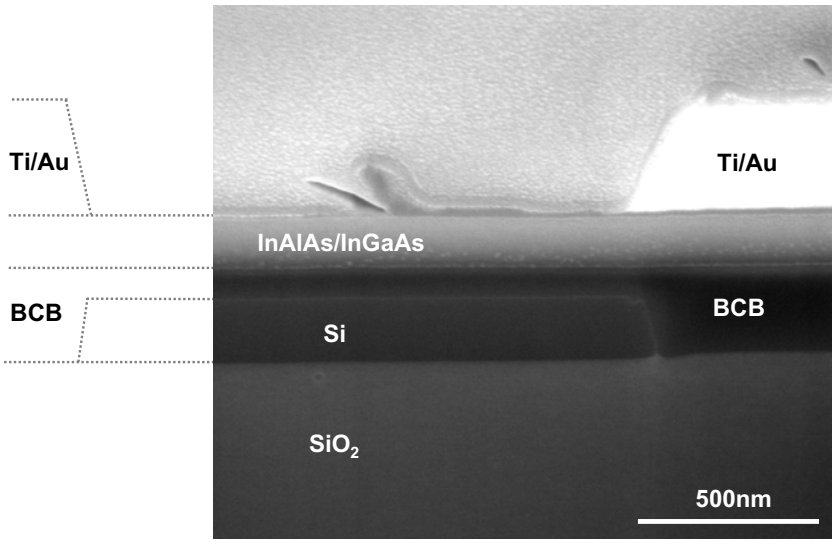


Figure 5.23: Cross section of the thin-film MSM detector bonded on top of an SOI waveguide

5.3.3.4 Post-processing

If necessary, the contact pads can be gold-plated (e.g. for wire-bonding) and a passivation layer can be deposited (BCB, oxide, nitride, ...) to prevent oxidation and to increase the long term reliability of the device.

5.4 Characterization

In this section, we report on the in-depth characterization of the fabricated detectors: responsivity, efficiency, dark current, linearity, reliability and bandwidth.

5.4.1 Introduction

To characterize the detectors, we make use of a tunable laser source which is connected to a standard single mode fiber. Polarization wheels allow to control the polarization. TE polarized light is coupled into the nanophotonic SOI waveguides using fiber couplers. This was explained in detail in chapter 2. These fiber couplers are shallowly etched one dimensional gratings, which couple near-vertical incident light into a 10μm wide ridge

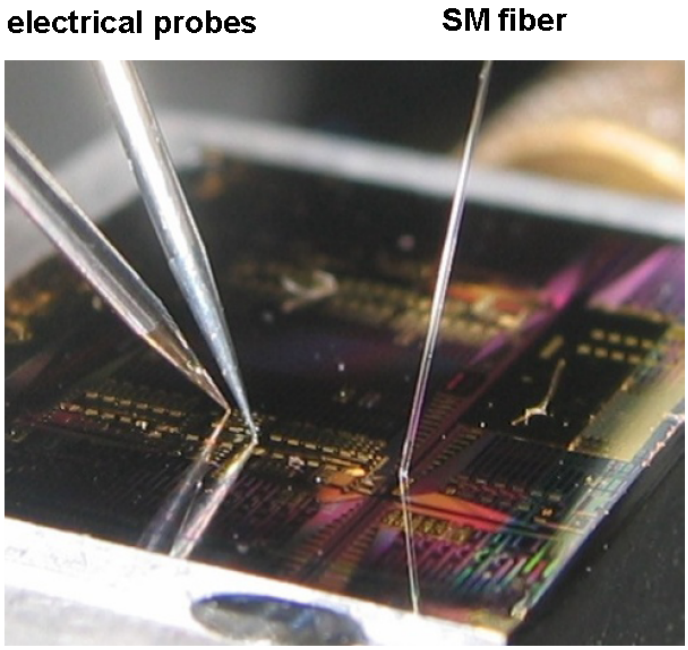


Figure 5.24: SOI chip on an electro-optical measurement setup. Electrical probes and an optical fiber are visible

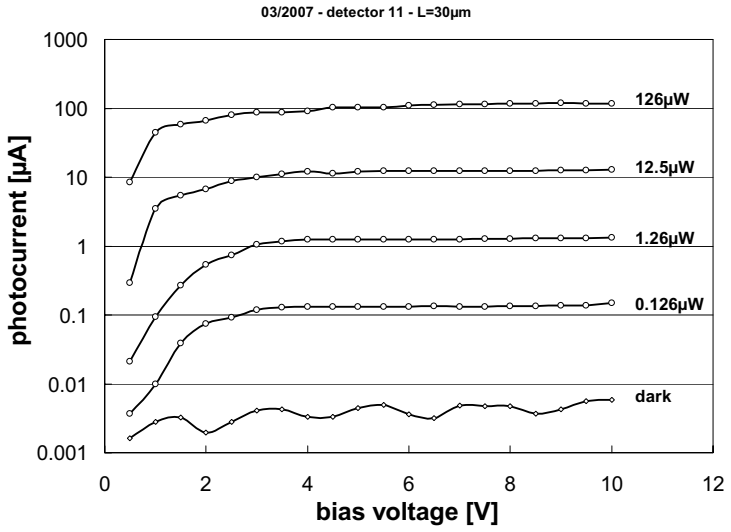
waveguide. These waveguides are then tapered down to 3μm wide waveguides using adiabatic tapers. For high power and linearity measurements, we connected the output of the tunable laser source to an Erbium doped fiber amplifier (EDFA) followed by an adjustable optical attenuator.

Figure 5.24 is a picture of a sample on the measurement setup. The two electrical probes bias a photodetector and the optical fiber is also clearly visible.

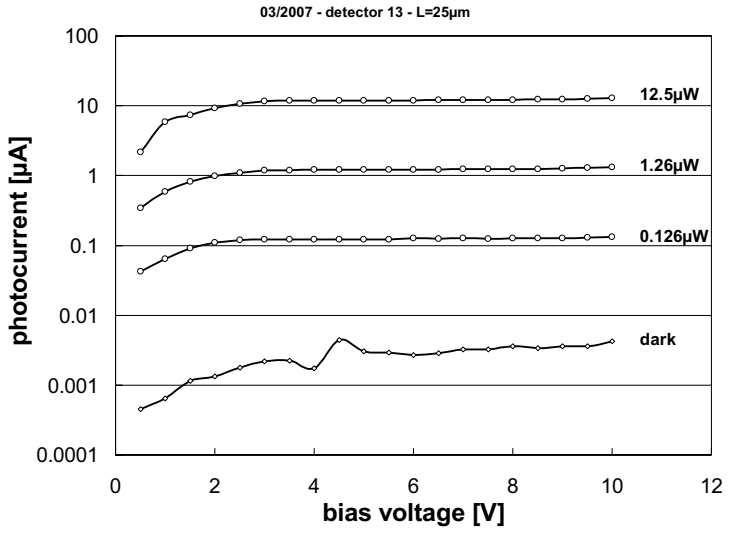
5.4.2 Photocurrent, responsivity and efficiency

5.4.2.1 Characterization of the photocurrent and responsivity

In this paragraph, we discuss measurement results of three detectors with different lengths, fabricated on one SOI waveguide sample. These detectors have a Schottky contact spacing of 3μm and are processed on top of a 3μm wide, deeply etched SOI waveguide with a height of 220nm. The BCB bonding layer thickness is $\sim$100nm (Figure 5.23). First of all, we characterized the fiber couplers by measuring the fiber-to-fiber transmission of



(a)



(b)

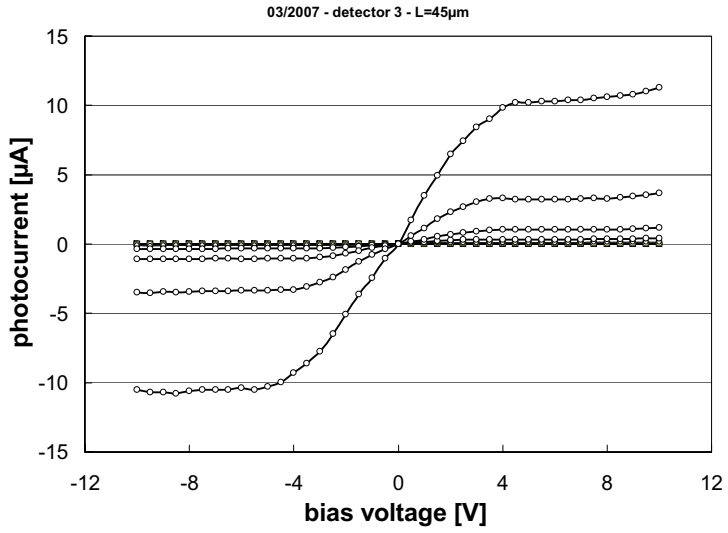
Figure 5.25: Measured I/V characteristics for (a), a 30μm and (b), a 25μm long detector

a reference waveguide on that sample. The measured coupling efficiency of the fiber couplers on these particular chips was 25% at a wavelength of 1.57μm and 21% at 1.55μm. These values are used to calculate the incident power on the detectors.

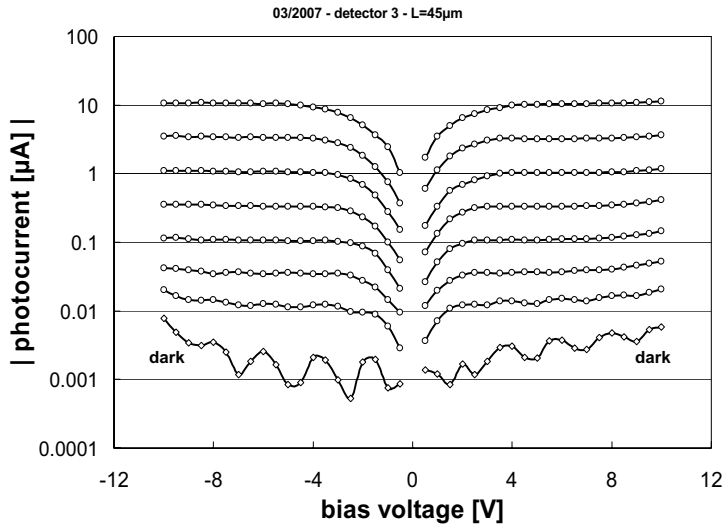
Figure 5.25(a) shows the dc current-voltage (I/V) characteristics of a 30μm long detector for different illumination conditions and a wavelength of 1.55μm. The dark current of the device was 4.5nA at a bias voltage of 5V. The power coupled into the fiber was varied from 600nW up to 600μW in steps of 10dB. Taking into account a fiber coupler efficiency of 21%, the SOI waveguide power varied from 126nW up to 126μW. The losses in the 3μm wide waveguides can be neglected because of their low propagation loss ($\sim$0.1dB/cm) and the short length from fiber coupler to detector ($\sim$500μm including taper). The photocurrent increases linearly with increasing waveguide power. For bias voltages above the flat-band voltage (4-5V), the on-chip responsivity (not taking into account fiber to chip coupling losses) reaches 1A/W at a wavelength of 1.55μm, corresponding with a quantum efficiency of 80%.

This responsivity showed no major change for different detector lengths ranging from 25μm to 40μm. Figure 5.25(b) plots the I/V characteristics of a 25μm long detector processed on the same SOI sample (100nm bonding layer). Again, the responsivity at $\lambda = 1.55\mu$m is 1A/W and the dark current and flat-band voltage are comparable. Those two measurement results demonstrate the good reproducibility of the photodetector performance. The measured quantum efficiencies are in good comparison with the simulation results discussed in paragraph 5.2.2. We have to take into account an error margin of about $\pm$20% on the measured responsivity. This error margin is due to the inaccuracy in the determination of the optical power that falls onto the detectors. This is strongly dependent on both the exact fiber coupler efficiency but also the waveguide loss to a smaller extent as mentioned above. During this work, we fabricated hundreds of these detectors and we measured a responsivity of $\sim$1A/W in a very reproducible way.

Figure 5.26 plots the I/V characteristics of a 45μm long detector. The waveguide power varies in a 30dB range from 12.6nW up to 12.6μW in steps of 5dB. Again, a low dark current ($\sim$nA's) and a nice linear behavior are demonstrated. These MSM detectors are symmetrical devices and this characteristic is clearly visible in a plot of the absolute value of the photocurrent versus bias voltage (figure 5.26(b)).



(a)



(b)

Figure 5.26: Measured I/V characteristics for a 45μm long detector on a linear and logarithmic scale to demonstrate symmetrical behavior

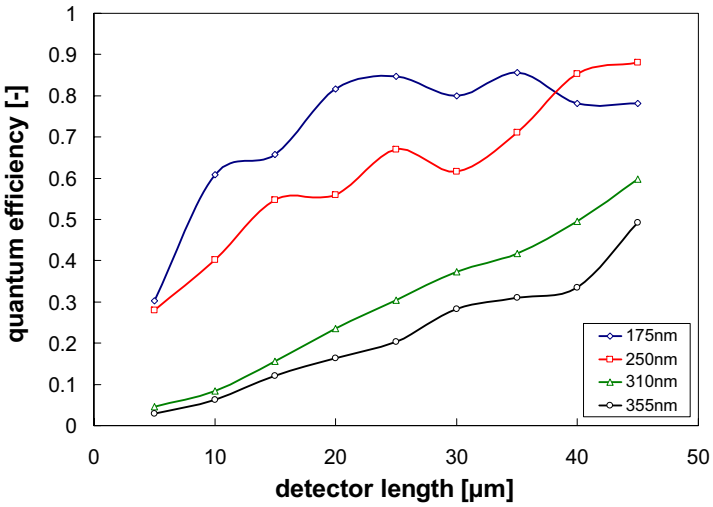


Figure 5.27: Measured quantum efficiency versus detector length for different bonding layer thicknesses

5.4.2.2 Influence of bonding layer thickness and detector length on efficiency

For most applications, the higher the detector efficiency, the better. For some applications however like power monitoring, we need a detector that only taps a small portion of the light from the waveguide. This can be accomplished by shortening the detector or by increasing the bonding layer thickness.

To experimentally investigate the influence of the bonding layer thickness and the detector length on the efficiency, we fabricated samples with different BCB bonding layer thicknesses by varying the dilution and the spinning speed of the mesitylene/BCB solution. On each of these samples we fabricated detectors with lengths ranging from 5μm up to 45μm. After processing and characterization, focused ion beam (FIB) cross sections were used to measure the thickness of the bonding layer. Figure 5.20 and figure 5.22(c) are pictures of these samples before and after metallization. respectively.

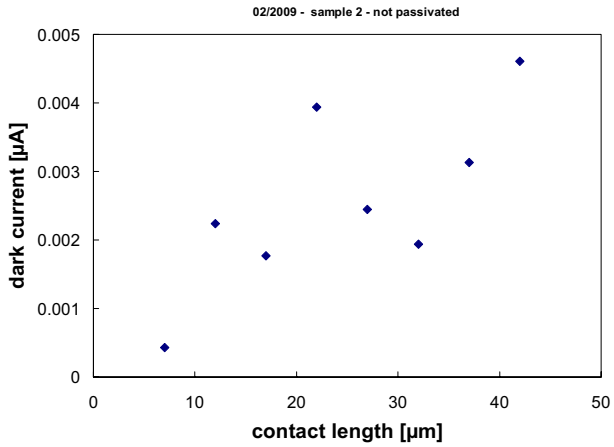
The results of these efficiency measurements can be seen in figure 5.27. Four different samples were processed and after FIB inspection, we found BCB thicknesses of 175nm, 250nm, 310nm and 355nm respectively. The detector efficiency was measured at a wavelength of 1.55μm and a bias

voltage of 5V. For the thinnest bonding layer (175nm), maximum detector efficiency is obtained for detectors with lengths above 20μm. The quantum efficiency saturates around 80-90% which is in agreement with the results shown in the previous paragraph. For the thicker bonding layers (310nm and 355nm), we observe an almost linear relation between efficiency and detector length for lengths ranging from 5 to 45μm. For the sample with the 310nm BCB layer, a 10μm length increase results in a 15% efficiency increase. These results are in good agreement with the simulation results shown in paragraph 5.2.2, figure 5.4. The only discrepancy arises from the fact that these simulations do not take into account metal absorption losses.

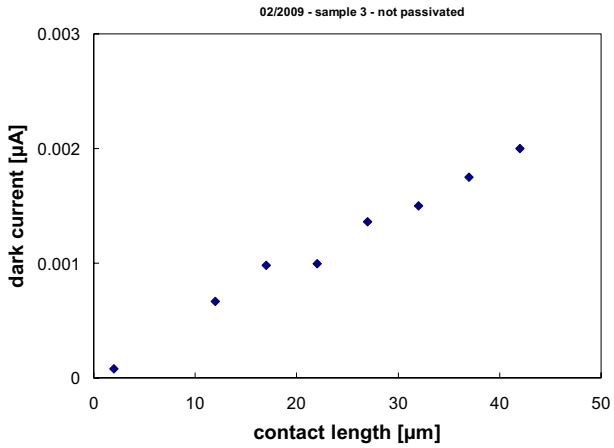
From these measurements, we can conclude that by using thicker bonding layers (>300nm), it is possible to control the absorbed power fraction for power monitor applications (see also chapter 6). On the other hand, very thin bonding layers (<200nm) result in very efficient and very compact devices. The advantage of short detectors is threefold: besides the compactness, short detectors have a low capacitance and a low dark current. This is because both capacitance and dark current scale with detector length. We demonstrated bonding layer thicknesses down to 50nm. However, alignment of the contact mask during lithography becomes very critical for short (<5μm) detectors, especially the definition of the contact window.

5.4.3 Dark current

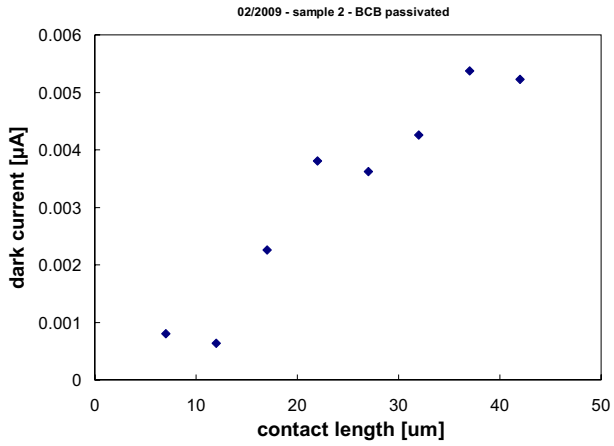
We fabricated detectors with different lengths ranging from 5μm to 45μm and measured the dark current. The width of each contact on the detector mesa is 7.5μm and the length is equal to the detector length minus 3μm. This is because the insulation layer overlaps 1.5μm on the front- end rear-edge of the detector mesa (figure 5.20 and 5.22). Figure 5.28 plots the dark current as a function of contact length at room temperature and a bias voltage of 5V. Measurement results for three different samples are shown. In figure 5.28(a) and 5.28(b) the dark current of two unpassivated devices is plotted. Figure 5.28(c) shows the dark current of a passivated device. The passivation consists of spinning and hard curing (1h, 250°C) a layer of BCB on the detectors after metallization. As can be seen, the dark current increases linearly with contact length (and thus contact area). For unpassivated samples, dark currents between 1nA and 5nA were measured at 5V bias for 37μm long and 7.5μm wide contacts (=40μm long detectors). This corresponds with a very low dark current density of 0.35-1.8mA/cm^2. Dark currents of passivated devices are usually somewhat higher (between 5nA and 10nA). This corresponds with dark current densities of 1.8-3.5mA/cm^2. This is probably due to the curing of the BCB layer (1h, 250C).



(a) Unpassivated sample 1

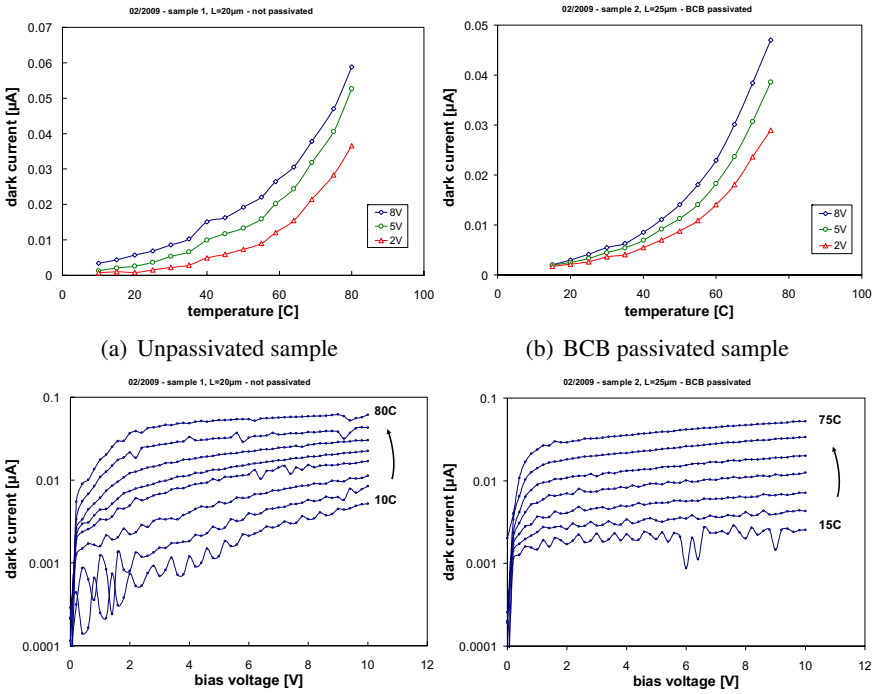


(b) Unpassivated sample 2



(c) BCB passivated sample

Figure 5.28: Dark current versus contact length for different samples



(a) Unpassivated sample

(b) BCB passivated sample

(c) Unpassivated sample

(d) BCB passivated sample

Figure 5.29: Influence of temperature on dark current

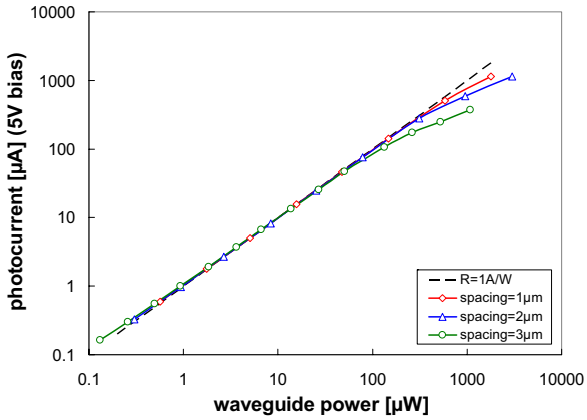


Figure 5.30: Measured photocurrent versus waveguide power for 40μm long detectors and different contact spacings (logarithmic scale)

For certain applications (e.g. automotive, optical interconnect on CMOS), these detectors have to be able to operate at elevated temperatures (70°C-80°C). We performed some experiments to measure the performance of the MSM detectors at elevated temperatures. I/V characteristics and quantum efficiency under illumination are not significantly affected by elevated temperatures. The dark current however is highly temperature dependent. This is due to the strong temperature dependent behavior of the leakage current in Schottky contacts. Fig. 5.29 shows the dark current for different temperatures ranging from 10°C to 80°C. Both the behavior of an unpassivated (left) and a passivated sample (right) are shown. As can be seen, there is a tenfold increase in dark current, which was to be expected. Unpassivated and passivated samples have the same temperature dependency.

5.4.4 Linearity

For most applications, a linear I/V relation between incident power and photocurrent over a wide range of optical powers is important. Figure 5.30 shows the measured photocurrent of detectors with a Schottky contact spacing and SOI waveguide width of 1, 2 and 3 μm at 5V bias as a function of waveguide power. The dashed line represents a responsivity of 1A/W. For devices with a larger contact spacing, the output saturates faster due to carrier screening effects.

From these measurements, we extracted the 1dB saturation current. This is the photocurrent at which the responsivity falls back to 80% of the

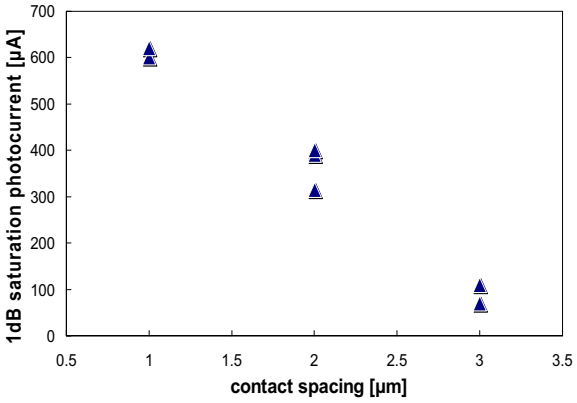


Figure 5.31: Measured 1dB saturation photocurrent as a function of contact spacing for 7 different samples

responsivity at low optical powers. Figure 5.31 plots this 1dB saturation current as a function of Schottky contact spacing for seven different detectors fabricated during three different processing runs. The measured data demonstrates the good reproducibility of the detector characteristics over different fabrication runs. Again, it is clear that the saturation current increases with decreasing contact spacing. The 1dB saturation photocurrent for a detector with 1μm contact spacing and waveguide width is 610μA (averaged measurement over 2 fabrication runs), resulting in a dynamic range of $>$40dB.

5.4.5 Reliability

To assess the long term reliability, some samples were subjected to damp heat experiments. For these tests, the samples are put in a furnace for 48h at a temperature of 85°C and a humidity of 85%. Visual inspection revealed no degradation of the detector and bonding interface after 48h of damp heat experiment. However, there might be a reliability issue due to oxidation of the to InAlAs layers. Figure 5.32 shows the measured dark current of an unpassivated detector (length = 40μm, temp = 20°C) before and after the damp heat experiment. As can be seen, the dark current significantly increased after the experiment. On the other hand, the I/V characteristics under illumination did not change significantly, neither did the quantum efficiency. Passivation is expected to solve this reliability issue. The detector or the entire SOI chip could be encapsulated to shield the photodetectors

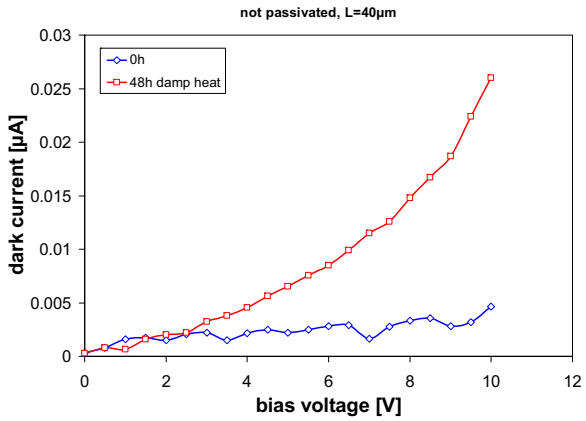


Figure 5.32: Dark current of an unpassivated sample before and after a 48h damp heat experiment (85%/85C)

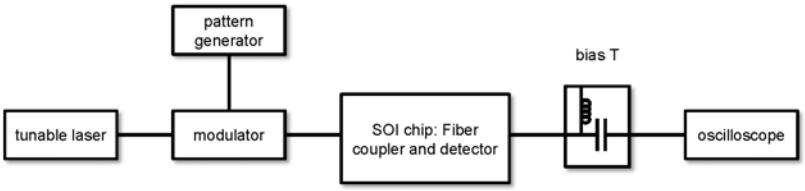


Figure 5.33: Setup for high speed measurements

and to prevent oxidization. However, in depth reliability experiments on passivated samples have not been carried out in this work.

5.4.6 Bandwidth

A scheme of the setup for measuring the detector bandwidth is shown in figure 5.33. The light of a tunable laser is externally modulated and coupled into the SOI chip by means of fiber couplers. The modulator is driven by a pattern generator. An RF probe is connected to the on-chip contact pads on one side and to a bias-T on the other side which is used to deliver the DC bias. The RF signal is measured using an oscilloscope.

The measured (normalized) frequency response of two photodetectors is shown in figure 5.34. We launched light at a wavelength of 1550nm into the waveguide detector, with a constant average power of $\sim$150μW and we measured the response for frequencies up to 12GHz, which was the limit of

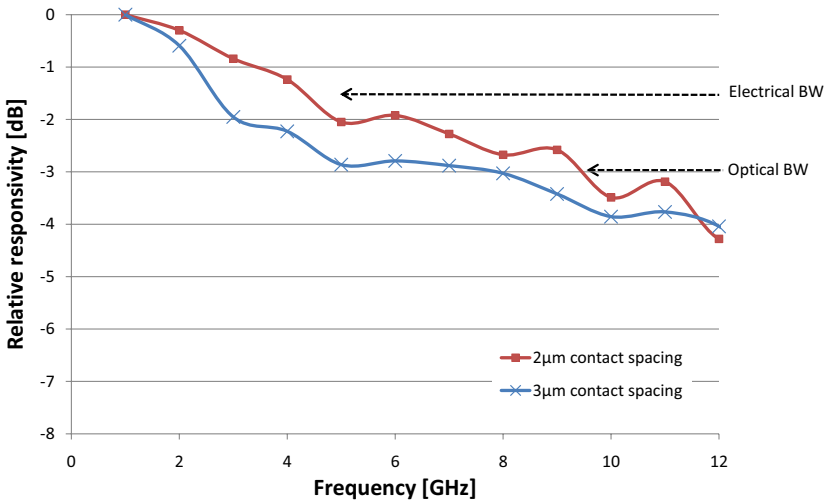


Figure 5.34: Measured frequency response for detectors with 3μm and 2μm contact spacing

the modulator used for these experiments. The optical bandwidths of detectors with 2μm and 3μm contact spacing and SOI waveguide width were measured to be 9.5GHz and 8GHz respectively at 8V bias. The electrical bandwidths were 4.5GHz and 2.5GHz respectively. The optical signal and the corresponding electrical detector signal for an input frequency of 10GHz are shown in figure 5.35

The measured bandwidth is lower as compared to the values predicted by simulation as discussed in a previous section. This can have different causes. First of all, we have not used on-chip 50Ω coplanar transmission lines. Also, we did not measure the frequency response of the bias-tee, RF cables and high speed probe, so we were not able to factor out their influence from the measurement results. For sure, more experiments are needed to be able to determine the bandwidth limiting factor. Also, more measurements to determine the influence of the optical power, the bias voltage and the electrode spacing need to be carried out to fully characterize and understand the high speed behavior.

We also measured eye diagrams for bit rates of 1Gbps, 3Gbps, 5Gbps and 10Gbps. This is shown in figure 5.36. Both the modulated optical input signal and the electrical output signal are visible. This is a detector with 2μm contact spacing and 8V bias. The eye closes for bit rates around 10GBps. At higher frequencies, the electrical eye is disturbed by the limited bandwidth of the optical modulator, which has a rise time of $\sim$50ps. The

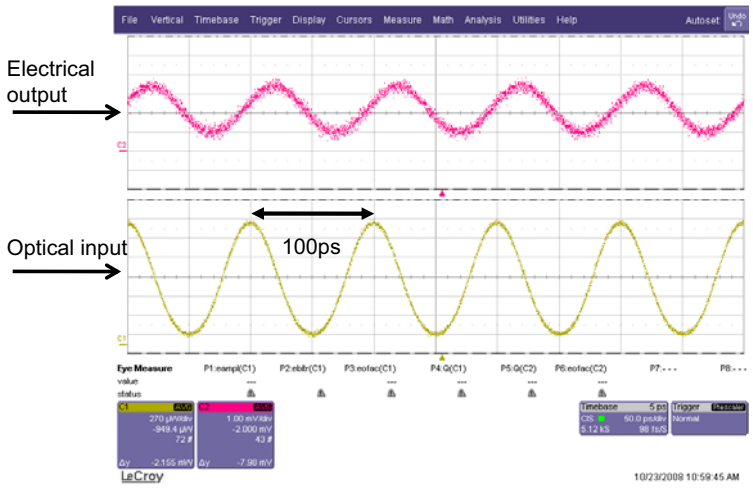


Figure 5.35: 10GHz measured optical signal from modulator and detected electrical signal from on-chip detector

measurement also suffers from a lot of noise. This is mainly because the relatively weak electrical signals are at the limit of the sensitivity of the oscilloscope. We believe that be inserting a low noise amplifier, the signal to noise ratio and the quality of the eye diagrams should increase.

5.4.7 Spectral response

For the measurement of the spectral response, light was launched into a cleaved SOI facet using a lensed fiber. This was done because horizontal coupling has a much broader spectral bandwidth as compared to vertical coupling using fiber couplers. Figure 5.37 shows the quantum efficiency (QE) for a 25μm long detector for wavelengths from 1.5μm to 1.64μm. These graphs are normalized so that maximum QE corresponds with 100%. These measurements show that efficient detection is possible for wavelengths up to at least 1.65μm, which corresponds to the bandgap wavelength of InGaAs lattice matched to InP.

If we compare this measurement results with the simulation results as presented in figure 5.7, we see that the measured QE decreases slightly faster than expected for increasing wavelengths. This might be caused in part by the wavelength dependency of the horizontal coupling which was not filtered out for these measurements.

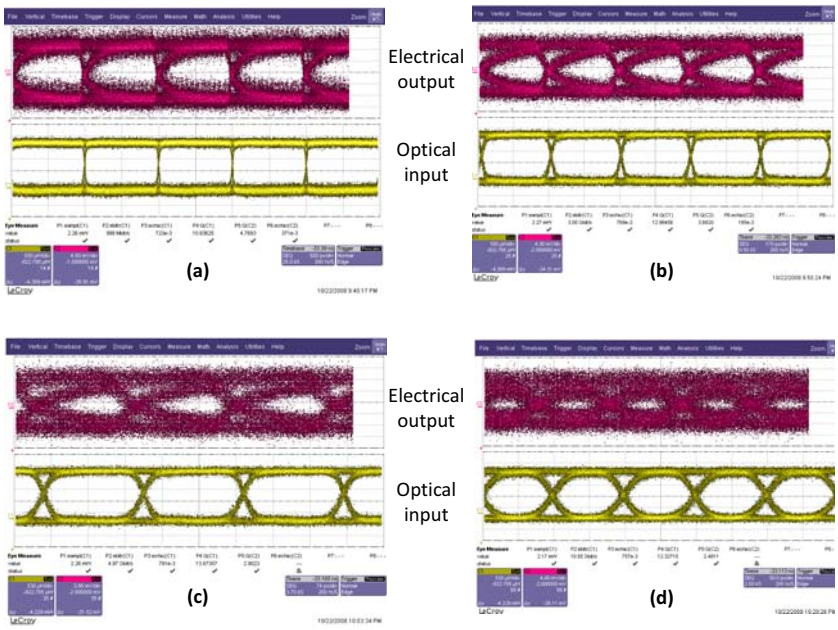


Figure 5.36: Eye diagrams at different bit rates: (a) 1Gbps, (b) 3Gbps, (c) 5Gbps and (d) 10Gbps

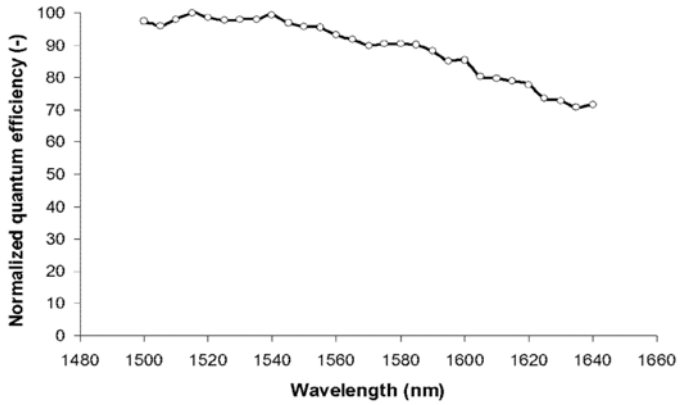


Figure 5.37: Normalized quantum efficiency as a function of wavelength for a 25μm long detector

5.5 Process development and optimization of detector characteristics

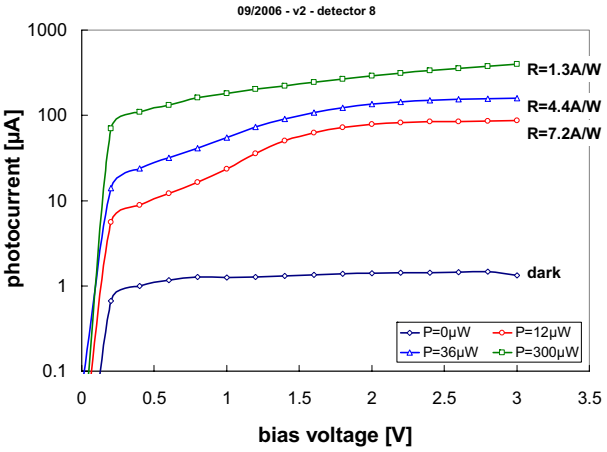
The detector performance we presented in this chapter was the results of an intense process optimization. Initial devices that were fabricated showed different problems: high dark current, asymmetric behavior and the presence of large gain at low optical powers. However, these devices were fabricated using standard processing techniques for the fabrication of III-V lasers, LEDs and PIN detectors: definition of a mesa by means of ICP/RIE (inductive coupled plasma etching/reactive ion etching), deposition of an insulation layer (BCB, SiO_x, SiN_x, ...) and opening of the contact window using ICP/RIE. To overcome these problems, we had to develop new processes.

5.5.1 Gain and nonlinear behavior

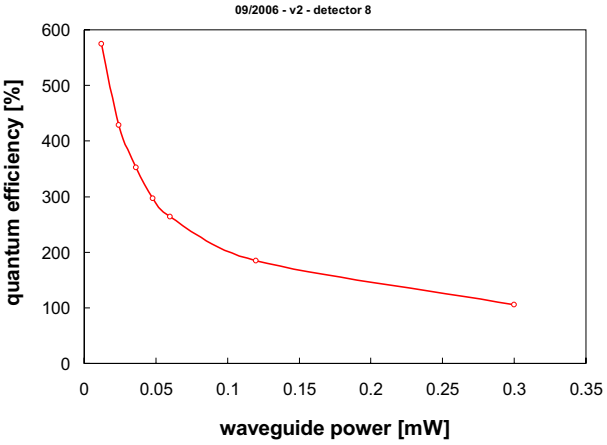
Figure 5.38(a) shows the measured photocurrent as a function of bias voltage for different levels of illumination for one of our first prototypes, fabricated using the standard processing technology for III-V optoelectronic components as described above. First of all, the dark current of this device is in the order of 1μA, which is about 3 orders of magnitude higher than the dark current of identical devices fabricated using the optimized processing. The dark current of optimized devices is in the order of 1nA.

Secondly, we observe a strong nonlinear current-power behavior. In the I/V curves presented in figure 5.38(a), we varied the waveguide power from 12μW over 36μW up to 300μW. The measured responsivity is 7.2A/W, 4.4A/W and 1.3A/W respectively. The wavelength is 1.55μm. At this wavelength, 100% quantum efficiency corresponds with a responsivity of 1.24A/W. This means that, especially at lower optical power levels, a very large gain is present. In figure 5.38(b), we plotted the quantum efficiency versus waveguide power. As can be seen, at low optical powers, the efficiency is very high ($> 500\%$). For higher optical powers, the efficiency levels out to sub 100% values. This behavior was observed in all first generation fabricated detectors: a high efficiency at low powers before it reaches the expected value of $\sim 80\%$ at high optical powers.

In order to solve this issue and to determine its origin, we completely reviewed each processing step in detail. We achieved a breakthrough by fabricating vertically illuminated detectors on dummy silicon samples. These devices were fabricated by evaporating two large Ti/Au Schottky contacts ($100\mu\text{m}\times100\mu\text{m}$) directly onto the InAlAs top layer without the need for etching the detector mesa or a contact window. The spacing between the



(a) I/V characteristics for different waveguide powers powers at $\lambda = 1.55\mu$m



(b) Quantum efficiency as a function of waveguide power

Figure 5.38: Detectors with high dark current and large gain at low optical powers

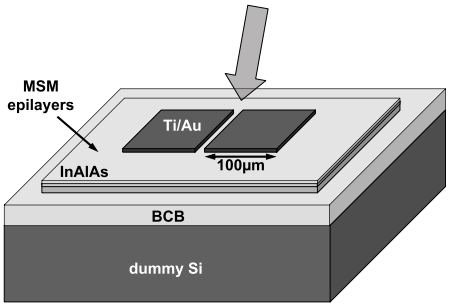


Figure 5.39: Vertically illuminated MSM detectors on dummy SOI samples

Schottky contacts is 5μm. Above this 5μm wide gap, we positioned an optical fiber for vertical illumination. A schematic drawing of this test structure is shown in figure 5.39. We characterized these devices and although the quantum efficiency of these device was very low due to vertical illumination and the 145nm thin InGaAs absorption layer, we observed a nice linear relation between the generated photocurrent and the optical power. From these measurements, we concluded that the ICP/RIE dry etching of the detector mesa and/or contact window was the cause of the large gain observed in the initial waveguide coupled MSM detectors.

Although both InGaAs/InAlAs MSM detectors with dry [8, 40] and wet [38, 41] etched mesas have been reported in literature, it is well know that plasma etching or ion beam etching can induce structural and electrical damage caused by the chemically or physically active species in the plasma or the energetic ions [42, 43]. This damage can deteriorate the electronic and optoelectronic properties of the semiconductor material [44]. This problem is also encountered during the processing of InGaAs/InAlAs/InP high electron mobility transistors (HEMTs) [42].

The current mechanisms that could be responsible for the gain at low optical powers are described by DeCorby and coworkers [45]. The authors state that gain is due to long-lifetime trapping of photogenerated electrons or holes, field enhancement at the anode or cathode, and subsequent secondary injection of holes or electrons, respectively. Low optical power is sufficient to saturate the traps, so their contribution to photoresponse becomes negligible at higher powers. Similar gain mechanisms have also been described elsewhere [46, 47].

To solve this issue, we investigated the possibility of replacing the ICP/RIE dry etching of both the detector mesas and the contact windows. This will be explained in the following paragraphs.

5.5.2 Definition of detector mesa

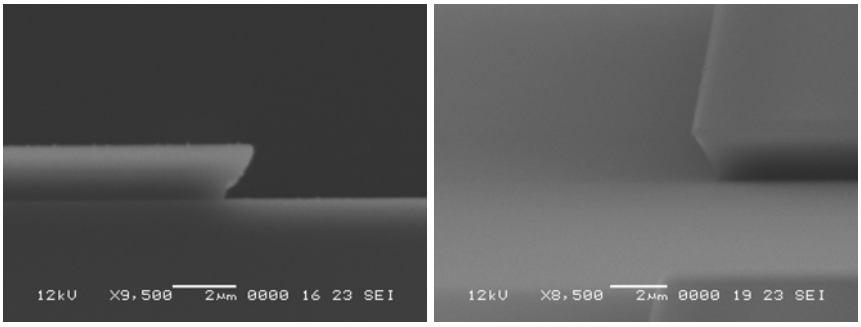
For the definition of the InAlAs/InGaAs detector mesa, we successfully replaced the dry etching by wet chemical etching. We experimented with different etch solutions and we obtained nice results using a $H_3PO_4/H_2O_2/H_2O$ (1:1:20) solution. This solution non-selectively etches both InAlAs and InGaAs. Experimentally, we observed that an etching time of 54 seconds completely etches the 205nm thick InGaAs/InAlAs layer stack. The etch time is a very important parameter and should be strictly controlled. Both exceeding the optimum etching time or stopping the etching too early can be problematic. If the InGaAs layer is not completely removed, a large part of the SOI sample will be covered with a strongly absorbing layer resulting in excessive on-chip loss. Etching too long will result in undercut. This undercut can become problematic when opening the contact windows. If the mesa sidewalls are exposed, it will destroy the I/V characteristics (see paragraph 5.3.3.2). We found that the mesa etching becomes less critical when the single lithography/etch step is replaced with a double litho/etch step. In a first step the detector mesas are etched and care is taken to avoid undercut (no over-etching). If some InGaAs is left on the BCB bonding layer on top of the SOI waveguide circuit , it can be removed during the second etch step. During this step, the mesas are protected with a slightly larger photoresist pattern (2μm larger on each side for example). This way, the remaining InGaAs can be safely removed and the mesas are protected.

5.5.3 Insulation and opening of the contact windows

For the replacement of the ICP/RIE dry etched contact windows in the BCB insulation layer, different approaches were investigated. The two most successful approaches turned out to be replacing the BCB with a photopatternable polymer and replacing the high energetic ICP/RIE etching by low power plasma etching (PE).

5.5.3.1 Photosensitive polymer

By replacing the BCB insulation layer with a photopatternable polymer, dry etching can be avoided. We performed experiments with PI-2737 from HD microsystems. This is a negative photodefinable polymer sensitive for illumination using a mercury broadband spectrum (λ=350-436nm) or G-line exposure (λ=436nm). We experienced problems relating to the slope of the sidewalls. In order to deposit the metallization on top of the contact windows, a nice positive slope is necessary. We obtained negative slopes and severe undercutting in some cases (see figure 5.40). We believe this was



(a) (b)

Figure 5.40: Sidewalls of patterned polyimide

caused by illumination problems during contact lithography. As a results, no working devices have been processed using this approach. We believe that the use of photodefineable BCB (Dow Chemical) can be a good alternative due to its compatibility with the BCB bonded samples. However, this route was not explored.

5.5.3.2 Plasma etching versus ICP/RIE etching

BCB can easily be dry etched using photoresist as a mask. The etch selectivity between BCB and the photoresist film is usually around 1:1. Since silicon is present in the backbone of BCB both oxygen and fluorine are required for dry plasma etching [48]. In the cleanrooms of the Photonics Research Group, dry etching of BCB is done using a mixture of oxygen and a fluorine containing gas: O_2/CF_4 or O_2/SF_6. Mostly, ICP/RIE etching is used for this task with a gas flow of 50sccm O_2/SF_6 (4:1) and an RF/ICP power of 150/50W. Using this standard recipe however, we noticed a bad detector performance as described above (gain, high dark current). We believe this is due to defects induced in the semiconductor during ICP/RIE etching.

The goal of replacing the ICP/RIE etching with plasma etching (PE) was to decrease the induced damage and defects in order to obtain better photodetector characteristics. PE is done by using a gas mixture inside a chamber to obtain ions that will react with the target material. The ionization of the gases is done by radio frequency (RF) excitation emitted by an electrode at the top of the chamber. The target wafer is placed on an electrode connected to the ground. The random movement of the ions inside the chamber makes them reach the target and a chemical reaction etches

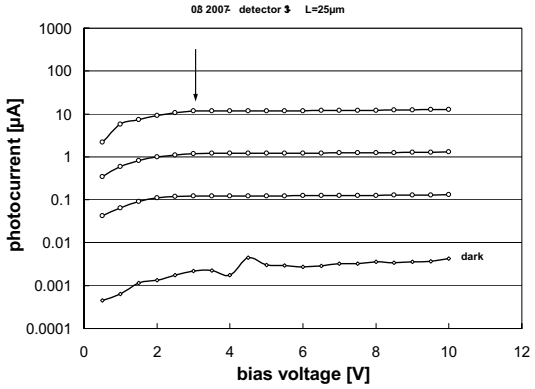
the material. As a result of the pure chemical reaction, PE is isotropic. RIE is a variation of PE. The principle of etching is almost the same, but this time, the chamber top electrode is connected to the ground and the wafer is placed on the excitation electrode. As a result of self-bias, the ions are accelerated in the direction of the wafer and next to a chemical etching process, a physical etching will also take place. This has consequences on the etching process: the etching is mainly anisotropic and surface damage will be induced.

We experimented with PE of the BCB insulation layer using a mixture of O_2 and CF_4. The recipe obtained after process optimization was the following. A 4.2:1 ratio of O_2 and CF_4, a chamber pressure of 300mtorr, a gas flow of 50sccm O_2 and 12sccm CF_4 and a low RF power of 8W(load). This resulted in an etch rate of $\sim$50nm/min: a contact window in a 300nm thick BCB insulation layer is opened in $\sim$6min. The samples are visually inspected after etching to make sure the contact windows are opened and the InAlAs SBEL layer is exposed.

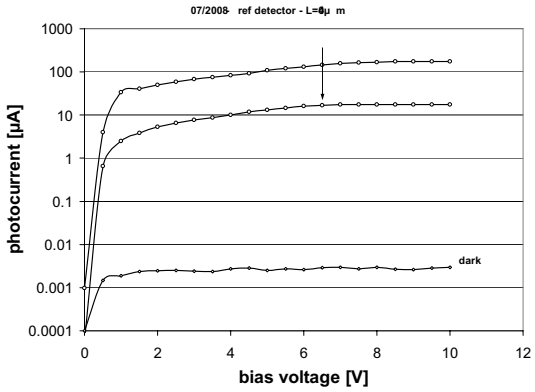
5.5.4 Results of process optimization and conclusion

The replacement of dry etching by wet chemical etching for the definition of the contact windows and reactive ion etching (RIE) by plasma etching (PE) for the opening of the contact windows resulted in a huge improvement of the detector characteristics. No more gain was observed, the detectors showed a linear current-power behavior, the dark current was reduced by a few orders of magnitude to values in the nanoampere range and a quantum efficiency (QE) of $\sim 80\%$ was measured. The QE is very reproducible over different samples and processing runs. Table 5.3 gives an overview of different steps of the optimized fabrication process. The measurement results of detectors fabricated following this processing schema were presented in paragraph 5.4.

Figure 5.41 shows the I/V characteristics of detectors fabricated using this optimized processing schema for different levels of illumination. The optical power increases in steps of 10dB. These detectors are identical but were fabricated during different processing runs. The contact spacing is 3μm and the length is 40μm. As can be seen, the flatband voltage is not reproducible and in some cases very high ($>$6V). This means that for these detectors, a large bias voltage needs to be applied in order to obtain maximum quantum efficiency. This large bias voltage is disadvantageous in terms of power dissipation and compatibility with receiver IC's. From a theoretical point of view, the flatband voltage corresponds to the voltage for which all of the active region is depleted and the electric field everywhere



(a)



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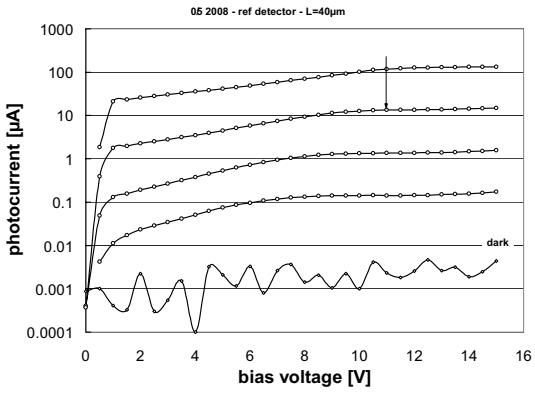

(c)

Figure 5.41: I/V characteristics for detectors fabricated during different processing runs to demonstrate bad reproducibility of flatband voltage

	What	How	Details
I	bonding + substrate removal	manual bonding and selective wet etching	HCl
II	etch-stop layer removal	InGaAs over InP, selective wet etching	$H_2SO_4/H_2O_2/H_2O$
III	sacrificial layer removal	InP over InAlAs, selective wet etching	$HCL/H_3PO_4/CH_3COOH$ (1:1:2) for 30s
IV	mesa etching	unselective wet etching of InAlAs/InGaAs	$H_3PO_4/H_2O_2/H_2O$ (1:1:20) for 54s
V	insulation + contact window opening	BCB and PE	O_2 and CF_4
VI	InAlAs surface preparation (oxide removal)	wet chemistry	NH_4OH/H_2O (1:10) for 20s
VII	metallization	thermal evaporation	Ti(20nm)/Au(200nm)

Table 5.3: Overview of the optimized MSM detector processing

has the same direction. At this voltage, the energy band at the forward biased Schottky contact becomes flat [5, 24]. The flatband voltage of a 1-D MSM photodetector is derived in [5]:

$$V_{FB} = \frac{qN_D L^2}{2\epsilon_S} \tag{5.15}$$

where N_D is the background doping concentration, L is the Schottky contact spacing and ϵ_S is the semiconductor permittivity. The doping concentration in our wafers is unknown but a typical background doping of $10^{15} cm^{-1}$ and a contact spacing of 3μm results in $V_{FB} = 6.3V$ according to this model as can be seen in figure 5.42.

We fabricated detectors on smaller SOI waveguides with smaller contact spacing (down to 1μm) to investigate the influence of the contact spacing on the flatband voltage but we did not notice a significant effect. We believe this is due to the bad reproducibility of the flatband voltage over different processing runs. This model however is for the simplified 1-D case. It is experimentally shown that other effects such as layer structure and more in particular the presence of a graded supperlattice and the thickness of the SBEL layer play an important role [17, 18].

The cause of this reproducibility problem is not fully understood. Different detectors on the same sample show similar flatband voltages, but this is not the case for identical detectors on different samples (= different processing runs). Possible explanations for this behavior are the following:

- The surface quality of the InAlAs SBEL layer can be influenced by the plasma etching process of the contact windows. As the exact

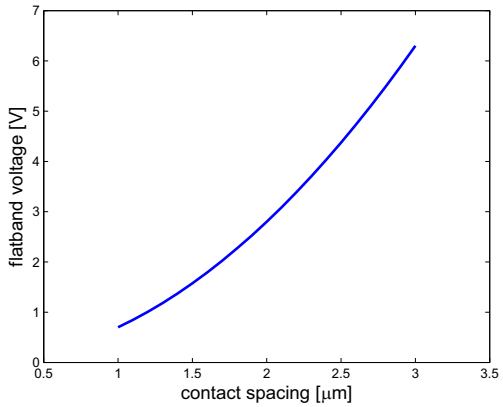

Figure 5.42: Flatband voltage as a function of Schottky contact spacing. The background doping is $10^{15}cm^{-1}$. Calculations are based on a simplified 1-D model [5]

BCB insulation layer thickness varies over different samples, the required etch time to open the contact window also varies. As a consequence, the amount of "over-etching" is different for each run.

- The die-to-wafer bonding is done manually. This means that the BCB bonding layer thickness is not well controllable and reproducible. If the bonding layer thickness is sub-100nm, 90% of the incident light will be absorbed in the first 5μm. As a consequence, the material quality and the alignment of the different layers at the detector front-edge become very critical parameters. Misalignment of the Schottky contacts or the contact window in this case can result in a very small electric field in the front-edge region where the absorption takes places resulting in a larger than expected flatband voltage.

This is shown in figure 5.43. In this case, the Schottky contacts are aligned too much towards the rear-edge of the detector resulting in a very low electric field in the front-edge region where most of the photons are absorbed. A high bias voltage will be necessary to fully deplete this region. This situation also occurs when the Schottky contacts are aligned on target (edge of the contacts coincides with the edge of the mesa) but when the contact window is too small or misaligned towards to rear-edge.

For different processing runs, both the BCB bonding layer thickness and the the exact alignment between the mesa, the contact window and the Schottky contacts varies. As we believe these parameters strongly influence the flatband voltage, this could be the cause of the bad reproducibility. To

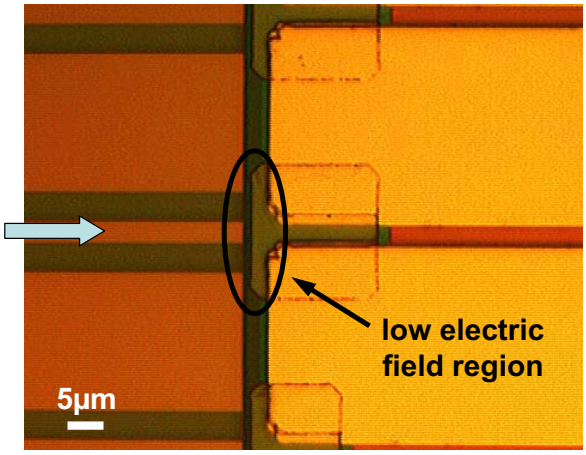

Figure 5.43: Top view picture of a photodetector. The contacts are aligned too much towards the rear-edge resulting in a low electric field in the front-edge region

make the detector performance less sensitive to the quality of the detector edge, the BCB bonding layer thickness can be increased in order to avoid strong absorption in the front-edge detector region. This was explained in chapter 5.2.2.

It is important to notice that this are assumptions and more experiments need to carried out to fully understand and solve this issue. We can conclude that due to the process optimization we obtained a high performance and compact detector with a low dark current, a high quantum efficiency and a linear current-power behavior over a wide dynamic range. The bad reproducibility of the flatband voltage remains an issue, but we pointed out possible problems and solutions.

5.6 Conclusions

In this chapter, we discussed the design, fabrication and characterization of an InGaAs MSM photodetector integrated on nanophotonic SOI waveguides. The integration technology is based on BCB die-to-wafer bonding. We demonstrated very compact detectors, with a high quantum efficiency and low dark current. Detectors with a length of 20μm have a responsivity of 1A/W at a wavelength of 1.55μm, a dark current of 5nA and a linear power-current behavior over a 40dB range. By tuning the length of the detector and/or the bonding layer thickness, the efficiency can be tuned for

power monitor applications. More results on the integration of these detectors with wavelength filters for WDM and spectrometer applications will be given in chapter 6.

We theoretically studied the high speed response and concluded that optical bandwidths above 30GHz can be reached for detectors with a contact spacing of 1μm. These contact spacings can be easily obtained using standard contact lithography. Very high speed operation (>50GHz) could be obtained by applying sub-nm spaced transverse fingers using e-beam lithography. First high-speed measurements have been carried out on prototypes. We showed eye diagrams up to 10Gbps and demonstrated electrical bandwidths up to 4.5GHz for detectors with 2μm contact spacing. This value is significantly lower as compared to the simulated bandwidth and more experiments need to be carried out to understand the cause. Also, in depth-characterization of the dependency of the detector bandwidth on bias voltage, optical power and contact spacing still needs to be done, together with detector passivation and in-depth reliability studies.

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6

Active/passive integrated devices

We designed and fabricated different SOI PICs with on-chip photodetectors. In this chapter, we give an overview of these devices. We discuss on-chip power monitors, resonant photodetectors, CWDM receivers, demultiplexers with flat-top shaped passbands and near-IR spectrometers. Finally, we demonstrate a packaged SOI spectrometer-on-a-chip. The chip is mounted on a printed circuit board, together with a transimpedance amplifier, analog switches and an I/O port. This board can be connected to a parallel PC port for automated read-out of the signals of the 30 on-chip photodetectors.

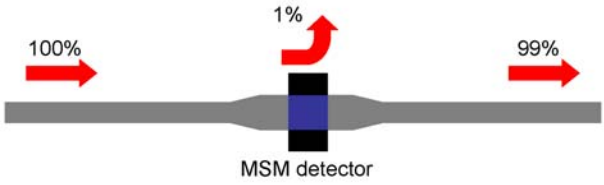


Figure 6.1: On-chip SOI power monitor using an InGaAs MSM detector to tap off a small part of the waveguide power

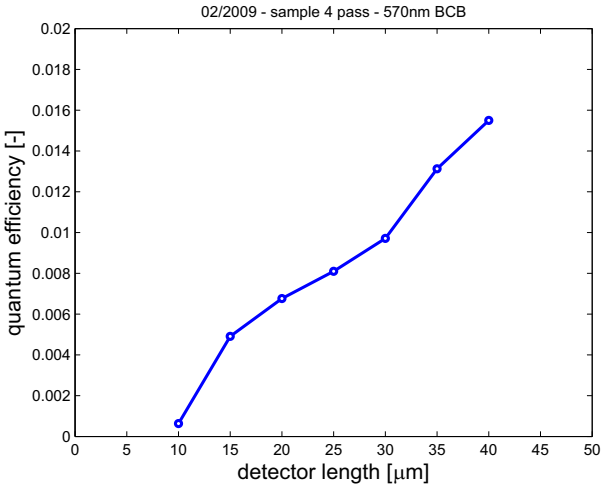


Figure 6.2: Measured quantum efficiency versus detector length. The BCB bonding layer thickness is 570nm

6.1 Power monitor

To measure the signal intensity at different locations on the SOI chip, power monitors can be integrated. These are typically detectors which tap off a small part of the waveguide power (figure 6.1). In chapter 5, we showed that by varying the length or the bonding layer thickness of an evanescently coupled InGaAs MSM detector, the detector efficiency can be controlled. This means that by integrating a short MSM detector with a relatively thick intermediate bonding on a straight SOI waveguide, we are able to monitor the waveguide power without the need for dedicated SOI splitters.

We processed different detectors with lengths ranging from 10 to 40μm on 3μm wide SOI waveguides. Figure 6.2 shows the measured quantum efficiency (QE) as a function of detector length at a wavelength of 1.55μm.

Figure 6.3: On-chip interconnect based on a single WDM link

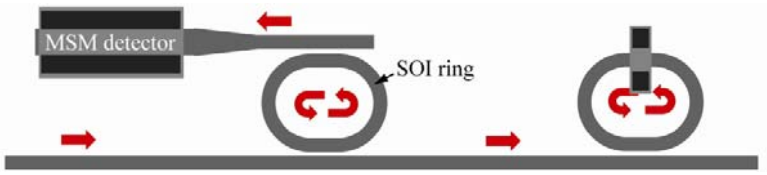
After processing, we measured a bonding layer thickness of 570nm by making a cross section. As can be seen, the QE varies almost linearly from 0.1% for a 10μm long detector to 1.6% for a 40μm long detector. This is in line with what we expect from simulations. We did not measure the power at the output of the waveguides but it can easily be estimated. The maximum measured QE of long MSM detectors with thin bonding layers is around 80%. This means that $1/4$ $(20/80)$ of the detected power is lost (mainly due metal absorption). This allows us to make an estimation of the throughput power because the relationship of both optical loss and optical absorption in the InGaAs layer in respect to the detector length is the same.

In order to fabricate power monitors with a reproducible efficiency, the bonding layer thickness should be well controlled. We bonded our samples manually but this does not allow for a strict control on the bonding layer thickness. A (semi-)automated setup using a die-to-wafer bonder could solve this issue.

6.2 Resonant photodetector

In future on-chip optical interconnects, wavelength division multiplexing (WDM) is an inevitable technology in order to fully exploit the bandwidth of an SOI waveguide. This can be done by using a multi-wavelength laser based on cascaded microdisk lasers [1, 2] at the transmitter side and an array of wavelength selective photodetectors at the receiver side (see figure 6.3).

Wavelength selective photodetection can be achieved by integrating a photodetector on the drop port of a ring resonator. This way, the wavelength of interest will be dropped from the bus waveguide and can be detected as shown in figure 6.4. A novel approach, also shown on the same figure and proposed by coworker Dr. L. Liu results in a much more compact device [3]. In this case, we bonded a short MSM detector on top of a part of the SOI ring. This way, no drop port is needed and due to the resonance, the detector can be made much shorter.



Conventional design broadband detector + ring resonator

Compact design absorbing mesa on ring(this work)

Figure 6.4: Conventional configuration and resonant detector configuration for wavelength selective detection

If the absorption loss induced by the InGaAs layer is equal to the coupling loss to the bus waveguide (assuming the intrinsic loss of the SOI ring cavity itself is negligible), all the light at the resonant wavelength will be dropped. Usually, these coupling and absorption losses are in the range of several percentages to tens of percentages depending on the required bandwidth. Therefore, the length of the detector can be strongly reduced and/or the thickness of the BCB bonding layer can be increased as compared to a standard high efficiency detector [3].

Figure 6.5 is a top view picture of the fabricated device, before and after metallization. The SOI ring resonator has a racetrack shape with a bending radius of 5μm and a straight section length of 7μm. The detector has a length of 5μm and is defined on top of a straight section of the ring. After bonding and mesa etching, we spun an insulation layer of BCB on the whole chip to ensure enough separation between the SOI structure and the metal wires. Then, we etched a contact window and deposited two coplanar Schottky contacts with a spacing of 3μm.

Figure 6.6 plots the detected photocurrent and the SOI waveguide power for different wavelengths. As can be seen, the power in the SOI waveguide has a Gaussian spectrum due to the fiber coupler used for interfacing with the optical fiber. One can see that the responsivity at the resonant wavelengths is $\sim$1.0A/W. This is as large as the responsivity of a conventional detector but due to the resonant behavior, it can be achieved for a detector length of only 5μm and a bonding layer thickness of 250nm. Off resonance, the detected current drops by more than 10dB (optical). The free spectral range is $\sim$12nm and the 3dB bandwidth is $\sim$2nm. A sharper resonance is possible by adjusting the coupling strength to both the bus waveguide and the photodetector.

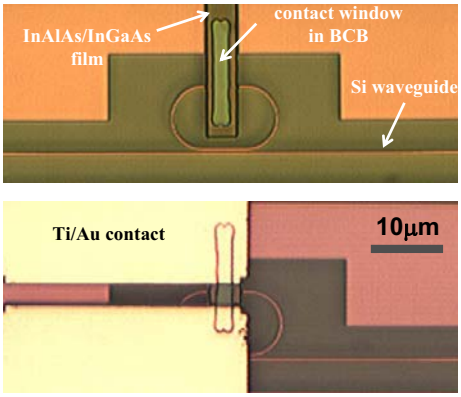


Figure 6.5: Top view of resonant photodetector before (top) and after (bottom) metallization

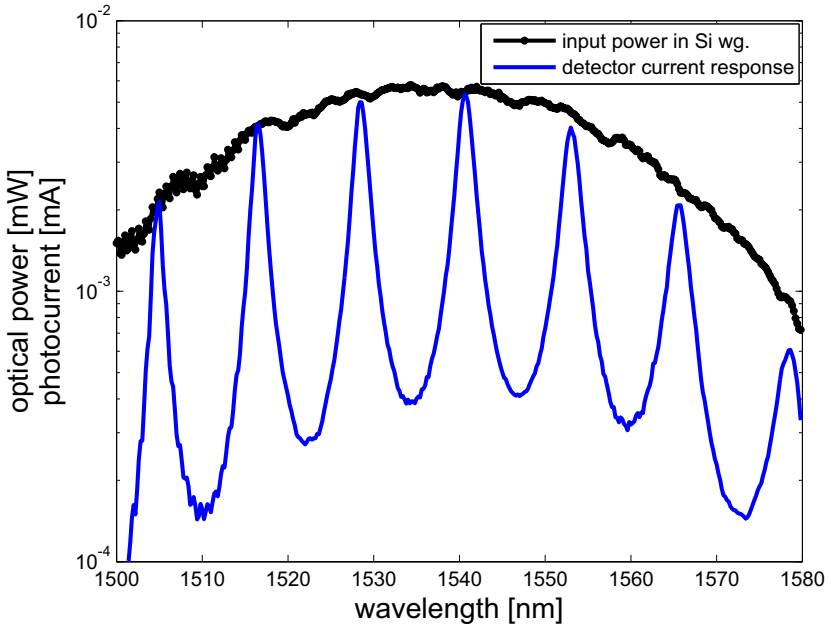


Figure 6.6: Optical SOI waveguide power and generated photocurrent

6.3 Echelle gratings

In this section, we give an overview of different PCG demultiplexers equipped with on-chip photodetectors and we also focus on possible applications. The design of these PCGs was described in chapter 3. In this chapter, we show measurement results of a CWDM receiver [4, 5], a PCG with integrated detectors, which is a building block for FTTH transceivers and a 30-channel near-infrared spectrometer for sensing applications [6, 7].

6.3.1 CWDM receiver

Coarse wavelength division multiplexing (CWDM) systems have a channel spacing of typically 20nm on the ITU wavelength grid and are designed for use with uncooled transmitter lasers. CWDM makes it possible to increase the capacity of a fiber optic link without installing expensive dense WDM (DWDM) systems. Currently, the majority of CWDM transceivers are based on thin film filter (TFF) technology. The main drawback to TFFs lies in the assembly costs of the discrete components and the difficulty of integration with lasers and detectors. Highly integrated modules are a key part of the solution to mass produce these CWDM transceivers in a cost-effective way while reducing size and increasing reliability. Both silica-based CWDM receivers and large-core silicon-on-insulator (SOI) transceivers with hybridized detectors and lasers have been proposed [8, 9]. However, the integration density of these transceivers remains limited due to first of all, the large waveguide bend radius in these material systems and secondly, the large waveguide pitch needed for the hybridization of preprocessed lasers and detectors.

Here, we demonstrate a compact CWDM demultiplexer consisting of a 4-channel PCG fabricated on a nanophotonic SOI platform and heterogeneously integrated MSM detectors. This device can be used either as an integrated CWDM power monitor or receiver. A top view picture of the fabricated device is shown in figure 6.7. The photodetectors are fabricated on a 25μm pitch and the total footprint of the demultiplexer, including photodetectors is only 0.1mm^2.

The measured spectral response of the receiver (TE-polarization) is shown in figure 6.8. The transmission spectrum of the fiber coupler is shown on the right axis. The minimum fiber to waveguide coupling loss was estimated to be 6dB at a wavelength of 1585nm. The optical crosstalk is -25dB and no significant deterioration of PCG characteristics were observed after detector integration. The presence of a BCB bonding layer (n=1.54) slightly decreases the refractive index contrast of the DBR grating

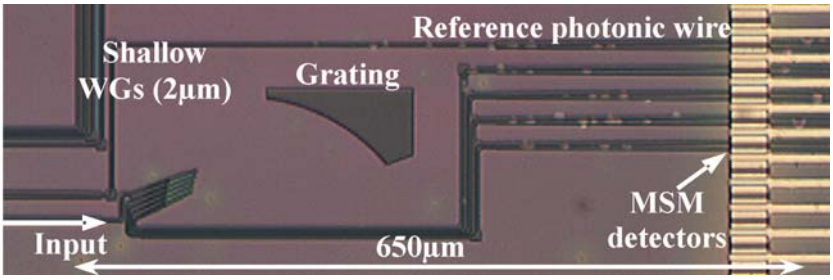


Figure 6.7: Top view picture of the CWDM receiver

facets resulting in a minor increase of grating reflection loss by 0.2dB on average in the 1.5μm-1.6μm wavelength range. The channel non-uniformity is mainly caused by the transmission spectrum of the fiber coupler as can be seen in figure 6.8. The detector efficiency is almost constant in the considered wavelength range.

The power budget can be calculated as follows. By fine-tuning the period of the fiber coupler, it is possible to make the central PCG wavelength and the maximum fiber coupler transmission coincide at λ=1.55μm. In this case, the total loss for the central channels is about 6dB (fiber coupler loss) + 2dB (on-chip PCG loss). Taking into account a detector responsivity of 1A/W at 1.55μm, the total responsivity for the central channels is $\sim$0.15A/W. However, as the main loss contribution is due to fiber coupling loss, the total responsivity of the receiver could be considerably increased (up to 0.6A/W) by using a more efficient fiber to waveguide coupling approach [10, 11].

6.3.2 PCG for FTTH transceivers

In chapter 3, we discussed a passive FTTH transceiver consisting of a grating duplexer to spatially separate the upstream and downstream channels and a PCG to demultiplex the two downstream channels. Typically, a service provider delivers an analog RF modulated video signal through a channel that is transmitted at a wavelength around 1550nm and digital data is sent to the end user through a channel at 1490nm. For the transceiver at the end user side, photodetectors need to be integrated on the two output waveguides of the PCG [12].

To relax tolerances by allowing some wavelength shift of the two lasers at the central office side and the PCG channels at the end user side, it is advantageous to broaden the passband of the downstream channels. A possible approach to achieve this without a loss penalty is by increasing the

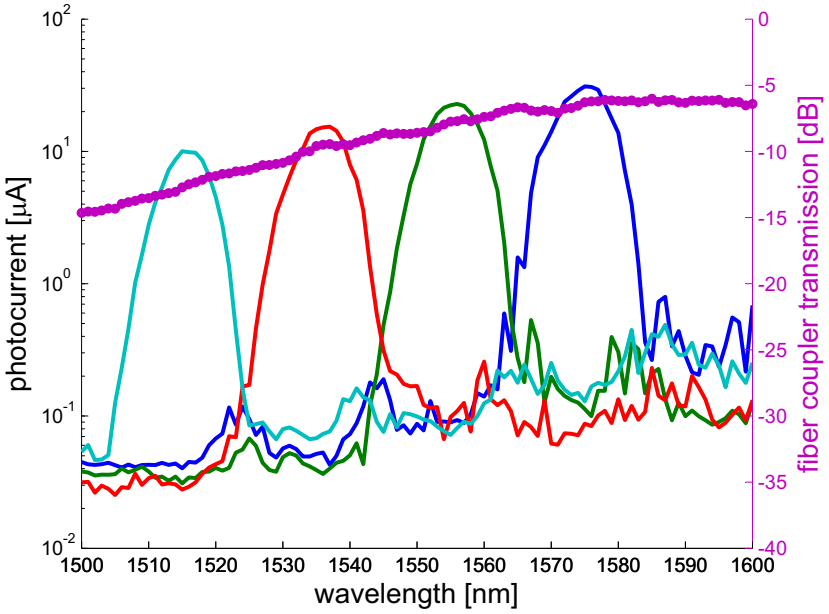


Figure 6.8: Photocurrent spectrum of the CWDM receiver for TE-polarized light on the left axis and transmission of a fiber coupler on the right axis

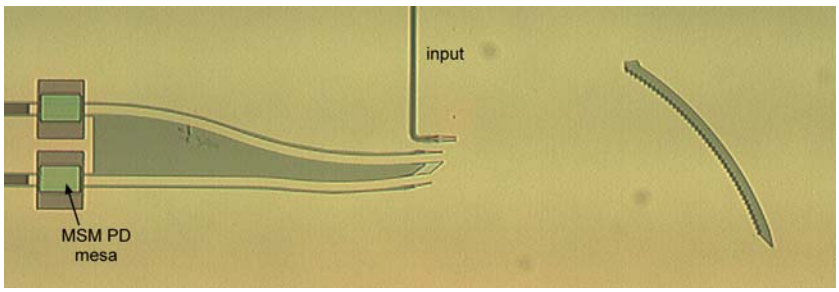


Figure 6.9: Top view of a FTTH demultiplexer with flat-top shaped passbands before detector metallization

width of the output waveguides. This is shown in figure 6.9. The PCG has one 2μm wide input waveguide and two 10μm wide output waveguides. Two MSM detectors are integrated on top of the output waveguides. As can be seen, this picture is taken before metallization.

The input field will be imaged along the Rowland circle and will not only couple to the fundamental mode, but also to higher order modes of the broad output waveguides. For a certain distance along the Rowland circle, corresponding to a certain wavelength range, the light will couple into one of the output waveguides with a constant efficiency ($\sim 100\%$) resulting in a flat-top channel response. Contrary to previous discussed devices, these output waveguides are not tapered to single mode photonic wires and as a consequence, the higher order modes, which flatten the channel passband will also be detected by an integrated MSM detector. The bandwidth itself is determined by the width ratio between the in- and output waveguides. The broader the output waveguides, the broader the channel passband.

Figure 6.10 shows the measured photocurrent spectrum of the 1550nm channel of a first prototype device. The detector of the 1490nm channel failed. A 30nm wide flat-top passband is clearly visible and we can expect an optical crosstalk around -25dB between both channels. The non-uniformity of the photocurrent within the passband is caused by the transmission of the input fiber coupler, which has a maximum fiber-to-chip coupling efficiency around 1585nm. This proof of principle device clearly demonstrates the possibility for obtaining flat-top shape channel responses that could be employed for CWDM and FTTH receiver applications. However, more work needs to be done to optimize this component. As one channel failed, we could not measure the exact channel isolation and also, we did not measure the photodetector efficiency for this device. Due to the large Schottky contact spacing, we noticed a dramatic increase in flat band voltage ($>$10V). To solve this issue, we did some first successful experi-

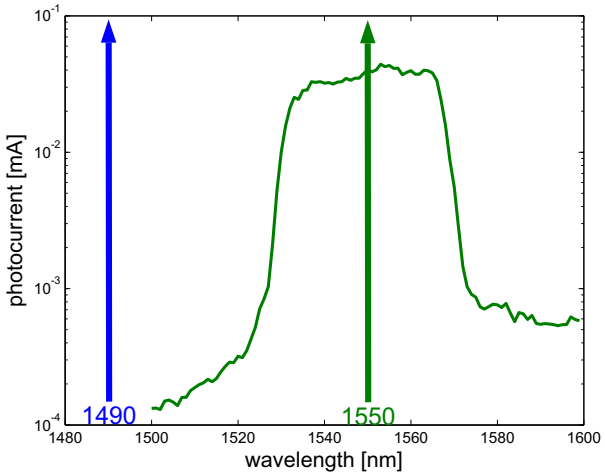
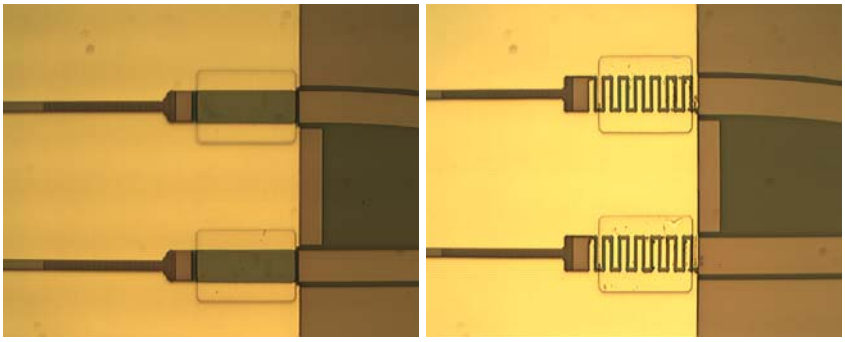


Figure 6.10: Photocurrent spectrum of the 1550nm downstream channel of the FTTH receiver



(a) Standard Schottky contact layout (b) Transversal finger configuration

Figure 6.11: MSM detectors on 10μm wide waveguides

ments with MSM detectors having a transversal finger structure. Both type of detectors are shown in figure 6.11. First measurements showed a lower flatband voltage and no major decrease of the quantum efficiency but more experiments need to be carried out to confirm this.

6.3.3 30-channel near-IR spectrometer

Near-infrared spectroscopy is a technique, which is widely used for highly sensitive measurements of the composition of unknown organic samples

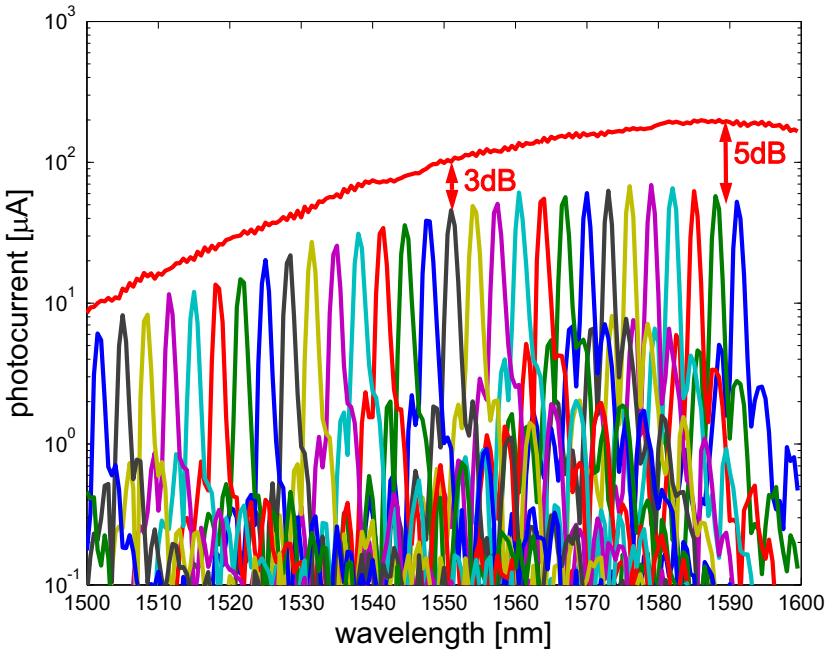


Figure 6.12: Photocurrent spectrum of the 30-channel spectrometer and reference photodetector (red line) for TE polarized light. For the first channel (at λ=1499nm), only the side lobes are visible

by exciting overtones and combinations of molecular vibrations. Typical applications include pharmaceutical, agricultural and biological analysis. Conventional photospectrometers in the labs are typically large and expensive and have a performance that often exceeds the requirements for typical industrial applications. For industrial applications, what counts are the cost, size, robustness, sample volume, measurement time, ... of the spectrometer. For these applications, miniaturized spectrometers [13] that can be mass fabricated are better suited and using these devices, a new range of applications such as real-time, mobile sensing becomes possible. For this purpose, we integrated an array of 30 photodetectors on the 30×3.2nm PCG we discussed in chapter 3. In contrast to existing microspectrometers, this device has no moving parts and can be fabricated on low-cost SOI substrates using wafer scale processing technology.

Figure 6.12 shows the photocurrent spectrum of both the spectrometer and a detector which is processed on top of a reference waveguide. As the quantum efficiency of the detectors is almost constant in the wavelength range from 1.5 to 1.6μm, the spectrum of the reference detector is mainly

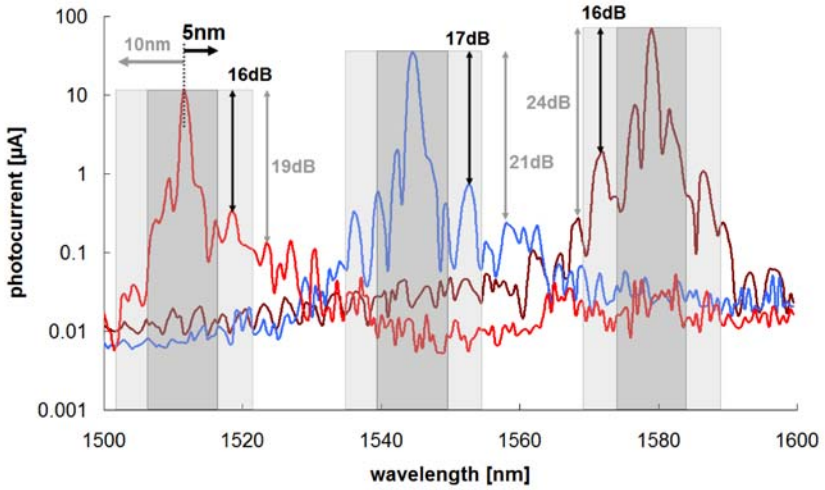


Figure 6.13: Photocurrent spectrum and optical extinction ratio (both short and longer range) of channel 5, 15 and 26

determined by the fiber coupler transmission. The on-chip loss (in respect to the reference detector) of the PCG ranges from 3dB for the central channels to 5dB for the longest wavelength channel. This corresponds with the measurement results of this PCG as discussed in chapter 3. The power budget of the spectrometer can be calculated in a similar way as for the CWDM receiver. By fine-tuning the fiber coupler, the central PCG wavelength and the maximum fiber coupler transmission will coincide at 1.55μm. The total loss for the central channels in this case is 6dB (fiber coupler loss) + 3dB (on-chip PCG loss). Waveguide loss can be neglected. Taking into account a detector responsivity of 1A/W at 1.55μm, the total responsivity for the central channels is $\sim$0.1A/W. The size of the spectrometer including photodetectors, but excluding electrical probe pads is $\sim$2mm^2.

The near-channel optical crosstalk varies between -10dB and -18dB. This is $\sim$5dB worse as compared to the pure passive device as presented in chapter 3. We believe this might be caused by thickness non-uniformities of the thin BCB bonding and insulation layer ($\sim$200-300nm) on top of the slab region of the PCG. Spinning a thicker BCB insulation layer should solve this issue. For spectrometer applications, the longer range extinction is as important as near-channel crosstalk. To assess the long range extinction ratio between the different spectrometer channels, we plotted the photocurrent of three (arbitrary) channels in figure 6.13. As can be seen, the side lobes rapidly decreases further away from the channel peak to saturate at

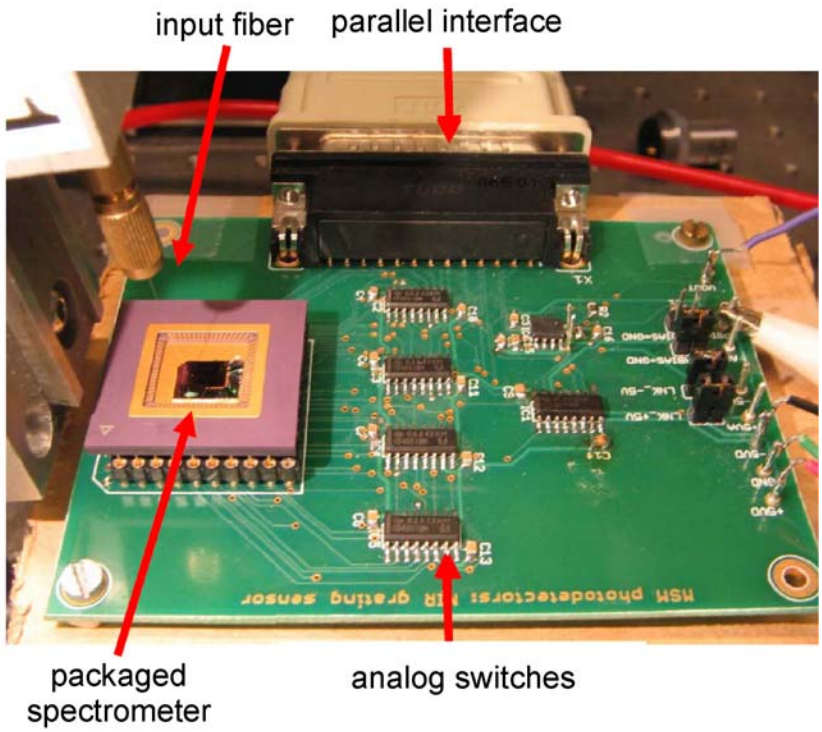


Figure 6.14: Spectrometer-on-a-chip mounted on a read-out board. Both the optical and electrical interfaces are visible

a value of about 10nA which is only slightly higher as the detector dark current. The extinction ratio outside a 5nm range of each channel is better than 15dB, and >20dB outside a 10nm range.

In the framework of a master thesis [14], this spectrometer chip was mounted and wire-bonded into a ceramic PGA (Pin Grid Array) package as can be seen in figure 6.14. This PGA was mounted on a read-out printed circuit board (PCB) which contains some analog switches, a transimpedance amplifier (TIA) and a parallel PC interface. The optical input fiber can be seen on the left side of the picture. A Labview program was used to sequentially read-out the signals of the 30 on-chip photodetectors.

6.4 Conclusion

In this chapter, we demonstrated SOI PICs with integrated photodetectors for different applications: power monitors and WDM receivers for on-chip interconnects, CWDM and FTTH receivers for telecom applications and a 30-channel near-infrared spectrometer-on-a-chip.

The spectrometer presented in this chapter has a record small footprint of only $\sim$2mm^2. This device clearly demonstrates the advantages of the heterogeneous integration approach presented in this work: efficient InGaAs photodetectors can be integrated on very compact passive SOI PICs. By making use of a die-to-wafer bonding approach, these detectors can be processed on wafer scale and are lithographically aligned to the underlying SOI waveguides. The 30 photodetectors were simultaneously processed on a pitch of only 25μm and showed uniform characteristics without a single failure.

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7

Conclusion and outlook

7.1 Conclusion

The objective of this work was to fabricate silicon PICs for WDM and near-infrared spectroscopy applications. These devices were fabricated by means of heterogeneous integration of InGaAs photodetectors onto passive silicon PICs. This integration technique, which allows to define the detectors on an SOI wafer scale in combination with the fabrication of the passive circuitry on low-cost SOI wafers using CMOS compatible processes can result in compact, highly integrated, low-cost and reliable miniature photospectrometers that can be mass-fabricated.

In a first part of this work, we investigated the heart of each spectrometer: the wavelength filter. For the first time, we fabricated a waveguide echelle grating (PCG) on a nanophotonic SOI platform. We showed that this material systems offers many advantages for the fabrication of PCGs as compared to other low- to medium index contrast material systems: strict fabrication tolerances on facet verticality are strongly relaxed, the footprint can be drastically reduced and there is no propagation of higher order slab modes which possibly deteriorate the performance. We demonstrated a prototype CWDM (de-)multiplexer with four 20nm spaced wavelength channels in the telecom window around 1.55μm. We obtained very high channels extinction ratios better than 30dB and by replacing each facet with a DBR-type reflector, we obtained a very low on-chip loss of 1.9dB. This technique showed to be very efficient for increasing the grating reflectivity without the need for metal coating.

For near-infrared spectroscopy applications, we demonstrated a 30 channel spectrometer with a $\sim$3nm resolution and an operational wavelength range of 100nm. We noticed that filters with a high resolution seem to be more sensitive to crosstalk as compared to device for coarse wavelength filtering. We identified slab thickness non-uniformity as being a major source of crosstalk. Although the performance of these PCGs is expected to rapidly improve with advances in fabrication technology, we believe that cascaded filters are the key to success for the realization of high resolution spectrometers that operate over a broad wavelength range. We reported on initial results of cascaded filters based on a combination of ring resonators and a PCG. In this case, the PCG is used for relatively coarse filtering over a broad wavelength range and high-Q ring resonators are used to filter a narrow peak out of each PCG channel. Spectrometers as presented in this work could possibly find application in low cost, on-chip biological and chemical sensors (e.g. biodiesel and glucose sensing), optical coherence tomography, ...

In a second part of this work, we focused on the integration of near-

infrared on-chip photodetectors. We discussed the two most promising approaches which exist today to fabricate these detectors on a SOI wafer scale: epitaxial grown Ge-on-SOI detectors and heterogeneously integrated InGaAs-on-SOI detectors by means of die-to-wafer bonding. We studied adhesive die-to-wafer bonding in more detail and we described the optimized integration process based on manual bonding of III-V dies on SOI using a sub-300nm intermediate BCB bonding layer. We demonstrated a high bonding yield and multiple die-to-wafer bonding. The integration approach based on die-to-wafer bonding offers important advantages as compared to hybrid integration techniques in which preprocessed InGaAs detectors are flip-chipped onto the SOI waveguide wafer. As the III-V dies are unpatterned before bonding, no strict, and therefore time consuming alignment accuracy is needed, resulting in a more cost efficient process. Moreover, the detectors can be fabricated on an SOI wafer scale and lithographically aligned to the underlying waveguides and by making use of evanescent coupling, a low coupling loss from waveguide to detector can be achieved.

After discussing the InGaAs-on-SOI integration technology based on adhesive die-to-wafer bonding, we elaborated on the design and fabrication of highly efficient InGaAs MSM detectors coupled to SOI waveguides. We demonstrated very compact detectors with a length of only 20μm, a responsivity of 1A/W at a wavelength of 1.55μm and a dark current of 5nA. Arrays of up to 100 detectors were fabricated on a 25μm pitch without a single failure. Simulation results showed that using standard contact lithography, electrical bandwidths up to 30GHz can be obtained. First high speed measurements on fabricated prototypes revealed optical bandwidths up to 9.5GHz.

Finally, we demonstrated our technology by fabricating different SOI PICs with on-chip detectors for (mainly) spectroscopic applications: power monitors and WDM receivers for on-chip interconnects, CWDM and FTTH receivers for optical communication applications and a 30-channel near-infrared spectrometer-on-a-chip.

7.2 Outlook

The SOI PICs presented in this work are currently at a point in their evolution where they have proven their potential but different issues remain to be solved before they can be deployed in the field.

Whereas the performance of single PCGs will eventually be sufficient for coarse wavelength filtering applications (e.g. CWDM, FTTH), cascading these devices with other filters might be needed for high resolution

spectrometers that operate over a broad wavelength range. We believe this is a very promising research topic that would allow to increase performance, thereby by fully exploiting one of the assets of silicon photonics: many devices can be integrated on a single chip. Other issues that must be solved and that are closely related to the nanophotonic SOI platform are temperature dependency, polarization dependency, broadband fiber-to-chip coupling and the influence of fabrication variations (e.g. Si slab thickness) on the wavelength.

Adhesive die-to-wafer bonding using BCB as described in this work is still a manual process which is well suited for research purposes and prototype manufacturing. However, in order to obtain a mature fabrication process that is suitable for commercial applications, an automated die-to-wafer bonding approach is needed. Only this way, SOI wafers can be populated with multiple III-V dies using a high yield bonding process with a reproducible BCB layer thickness. We demonstrated processing of bonded III-V devices on a small sample scale, but additional developments are needed in order to translate this into a high yield wafer scale processing of active III-V devices on 8 inch SOI wafers.

We demonstrated the integration of high performance InGaAs detectors on an SOI platform. However research- and even commercial interest has been oriented more towards Ge-on-SOI detectors in the last couple of years. During this period, a huge progress has been made in this field and SOI PICs with integrated Ge detectors have even become commercially available. The reason for this is mainly technology-related. Even if InGaAs would be the preferable detector material due to its direct bandgap structure and optimal energy gap for wavelengths used for telecommunications, the integration in Si technology has been shown to be more complicated. However, as mentioned before, we believe that InGaAs-on-SOI detectors can be an attractive alternative to Ge-on-SOI detectors for future applications. For the fabrication of on-chip lasers, integration of III-V material is the only viable solution at the moment and detectors and sources could be fabricated in the same processing steps, using the same wafer scale III-V technologies. Also, for prototyping and research purposes, smaller investments are needed for die-to-wafer bonding as compared to the expensive equipment needed for heteroepitaxial growth. Third, for spectroscopy applications in the 1.65-1.7μm wavelength range (e.g. glucose sensing), the absorption of Ge is too low for efficient photodetection whereas efficient detection is still possible using InGaAs. Last and maybe most important, the heterogeneous integration based on very thin BCB die-to-wafer bonding is very generic. By bonding other semiconductors materials for example such as InGaAs quantum dots or InAsSb, the bandgap can be further reduced and

long wavelength detection becomes possible.

A Publications

A.1 International journals

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List of Figures

List of Tables

List of Acronyms

A

AWG	Arrayed Waveguide Grating

B

BCB	BenzoCycloButene
BEM	Boundary Element Method

C

CAMFR	CAvity Modelling FRamework
CATV	Cable Television
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CWDM	Coarse Wavelength Division Multiplexing

D

DBR	Distributed Bragg reflector
DC	Directional Coupler
DFB	Distributed Feedback

DI	Deionized
DUV	Deep-ultraviolet
DWDM	Dense Wavelength Division Multiplexing

E

EDFA	Erbium Doped Fiber Amplifier
ELO	Epitaxial Lateral Overgrowth

F

FBG	Fiber Bragg Grating
FDTD	Finite Difference Time Domain
FIB	Focused Ion Beam
FPR	Free Propagation Region
FSR	Free Spectral Range
FTTH	Fiber To The Home

H

HEMT	High Electron Mobility Transistor

I

IC	Integrated Circuit
IPA	Isopropyl Alcohol
ITU	International Telecommunication Union

L

LED	Light Emitting Diode
LD	Linear Dispersion

M

MEMS	Micro Electro-Mechanical Systems
MMI	MultiMode Interference coupler
MoM	Method of Moment
MZI	Mach Zehnder Interferometer

O

OSA	Optical Spectrum Analyzer

P

PCG	Planar Concave Grating
PD	Photodetector
PDL	Polarization Dependent Loss
PE	Plasma Etching
PGA	Pin Grid Array
PIC	Photonic Integrated Circuit

Q

QE	Quantum Efficiency

R

RCWA	Rigorous Coupled Wave Analysis
RF	Radio Frequency
RIE	Reactive Ion Etching
RR	Ring Resonator

S

SC	Standard Clean
SEM	Scanning Electron Microscope
SNR	Signal To Noise Ratio
SOG	Spin-on Glass
SOI	Silicon-on-Insulator

T

TE	Transverse Electric
TFF	Thin Film Filter
TIA	Transimpedance Amplifier
TIR	Total Internal Reflection
TM	Transverse Magnetic

U

UV	Ultraviolet

W

WDM	Wavelength Division Multiplexing
WG	Waveguide