Graphene-Silicon Photonic Integrated Circuits: Design, Technology and Devices

Hybridisatie van geïntegreerde fotonische circuits op basis van silicium met grafeen: ontwerp, technologie en componenten

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Leila

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List of Acronyms

A

ALD   Atomic layer deposition
AFM   Atomic Force Microscopy

B

BOE   Buffered Oxide Etch
BR   Bit Rate

C

CMOS   Complementary Metal-Oxide-Semiconductor
CMP   Chemical Mechanical Planarization
CVD   Chemical Vapour Deposition

D

DLG   Double-Layer Graphene
DI   Deionized
DVS-BCB   Divinylsiloxane-Bis-Benzocyclobutene
DML   Directly modulated laser

E

ER   Extinction Ratio
EAM   Electro-Absorption Modulator

F

FWHM   Full-Width at Half-Maximum
FOM   Figure of Merit
FIB   Focused Ion Beam
FP   Footprint

I

IL   Insertion Loss

L

LN   Lithium Niobate

M

MLL   Mode-locked laser
MPW   Multi-project wafer
MZM   Mach-Zehnder Modulator
ME   Modulation efficiency

N

NRZ   Non-Return-to-Zero

O

OBW   Optical Bandwidth

P

PMMA   Poly methyl methacrylate
PDMS   Polydimethylsiloxane
PhC   Photonic Crystal
PECVD   Plasma-Enhanced Chemical Vapor Deposition
Pol   Polarization

Q

QF   Quality Factor

R

RIE   Reactive-Ion Etching

S

SA	Saturable Absorber
SiN	Silicon Nitride
SOI	Silicon on Insulator
SLG	Single-Layer Graphene
SMSR	Single mode suppression ratio
SEM	Scanning Electron Microscope

T

TE	Transverse-Electric
TM	Transverse-Magnetic
TEM	Transmission Electron Microscope
TLM	Transmission Line measurement

V

V_{pp}	Peak to peak voltage

Nederlandse samenvatting
–Summary in Dutch–

Optische interconnecties hebben hun nut bewezen als een revolutionaire oplossing om aan de noden van snelle en breedbandige datanetwerken met een laag energieverbruik en lage overspraak te voldoen. Deze interconnecties worden momenteel volgens verschillende technologieën ontwikkeld, waaronder InP monolithische integratie. Recentelijk kregen twee-dimensionale (2D-) materialen bijzondere aandacht vanuit de onderzoeksvelden materiaalkunde, fysica, chemie en elektronica omwille van hun uitzonderlijke eigenschappen. Grafeen is een uniek 2D-materiaal dat interessant is als alternatief tot de eerder vermelde technologieën. Grafeen is één atoomlaag dik, heeft een lineaire dispersie en een sterke absorptie in het frequentiedomein gebruikt voor optische communicatie. Golfgeleiders geïntegreerd met grafeen bieden veel fotonische toepassingen waaronder signaaldetectie, modulatie en schakelaars.

Deze thesis beschrijft de verschillende aspecten in de realisatie van grafeen-gebaseerde optische schakelaars. Zowel ontwerp, fabricage als karakterisatie worden in detail toegelicht.

De eerste stap behelsde het ontwerp van grafeen-gebaseerde modulatoren en schakelaars. De vooropgestelde componenten werken capacitief en maken gebruik van silicium- of Si_3N_4-platformen. Het eerste ontwerp integreert een monolaag grafeen op silicon-on-insulater (SOI), waarbij de monolaag getransfereerd wordt op een gedopeerde silicium golfgeleider, ervan gescheiden door een dunne oxidelaag. De gedopeerde golfgeleider fungeert als plaat van de capaciteit voor het device. De tweede structuur bevat een dubbele laag grafeen bovenop een SOI golfgeleider, waarbij de twee lagen grafeen van elkaar gescheiden zijn door een dun diëlektricum. In dit ontwerp is de dopering van het silicium overbodig aangezien de aandrijfspanning wordt aangelegd over de twee grafeenlagen. De derde configuratie maakt gebruik van een dubbele grafeenlaag op een siliciumnitride golfgeleider. Dit ontwerp is gelijkaardig aan het vorige, het enige verschil zijnde dat de golfgeleider nu uit siliciumnitride bestaat. In de laatste configuratie is een dubbele laag grafeen ingebed in een SiN golfgeleider, het diëlektricum is dus vervangen door SiN.

De mechanismen verantwoordelijk voor lichtverliezen en de dynamische prestatie van deze devices werden gesimuleerd. We merkten dat de FOM, zijnde de verhouding van de extinctieratio (ER) tot het insertieverlies, onafhankelijk was van de configuratie maar opmerkelijk beïnvloed werden door de kwaliteit van het grafeen. Een andere belangrijke parameter is de 3 dB-bandbreedte. Volgens onze berekeningen kan een bandbreedte van 16 GHz en een extinctieratio van 5 dB bereikt worden in een korte modulator met een kleine capaciteitsbreedte en een dik gate oxide (bijvoorbeeld in een 20 µm-lange component met een 0.8 µm-brede capaciteit en een 5 nm-dik gate oxide bijvoorbeeld). Een 200 µm-lang device zou echter meer dan 20 dB extinctieratio kunnen bereiken met een schakeltijd van 0.4 ns.

Vervolgens vatten we de fabricage aan: we ontwikkelden stappen voor het verwerken van grafeen door verschillende structuren te construeren voor transmissielijnmetingen. Op deze manier konden we ook de resistiviteit van het grafeen optimaliseren. We merkten dat twee devices degelijk presteerden. Het eerste was een transmissielijnstructuur van grafeenstroken met palladium elektrodes. Het tweede was Al_2O_3-bedekt grafeen gecombineerd met rand-gekoppeld grafeen met een contactsweerstand van 400-900 Ω.µm en een vierkantsweerstand van om en bij 400 $\Omega/\square$.

Verder ontwikkelden we een nieuwe methode om grafeen van micrometergrootte te transfereren. Tot op heden waren zulke methodes gebaseerd op een manueel proces aan de hand van zelfgebouwde instrumenten, waardoor de kwaliteit van het proces sterk afhankelijk is van de kunde van de onderzoeker. Om reproduceerbare grafeenoverdracht mogelijk te maken en de gebruikersafhankelijkheid te verminderen, ontwikkelden we een nieuwe methode om micrometergroot grafeen te transferprinten aan de hand van een geautomatiseerde commerciële transferprinter (X-Celeprint, model µTP 100). Dit proces is gebaseerd op het creëren vij hangende, micrometergrote grafeenpatronen op een Si substraat, beschermd door een fotoresistieve laag (voortaan de coupon genoemd). De coupons werden bereid zodat ze door een PDMS stempel opgepikt konden worden (deze stempel is aan de stempelhouder van de transferprinter gehecht) om ze dan op een specifieke component op het doelsubstraat te printen. Na het printen kon de fotoresist verwijderd worden met aceton. Om de optische absorptie van het geprinte grafeen te karakteriseren, transfereerden we verschillende grafeencoupons op een geplanariseerde siliciumnitride golfgeleider. Het verkregen verlies van 0,054 dB/µm was in lijn met onze simulaties. Bovendien maten we het Raman spectrum voor het getransfereerde grafeen op de SiN golfgeleider. We vonden een 2D-band met een halfwaardebreedte gelijk aan

33 cm^{-1}, een G-band met halfwaardebreedte 15 cm^{-1} en $I_{2D}/I_G = 2,36$. Deze resultaten waren in goede overeenstemming met die van een referentiestaal. Er werd geen D-band geobserveerd (deze is indicatief voor defecten in het monster), wat de performantie van de ontwikkelde transferprintmethode bevestigt.

De volgende stap was de overdrachtsmethode toepassen op een op grafeen-gebaseerde schakelaar, geïntegreerd met voorwaarts- en zijwaartsgekoppelde silicium fotonische kristalcaviteiten. Metalen contacten werden op het grafeen aangebracht en een ionische gellaag werd toegevoegd.

We maten een hoge extinctieratio van 17 dB voor de voorwaartsgekoppelde caviteit en 4,7 dB voor de zijwaartsgekoppelde door een spanning van -1,2 V aan te leggen (**Figuur 1**). De verschuiving van de caviteitsresonantie was 0,7 nm voor beide devices. De transmissie en kwaliteitsfactor namen toe bij negatievere spanning voor beide componenten. Dit resultaat duidt aan dat de grafeenlaag transparanter werd, zoals verwacht.
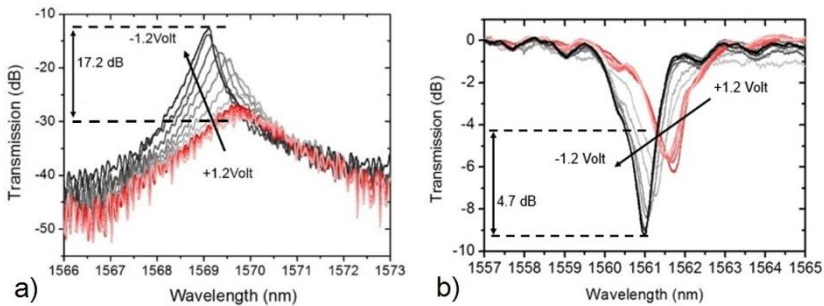
Figuur 1: Het transmissiespectrum van a) een voorwaartsgekoppelde caviteit. b) een zijwaartsgekoppelde caviteit voor verschillende gatespanningen.

Om de mogelijke verbeteringen aan het ontwerp te evalueren werd een model gebaseerd op gekoppelde modetheorie gebruikt. We zagen dat de voorwaarts-gekoppelde caviteit geoptimaliseerd kan worden door de reflectiviteit van de spiegels, en dus Q_c, te verminderen. Voor $Q_c = 3500$ bijvoorbeeld kan een goed resultaat, $ER \sim 10$ dB, verkregen worden met tegelijkertijd een insertieverlies onder 3 dB, rekening houdend met de huidige kwaliteit van de grafeenlaag. Verdere verbeteringen worden verwacht voor kwaliteitsvoller grafeen. De zijwaarts-gekoppelde caviteit toonde weinig variaties met Q_c en verdere verbeteringen vergen optimalisatie van het fabricatieproces.

Tenslotte gingen we over tot het maken en karakteriseren van een schakelaar gebaseerd op een dubbele laag grafeen, geïntegreerd in een SiN golfgeleider. Een dunne laag SiN werd gebruikt als buffer tussen de twee grafeenlagen die rusten op een 300 nm-dikke SiN golfgeleider. Het aanbrengen van de grafeenlaag werd geoptimaliseerd aan de hand van Raman spectroscopie en ellipsometrie. De bovenste SiN laag (300 nm) werd dan afgezet en geëtst om de vorm van de golfgeleider te bekomen. In deze configuratie werden metalen contactoppervlakken bovenop de grafeenlagen aangebracht om het Ferminiveau te manipuleren. Volgens onze simulatie werden er goede prestaties verwacht van deze component, in het experiment werd echter een extinctieratio van slechts 3,5 dB voor een spanning van 10 V gemeten. Een reden kan het gebruik van SiN als diëlektricum zijn aangezien dit een heel hoge lekstroom heeft. Dit zou opgelost kunnen worden door een kwaliteitsvolle Al_2O_3 laag via ALD aan te brengen. Verder zou een volgend ontwerp een structuur kunnen bevatten om de koppeling tussen de 300 nm en 600 nm dikke SiN lagen te verbeteren. Fabricage van zo'n ontwerp zou echter e-beam lithografie vereisen.

English summary

Optical interconnects have shown to be a revolutionary solution to meet the requirements of high-speed and high-bandwidth data networks with low power consumption and low cross talk. These interconnects are currently being developed based on several technologies, such as monolithic integration of III-V materials, silicon-on-insulator, silicon nitride, heterogeneous integration, and GeSi. Recently, two-dimensional (2D) materials with exceptional properties have received considerable attention in theoretical and experimental studies in various research fields, including materials science, physics, chemistry, and electronics. Graphene is a unique 2D material that has attracted interest for use as an alternative to the aforementioned technologies in photonics. Graphene is one atom thick, with a linear dispersion and high absorption in communication bands. Graphene-integrated waveguides enable many photonic applications such as signal detection, modulation and switching. This thesis concerns the development of graphene-based switches including design, fabrication and characterization.

Our first step was to design graphene-based modulators and switches. The suggested devices are capacitor-based devices, on silicon or Si_3N_4 platforms. The first design incorporates single-layer graphene on silicon-on-insulator (SOI), consisting of a single-graphene layer transferred to a doped silicon waveguide, separated by a thin oxide layer. The doped silicon waveguide serves as a plate of the capacitor. The second structure features a double layer of graphene on top of a SOI waveguide, incorporating two layers of graphene, separated by a thin dielectric. In this design, a doped Si waveguide is unnecessary because the driving voltage of the device is applied between the top and bottom graphene layers. The third configuration is double-layer graphene on a silicon nitride waveguide. This design is similar to the double-layer graphene on Si waveguide, except that the waveguide is Si_3N_4. The final configuration is double-layer graphene embedded into a SiN waveguide.

The optical loss mechanism and dynamic performance of these devices were simulated. We observed that the figure of merit (FOM), i.e., the extinction ratio over the insertion loss was independent of the configuration but markedly affected by the graphene quality. Another important parameter in these devices is the 3-dB bandwidth. According to our calculations, a bandwidth of 16 GHz and an ER of 5 dB can be obtained in a short modulator

with a short capacitor plate width and a thick-gate oxide (e.g a 20-µm long device with a 0.8-µm capacitor width and 5-nm gate oxide thickness). A 200-µm long device on the other hand should allow for more than 20 dB ER and switching speed up to 2.5 GHz (0.4 ns).

Next, we proceeded to the fabrication; we developed steps for processing graphene by fabricating various transmission line measurement (TLM) structures. In this way we could also optimize the resistivity of the graphene. We observed that two devices showed decent performance. The first configuration was a TLM of graphene strips with palladium electrodes. The second was Al_2O_3-capped graphene combined with graphene edge contacting with a contact resistance of 400–900 Ω.µm and sheet resistance of approximately 400 $\Omega/\square$.

Furthermore, we developed a new micron-size graphene transfer method. To date, such transfer methods have relied on manual processes with the use of home-built tools, depending on the handling skills of the operator. To allow reproducible graphene transfer and minimize the dependence on handling skill, we developed a new method for micron-size graphene transfer printing using an automated commercial transfer printer (X-Celeprint, model µTP-100). This process is based on the fabrication of suspended micron-size graphene patterns on a Si substrate protected by a photoresist layer (hereafter referred to as a coupon). The coupons were prepared such that they could be picked up by a PDMS stamp (attached to the stamp holder of the transfer printer) and printed onto a specific device on the target substrate. After printing, the photoresist could be removed with acetone. To characterize the optical absorption of the printed graphene, we transferred several graphene coupons onto planarized silicon nitride waveguides. The extracted loss of 0.054 dB/µm was in line with our simulations. Moreover, we measured the Raman spectrum for the transferred graphene on the SiN waveguide. We found a 2D-band with a full width at half maximum (FWHM) of 33 cm^{-1}, a G-band with a FWHM of 15 cm^{-1}, and I_{2D}/I_G = 2.36. These results were in good agreement with those from a reference sample. No D-band (indicative of defects in the graphene) was observed, confirming the effectiveness of the developed transfer printing method.

The next step was to apply the developed transfer method to fabricate a graphene-based switch integrated on front-coupled and on side-coupled Si-based photonic crystal (PhC) cavities. After graphene transfer, metal pads were then fabricated on the graphene, and an ionic gel layer was coated on the sample.

We measured a high extinction ratio of 17 dB from the front-coupled cavity and 4.7 dB from the side-coupled cavity by applying a voltage of −1.2

V (Error! Reference source not found.). The shift of the cavity resonance was 0.7 nm for both devices. The transmission and quality factor increased for both devices as the voltage became more negative. This result indicates that the graphene layer became more transparent, as expected.

To evaluate possible design improvements a model based on coupled mode theory is used. We observed that the front-coupled cavity can be optimized by reducing the strength of the mirror section and thus a lower Q_c E.g. with $Q_c = 3500$, it is possible to obtain a good $ER \sim 10$ dB while reducing the IL below 3dB, taking into account the current quality of the graphene layer. Further improvements are expected for higher quality graphene. The side-coupled cavity showed limited variations with Q_c and further enhancement requires fabrication optimization.
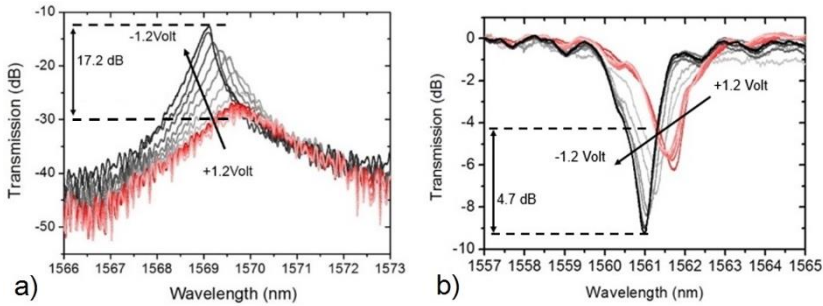
Figure 1: The transmission spectrum of a) Front-coupled cavity. b) Side-coupled cavity for different gate voltages.

Finally, we fabricated and characterized a double-layer graphene-based switch embedded in a SiN waveguide. A thin layer of SiN was used as a spacer between the two graphene layers (transferred by our developed technique) lying on a 300-nm SiN waveguide. The deposition of this layer on graphene was optimized by Raman spectroscopy and ellipsometry. The top SiN layer (300 nm) was then deposited and etched to form the shape of the waveguide. In this configuration, metal pads were fabricated on the graphene layers to control the Fermi level. According to our simulation, good performance was expected from this device; however, in the fabricated device, we measured only a 3.5-dB extinction ratio at an applied voltage of 10 V. One reason for this is the use of SiN as a dielectric, which has a very high leakage current. The use of a high-quality Al_2O_3 layer deposited by atomic layer deposition might address this issue. Furthermore, an improved device could feature a tapered top SiN layer to enhance coupling between the 300-nm SiN and 600-nm SiN layers; however, fabrication of this device would require the use of e-beam lithography.

1

Introduction

Contents

In this chapter, we will discuss technology and devices required for optical communication. In this context, the need for efficient, compact, fast, and broadband electro-optical modulators will be explained. Graphene will be briefly introduced, and its properties will be discussed. Graphene-integrated photonic circuits will be presented as an alternative platform to existing technologies. Finally, we will review some techniques for the fabrication and characterization of graphene for photonics-related applications.

1.1 Optical interconnects

It has been predicted that integrated circuits will encounter an interconnection bottleneck. One of the main problems limiting high-data rate electrical interconnections over long distances is signal attenuation. Such attenuation is unavoidable in electrical wires because of the resistance of conductors and dielectric losses. This attenuation becomes worse at higher frequencies, leading to severe signal distortion [1].

To overcome the aforementioned issues of electrical interconnects, optical interconnects based on low-loss optical fiber links have been introduced, enabling ultra-high-speed communication. In addition, these data-transparent optical links provide a low cost solution. Fiber-optic communication has dominated the long-distance, metro, and access communication networks, for distances more than 100 m. Recently optical interconnects have also received attention for applications to much shorter interconnection, distances of 1 cm to 100 m and even for on-chip interconnects (distances of 100 µm to 1 cm).

Optical interconnects do not suffer from the bottlenecks associated with electrical interconnects. The losses in optical media are independent of the modulation speed. Crosstalk between adjacent fibers is negligible. Hence, optical interconnects provide high bandwidth, low power consumption, low latency, and low crosstalk compared with electrical interconnects. However, implementing them in communication systems remains challenging. For instance, the energy consumption on electrical backplanes is of the order of a few tens of pico-joules per bit. Therefore, target energies for optical interconnects should be approximately the same, or even lower.

1.2 Silicon photonics

Silicon, a high refractive index material, can be used to build a high contrast waveguide platform, allowing for compact photonic integrated circuits. The main advantage of Si is that it is widely used in electronics, therefore photonic integrated circuits can be fabricated using mature CMOS technology. A large

amount of passive components have already been successfully demonstrated on the SOI platform. Research is ongoing on this platform for the demonstration of active components. In this section, we focus on modulators, one of the main active devices and briefly review the state-of-the-art on modulators.

Many studies have been devoted to demonstrating light modulation with the use of various technologies, such as those based on lithium niobate (LN). LN modulators are broadband, operating in both C and L bands; high speed, and thermally stable; however, LN modulators are not easily scalable because of the difficulty of nanostructuring LN [2]. Si Mach-Zehnder modulators (MZMs) are high-speed and broadband; however, these modulators have a large footprint and consume large amounts of power. Intensity modulation at 60 Gb/s has been reported with the use of a 0.75-mm-long Si MZM [3]. Conversely, Si ring modulators are compact, but not broadband. These modulators are also highly sensitive to temperature variation [4]. GeSi-based electro-absorption modulators (EAMs) have a higher optical bandwidth than that of Si-based ring modulators and a lower footprint and power consumption than that of MZMs but have high costs associated with complex processing. A 100-Gb/s C-band GeSi EAM has recently been demonstrated by imec [5]. Ge EAMs are compact and high-speed; however, these modulators are also wavelength-dependent (10 nm operational bandwidth) and require many extra processing steps. A 56-Gb/S Ge EAM has also recently been reported [6]. In 2016, a monolithic EAM was demonstrated on an InP platform at 56 Gb/s by Fraunhofer HHI [7]. The same bitrate has recently been demonstrated by heterogeneous integration of InP-on-Si, in our group [8]. Although III-V-based devices are promising, they require high-cost technologies. An alternative technology is polymer-based modulators [9],[10]. A 100-Gb/s (dual binary) Si organic hybrid modulator has been reported by KIT [9]; however, polymer involved devices may suffer from long-term stability issues. All of discussed modulators thus far are external modulators. However, there are also interesting reports on directly modulated lasers (DML), including the monolithic DML [12], InP-on-Si DML published by our group [13] and VECSELs [14].

Table 1.1: State-of-the-art modulators.

Modulator type	Length	BW [GHz]	BR [Gb/s]	V_π	V_{pp}	DC ER [dB]	IL [dB]	OBW [nm]
LN modulators (on chip) [2]	2 mm	15	22	9	5.5	10	2	
Si MZ modulator [3]	0.75 µm	28	60	2.7	6.5	30	6.5	
Si ring modulator [4]	5 µm	20	44		2.2	9	1	
SiGe EAM [5]	80 µm	> 50	100		1.8	4	4.4	10
Ge EAM [6]	40 µm	> 50	56		2.5	4.6	4.9	22
Si organic hybrid modulator [7]	1 mm	100	100	1.1	1.4		2	
III-V-on-Si EAM [8]	80 µm	25	56		1.5	15	5	
Monolithic III-V EAM [9]	80 µm	35	56		1.9	18		
Monolithic III-V MZM [11]	4 mm	44	56		1.5	25		
Monolithic III-V DML [12]	250 µm	55	56			4		
III-V-on-Si DML [13]	340 µm	35	56		1.5	3.5		
VECSEL [14]	5 µm diameter	18	56		1.5			

The integration of graphene with Si photonics can introduce potentially a low cost technology with compact, high speed and broadband active devices such as modulators and photodetectors. In the next sections, we further discuss about the advantages of graphene.

1.3 Graphene

Graphite is a three-dimensional allotrope of carbon, which became widely known after the invention of the pencil in 1565 [15]. Its application as a writing instrument is attributed to the fact that graphite is composed of graphene layers that are bonded to each other by weak Van der Waals forces. Hence, when a pencil is pressed against a sheet of paper, graphene stacks can be produced on the paper, which might also contain individual graphene layers. Although graphene is produced every time someone writes with a pencil, it was first isolated 440 years after its invention, in 2004, by Andre Geim jointly with Konstantin Novoselov via a mechanical exfoliation method [16].

1.3.1 Graphene properties

Graphene is a semi-metal with a linear dispersion near the corners of the Brillouin zone. The six corners of the Brillouin zone are known as the Dirac points, and the electrons and holes at the Dirac points are known as Dirac fermions. With the fermi level at the Dirac points, graphene has minimum conductivity because of the zero density of states. However, the Fermi level of graphene can be tuned by doping; therefore, its conductivity can be modulated [17],[18]. An ultra-high mobility of 200,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ has been experimentally demonstrated for suspended graphene [19]. However, in reality, the quality of graphene and its substrates are limiting factors. Another remarkable property of graphene is its strength. The high strength of 1.42-Å-long carbon bonds makes graphene one of the strongest materials ever discovered (by weight) [18].

Graphene also exhibits excellent optical properties, which make it an ideal material for photonic and optoelectronic applications [20]. For example, the linear dispersion of Dirac electrons enables broadband applications. The high mobility of graphene makes it a suitable material for high-speed modulation of light. Saturation of the absorption is observed as a consequence of Pauli blocking. This is an important optical characteristic of graphene for its applications in the field of mode-locked lasers.

Figure 1.1 illustrates the absorption spectrum of graphene with finite doping and the optical transitions involved in the process. From near-infrared to visible frequencies, absorption can be attributed to interband transitions.

The 2.3% absorption of infrared light is particularly high considering the single-atom thickness of graphene [21]. In 2008, it was reported that the amount of absorbed light in a graphene layer is related to its fine structure constant, rather than being controlled by specific material parameters. On the basis of this result, adding another layer of graphene will increase the amount of absorption in proportion. [22].
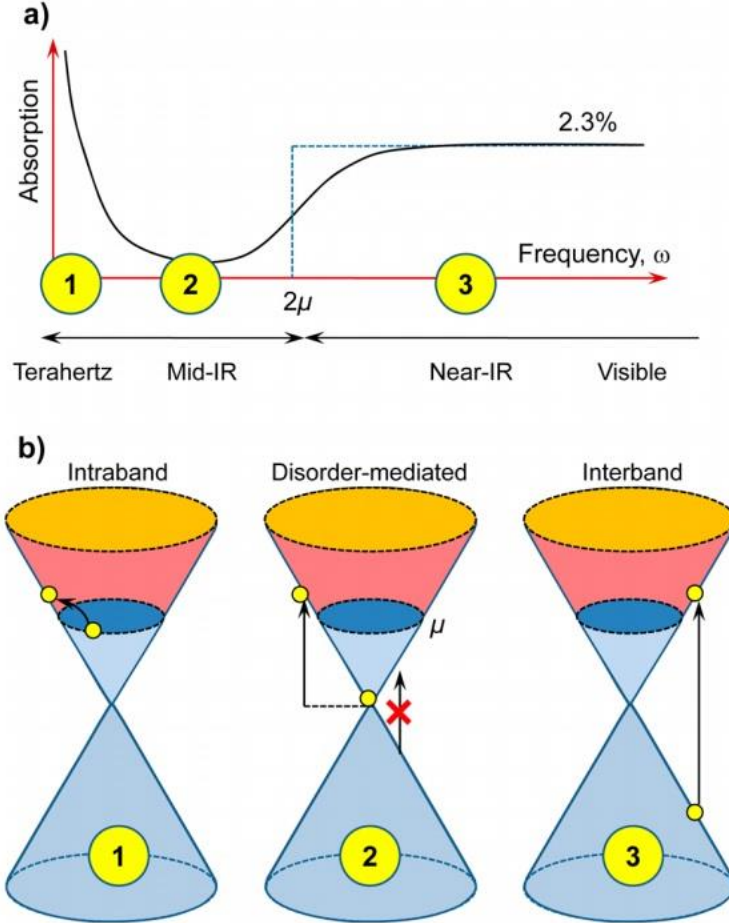
Figure 1.1: a) Absorption spectrum of n-doped graphene, illustrating the maximum absorption at terahertz frequencies, minimum absorption in the mid-infrared region, and 2.3% absorption in the near-infrared region. b) Optical transition processes (figure from [21]).

1.3.2 Graphene electro-absorption modulators

Integrated optical modulators with a high modulation speed, small footprint, low power consumption, and large optical bandwidth are highly desired to realize high-density, low-power optical interconnects for future data centers and high-performance computing systems [23],[24]. A modulation depth (or extinction ratio) greater than 7 dB is preferable for most applications, such as high-data rate interconnects. However, a modulation depth less than 4 dB is adequate for certain applications, such as passive mode-locking and short-distance data transmission [23]. The targeted energy consumption for future energy-efficient optical modulators is estimated to be a few fJ bit^{-1} for on-chip connections (approximately two orders of magnitude below current power consumption levels) [25]. The insertion loss of a modulator is also of practical significance, because it directly relates to the energy efficiency of the system. Other considerations, such as stability and cost, are also essential. In the following sections, we will review existing graphene EAMs. However, this technology is undergoing rapid development and further progress will likely be achieved with time.

In 2011, the first graphene waveguide EAM was fabricated at Berkeley by integration of a single-graphene layer on a silicon waveguide [26]. A schematic of the modulator is illustrated in **Figure 1.2**. A doped Si layer was used to connect the waveguide to the metal pad. In this design, both the Si layer and Si waveguide were doped to reduce the contact resistance. An ALD Al_2O_3 layer was deposited as a spacer between the waveguide and the graphene layer. CVD-grown graphene was then transferred onto the Al_2O_3 layer and metal pads were deposited on the graphene and the Si slab. By electrically tuning the Fermi level of graphene, a modulator with a 3-dB bandwidth of 1.2 GHz (at a bias voltage of −3.5 V) and an extinction ratio of 4 dB was demonstrated using a 4 V voltage swing. The device operated from 1.35 to 1.6 µm with an active area of 25 µm^2 (graphene length = 40 µm, waveguide width = 0.6 µm) and a negligible insertion loss.
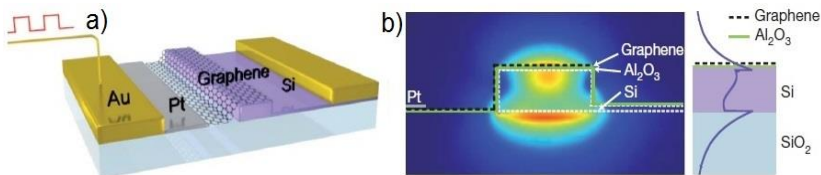
Figure 1.2: a) Graphene-based waveguide-integrated optical modulator. b) Left: TM mode profile in the graphene modulator. Right: Magnitude of the electric field in the cross section of the waveguide (figure from [26]).

In 2012, the same group reported a graphene modulator using a double-layer of graphene on a Si waveguide with an Al_2O_3 layer between the graphene layers acting as a spacer and contacting both graphene layers [27] (**Figure 1.3**). The device modulation depth was improved to 6.5 dB over a 40-µm-long device with an applied voltage of 6 V. The insertion loss was 4 dB. The 3-dB bandwidth of the device was 1 GHz at a 2-V bias voltage.
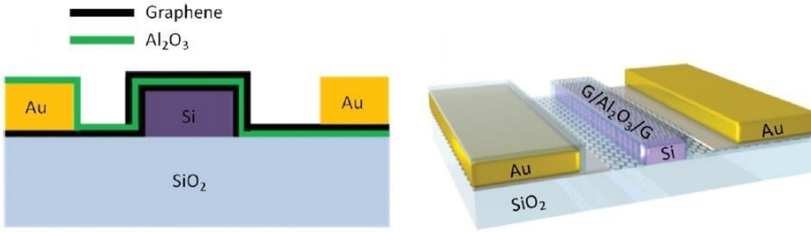
Figure 1.3: Double-layer graphene modulator (figure from [27]).

In 2015, another double-layer graphene modulator on Si was reported by AMO [28]. In this device, a longer graphene layer than that of previous devices was used; thus, the extinction ratio was improved to 16 dB with only a 3.3-dB insertion loss. The 3-dB bandwidth of the modulator was 670 MHz.
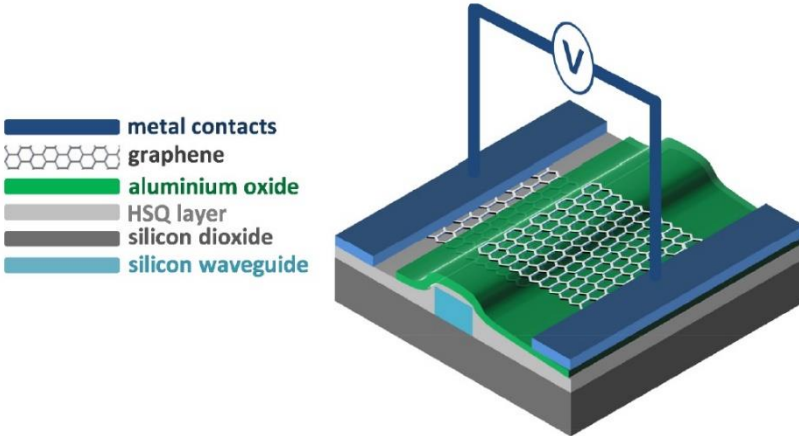
Figure 1.4: Double-layer graphene modulator on a Si waveguide (figure from [28]).

In 2015, a double-layer graphene modulator on a SiN ring resonator with 30-GHz modulation bandwidth was demonstrated (**Figure 1.5**). Similar to the previous modulators, metal pads were fabricated on two graphene layers. In this device, a relatively thick Al_2O_3 layer was deposited between the two graphene layers to reduce the device capacitance. Large signal measurements showed a 22-Gb/s non-return-zero (NRZ) modulation with 7.5 V_{pp} and a bias

voltage of −30 V. A modulation efficiency of 15 dB per 10 V and an energy consumption of ∼800 fJ per bit were reported. Although this device has a high extinction ratio and a high modulation bandwidth, it sacrificed broadband operation, an important property of graphene [29].
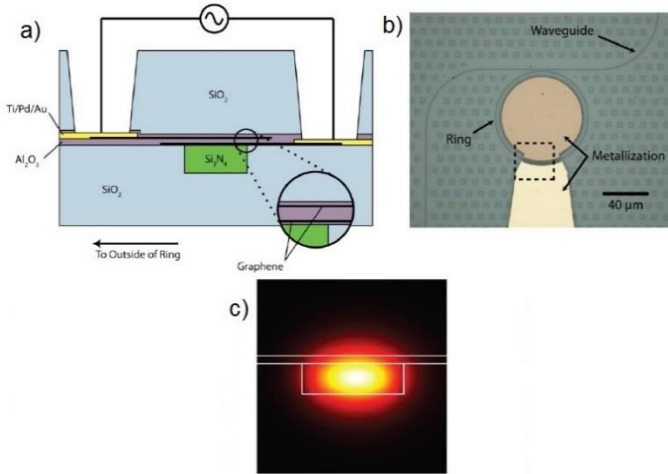
Figure 1.5: a) Schematic of a modulator consisting of a graphene/graphene capacitor integrated along a ring resonator. b) Optical image of the final fabricated device. c) TE mode profile in the graphene modulator (figure from [29]).

In 2014, a single-layer graphene modulator on a Si waveguide was reported by our group [30],[31]. The design was similar to that in reference [26]. The only difference in the design of [31], was that the waveguide was fully planarized to simplify the integration of graphene with the waveguide (**Figure 1.6**). A bandwidth of 5.9 GHz at a bias voltage of 1.75 V was achieved, and 10-Gb/s NRZ modulation with 2-dB dynamic extinction ratio was demonstrated (2.5 V_{pp} modulation).
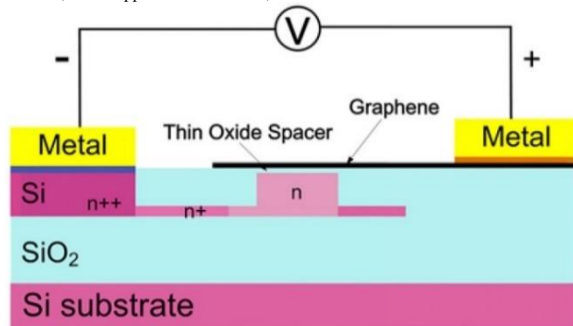
Figure 1.6: Single-layer graphene modulator on a planarized Si waveguide (figure from [31]).

In 2016, the Berkeley group reported a 35-GHz graphene modulator [32] by fabricating the double-layer graphene structure below the waveguide, as shown in **Figure 1.7**. A thick Al_2O_3 layer was deposited between two graphene layers to improve the speed. Consequently, with the use of a thick spacer, the modulation depth was only 2 dB under a bias voltage of 38 V.
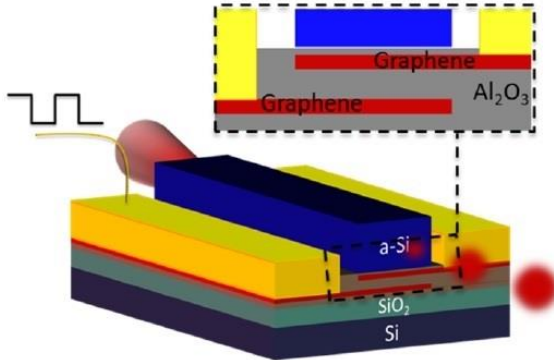
Figure 1.7: Schematic of a device showing two layers of graphene separated by a 120-nm Al_2O_3 dielectric layer to form a capacitor (figure from [32]).

Table 1.2 summarizes the important parameters of the previously mentioned graphene EAMs. A notable feature of all these modulators is the polarization. All operate with TM waveguides because the interaction of the TM mode with the graphene layer in these structures is higher than that of the TE mode. The only exception is in reference [29], which was based on a SiN platform. Polarization becomes an important factor when graphene-based devices are integrated with other photonic building blocks, such as lasers, which mostly operate in TE mode.

Table 1.2: State-of-the-art graphene modulators.

EAM type (ref)	OBW [nm]	3dB BW [GHz]	Max BR [Gb/s]	ER [dB]	IL [dB]	T [°C]	Vpp [V]	FP [µm²]	C [pF]	R [Ω]	ME [dB/V]	Pol
SLG*-Si strip wg [22]	250	1.2		4				25	0.22	600		TM
DLG*-Si strip wg [23]		1		6.5				16				TM
DLG*-Si strip wg [24]		0.67		16	3.3			156	2.3	105		TM
DLG-SiN ring [25]	0	30	22	15			7.5	30		Rc=500 Rs=500	1.5	TE
SLG-Si rib wg [27]	80	5.6	10	5.2	3.8	Static 20-49	2.5	37	0.08	241	1.5	TM
DLG-Planar a-Si wg on top [28]	140	35		2	0.9	Dynamic 25-145		18			0.052	TM

*SLG and DLG indicate single layer graphene and double layer graphene.

1.3.3 Graphene growth techniques

Although high-mobility graphene can be achieved through micromechanical exfoliation [33], this approach is not well suited for industrial applications because it suffers from a random distribution and the formation of flakes with uncontrollable size and thickness [34]. On the contrary, CVD growth of graphene is the most mature and scalable method. In this technique, carbon-containing gases are decomposed on metal surfaces such as Cu, Ni, Pd, Ir, and

Co at high temperatures [34]-[39], or on dielectrics [40]-[42], and converted into a graphene layer. Growth on copper foils enables fabrication of high-quality graphene over a large area. In addition, thin copper foils are inexpensive and can be easily etched to release the graphene layer. After copper etching, the transfer of graphene onto the desired substrates is possible. These features of copper make it an interesting material for graphene growth. **Figure 1.8** illustrates the three main steps in CVD graphene growth on copper foil.

The material of choice in the market is currently CVD-grown graphene on copper foil because the transfer of graphene from copper is much easier than that from other metals. The graphene used in this thesis was also grown on a copper foil by Graphenea [43].
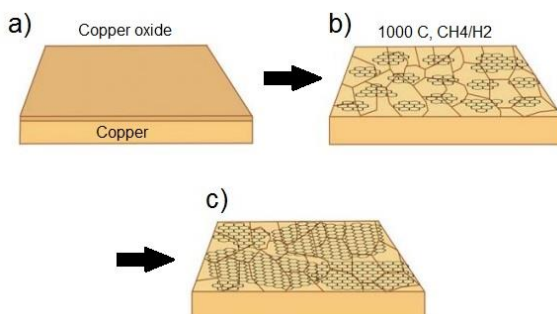
Figure 1.8: Schematic illustration of the three main stages of graphene growth on copper foil by the CVD method. a) Copper foil with a native oxide layer. b) Exposure of the copper foil to CH_4/H_2 atmosphere at 1000 °C, leading to nucleation of graphene islands. c) Enlargement of the graphene flakes with various lattice orientations (figure from [34]).

1.3.4 Graphene transfer

The most common approach for graphene transfer is to protect the graphene layer on the original growth substrate with PMMA. The substrate is then etched away to obtain a free-floating graphene-PMMA stack. The graphene-PMMA stack can then be scooped onto the selected substrate. Finally, the PMMA layer is removed on the target substrate to obtain a clean graphene layer. Substrate wet etching is feasible for metals such as Ni and Cu but is more challenging for metals such as Ir, Pd, and Pt [44]. In the following chapters, we will discuss the graphene transfer method in more detail.

1.3.5 Graphene visualization

Although graphene is produced every time one uses a pencil, finding graphene monolayers on a substrate is difficult. A visualization technique has been demonstrated for SiO_2 substrates. Using a model based on the Fresnel law, researchers at the University of Manchester have investigated the dependence of contrast on the SiO_2 thickness and light wavelength (**Figure 1.9**) [45],[46]. In this approach, graphene layers on several SiO_2/Si samples with different SiO_2 layer thicknesses were deposited. Normal light illuminated the graphene/SiO_2/Si substrates from air and the reflected light was measured. The contrast was defined as the relative intensity of the reflected light in the presence and absence of graphene. On the basis of these results, 300 nm and 90 nm were found to be the optimal SiO_2 thickness for producing the highest contrast [45].

Currently, commercial graphene on SiO_2 is on 300-nm SiO_2 substrates. Therefore, using green light, one can easily spot graphene layers on the substrate.
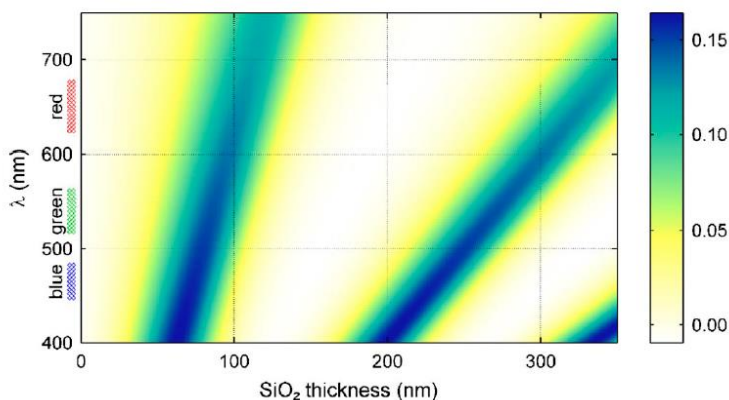
Figure 1.9: Color plot of graphene contrast as function of light wavelength and SiO_2 thickness. Color scale on the right indicates the expected contrast (figure from [45]).

Figure 1.10 shows graphene layers on 300-nm SiO_2 and 200-nm SiO_2 viewed with an optical microscope. The graphene layer is completely invisible on the 200-nm SiO_2 substrate [45].
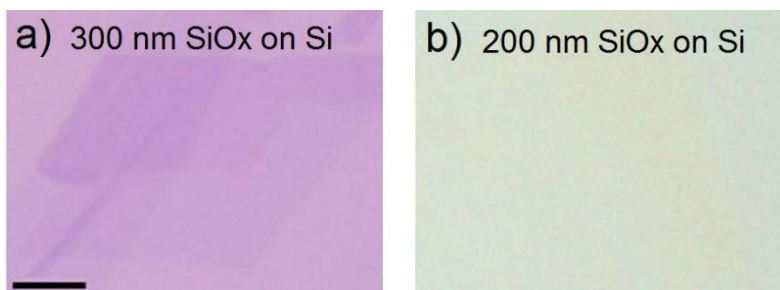
Figure 1.10: Graphene on Si substrates: a) 300-nm SiO$_2$; b) 200-nm SiO$_2$. Scale bar is 5 µm (figure from [45]).

Consequently, graphene layers on photonic devices are not visible either on the Si waveguide or in the trenches of the waveguide, which is a thick SiO$_2$ layer (>2 µm). Furthermore, graphene layers are very thin and not measurable with a standard profilometer. These features make the fabrication of graphene-based photonic devices challenging. However, graphene on 300-nm SiO$_2$ can be used as a substrate for basic characterization such as contact resistance or sheet resistance measurements. This substrate can also be used to develop specific fabrication processes, such as the bilayer resist process that is described in this thesis (chapter 3).

1.3.6 Graphene characterization techniques

To characterize the graphene layer quality, which involves information about the number of layers, thickness, defects, and the amount of doping, many techniques have been used, including atomic force microscopy (AFM), transmission electron microscopy (TEM), and Raman spectroscopy. Scanning electron microscopy (SEM) is another method for imaging of graphene. In the remaining sections of this chapter, each technique is briefly introduced.

1.3.6.1   Scanning electron microscopy

Scanning electron microscopy (SEM) is a non-contact and relatively convenient method for graphene observation. It is a useful technique for rapid characterization of micro- and nano-scale graphene features, including wrinkles, folding lines, and grain shapes. Although a SEM image can be used for an initial estimation of graphene quality, it is a challenging to use SEM as a technique for direct imaging of graphene. Because of the atomically thin structure of graphene, it is transparent to the high acceleration voltages used in SEM imaging and its properties can also be altered during imaging [47].
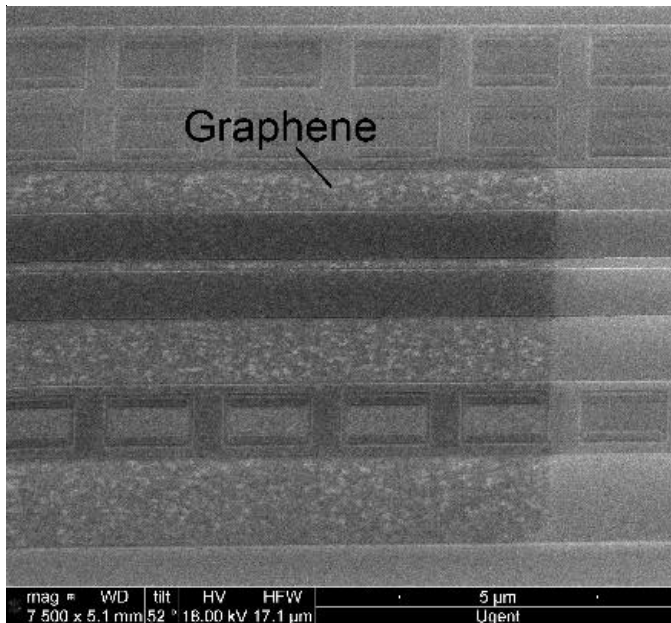
Figure 1.11: SEM image of a monolayer graphene on one of our SOI samples.

1.3.6.2   Atomic force microscopy

Atomic force microscopy (AFM) is used to map the topography of materials. Its accuracy depends on the adhesion of an AFM probe tip to the surface. This method is extensively used because it provides three-dimensional images, enabling the measurement of film thickness. However, AFM has proven to be inaccurate because of different reported values for single-layer graphene thickness, ranging between 0.4 and 1.7 nm [48]. The discrepancy in the reported values has been attributed to AFM probe tip and surface interactions, image feedback settings, and surface chemistry [48].
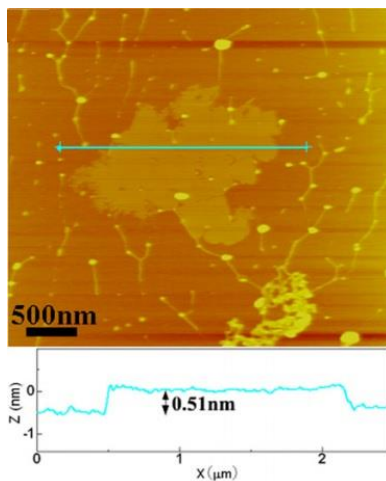
Figure 1.12: AFM image of graphene (figure from [49]).

1.3.6.3 Transmission electron microscopy

Transmission electron microscopy (TEM) is another technique for measuring the thickness of graphene and estimating the number of layers. In this method, the electron beam is focused on the folding edge of a flake. At the folding edge, graphene planes are parallel to the electron beam, and each plane diffracts electrons and appears as a dark line in the image. The dark lines of the image can be counted to determine the number of layers and the thickness of the flake [50]. **Figure 1.13** shows a TEM image of multilayer graphene.
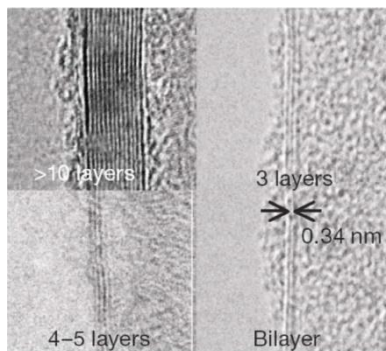
Figure 1.13: TEM image of multilayer graphene (figure from [50]).

1.3.6.4   **Raman spectroscopy**

Raman spectroscopy is a powerful method for precise measurement of graphene quality, including the number of layers, doping level, and defects [51]-[54]. The most important bands (for extraction of the information about graphene equality) in the Raman spectrum are the D, G, and 2D bands, appearing near 1350, 1582, and 2700 cm^{-1}, respectively. The 2D band is so named because it occurs at approximately twice the frequency of the D-band. **Figure 1.14** shows a Raman spectrum of pristine and defected graphene. In the spectrum of high-quality and defect-less graphene, the 2D band is expected to have higher intensity compared to G band. The D and D' bands appear in the spectrum of graphene with defects.
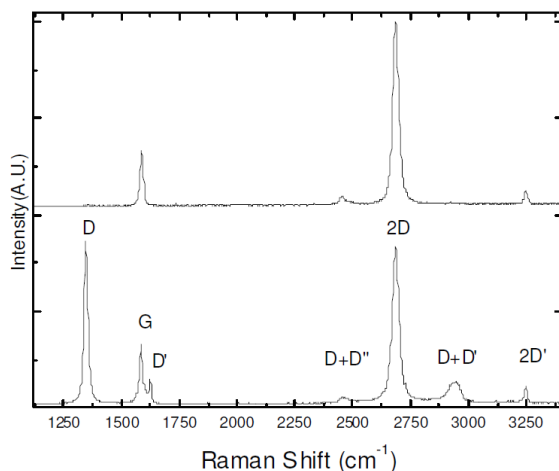
Figure 1.14: Raman spectra of pristine (top) and defected (bottom) graphene. (figure from [55]).

1.4 Research objectives

This project has three main objectives. First, to perform a detailed simulation of various configurations of graphene EAMs and switches on Si and SiN integrated waveguide platforms. On the basis of these simulations, we will further design and fabricate graphene-based switches. Our second objective is the development of micron-size graphene transfer printing based on a commercial transfer printer. The third objective is fabrication and characterization of a graphene-based switch using the developed transfer technique. The performance of the devices will be examined to establish the versatility of our developed transfer method. To accomplish the third

objective, we will fabricate a hybrid graphene-Si photonic crystal cavity and a double-layer graphene-based device on a SiN platform.

In this research, the graphene was provided by Graphenea. The SOI and SiN waveguides were fabricated with the use of Imec's pilot lines. Other works, such as the simulation, design, fabrication, and characterization, were performed in the Photonic Research Group at Ghent University.

1.5 Outline of the work

In chapter 1, we review the state-of-the-art modulators, the background of graphene EAMs, graphene properties, and characterization techniques. The thesis objectives are then defined.

In chapter 2, simulation results for different structures are presented for both Si and SiN platforms. On the basis of these simulations, the trade-offs between the important parameters for both modulators and switches are discussed.

In chapter 3, we explain the fabrication processes used to make graphene-based devices. This chapter primarily focuses on the fabrication and characterization of different TLM devices and optimization of the main processing steps of the graphene sample.

In chapter 4, a micron-size graphene transfer method is developed with the use of an automated tool. This chapter presents details of the processing and transfer printing. Raman spectroscopy and some basic optical and electrical characterizations are performed to evaluate the graphene quality after printing.

In chapter 5, we demonstrate graphene-based switches integrated onto a front-coupled and a side-coupled Si photonic crystal cavity, using the transfer method presented in chapter 4. The fabrication and characterization of these devices are discussed in this chapter. We demonstrate high extinction ratios of 17 dB with the front-coupled cavity and 4.7 dB with the side-coupled cavity.

In chapter 6, a double-layer graphene-based switch embedded in a SiN waveguide is presented. This device was also fabricated based on the developed transfer printing technique. The fabrication process steps, initial characterization results, requirements, and challenges are discussed.

Finally, in chapter 7, conclusions and a future outlook are given.

1.6 Publications

Publications in international journals

1. **L. Abdollahi Shiramin**, W. Xie, B. Snyder, P. De Heyn, P. Verheyen, G. Roelkens, D. Van Thourhout, High Extinction Ratio Hybrid Graphene-Silicon Photonic Crystal Switch, submitted for publication in IEEE Photonics Technology Letters, (submitted).
2. A. Abbasi, **L. Abdollahi Shiramin**, B. Moeneclaey, J. Verbist, X. Yin, J. Bauwelinck, D. Van Thourhout, G. Roelkens, G. Morthier, III-V-on-Silicon C-band High-Speed Electro-Absorption Modulated DFB Laser, Journal of Lightwave Technology, (2017).
3. **L. Abdollahi Shiramin**, A. Bazin, S. Verstuyft, S. Lycke, P. Vandenabeele, G. Roelkens, D. Van Thourhout, Transfer printing of micron-size graphene for photonic integrated circuits and devices, ECS Journal of Solid State Science and Technology, p.P435-P439 (2017).
4. **L. Abdollahi Shiramin**, D. Van Thourhout, Graphene Modulators and Switches Integrated on Silicon and Silicon Nitride Waveguide, Journal of Selected Topics in Quantum Electronics (JSTQE), p.36000107 (2017).

Publications in international conferences

1. A. Abbasi, J. Verbist, **L. Abdollahi Shiramin**, M. Verplaetse, T. De Keulenaer, R. Vaernewyck, R. Pierco, A. Vyncke, X. Yin, G. Morthier, J. Bauwelinck, G. Roelkens, 100 Gb/s Duobinary Electro-Absorption Modulation of an InP-on-Si DFB Laser Diode, submitted for publication in OFC conference, United States, (submitted).
2. **L. Abdollahi Shiramin**, W. Xie, B. Snyder, P. De Heyn, P. Verheyen, G. Roelkens, D. Van Thourhout, Electrically Tunable Absorption in Graphene-Integrated Silicon Photonic Crystal Cavity, 14th International Conference on Group IV Photonics (GFP), Berlin, (2017).
3. A. Abbasi, **L. Abdollahi Shiramin**, B. Moeneclaey, J. Verbist, X. Yin, J. Bauwelinck, D. Van Thourhout, G. Roelkens, G. Morthier, 2x56 Gbps Electroabsorption Modulated III-V-on-silicon DFB Laser, accepted for publication in European Conference on Optical Communication (ECOC), Sweden, (2017).
4. **L. Abdollahi Shiramin**, A. Bazin, S. Verstuyft, S. Lycke, P. Vandenabeele, G. Roelkens, D. Van Thourhout, Demonstration of a New Technique for the Transfer Printing of Graphene on Photonic Devices, Conference on Lasers and Electro-Optics (CLEO), United States, p.paper SW4K.6 (2017).
5. **L. Abdollahi Shiramin**, D. Van Thourhout, Design of Hybrid Integrated Graphene Optical Switch with an III-V-on-Si laser, European Conference on Integrated Optics (ECIO'2017), Netherlands, p.paper WP1.5 (2 pages) (2017).

6. K. Alexander, M. Mohsin, U.D. Dave, **L. Abdollahi Shiramin**, S. Clemmen, D. Neumaier, B. Kuyken, D. Van Thourhout, Electrically Tunable Optical Nonlinearity of Graphene-covered SiN waveguides, accepted for publication in Conference on Lasers and Electro-Optics (CLEO) 2017, United States, (2017).
7. D. Van Thourhout, **L. Abdollahi Shiramin**, C. Alessandri, K. Alexander, B. Kuyken, M. Pantouvaki, I. Asselberghs, S. Brems, J. Van Campenhout, C. Huyghebaert, Hybrid Graphene-Silicon Photonics Devices for Telecom and Datacom, Graphene 2017, Spain, (2017).
8. D. Van Thourhout, M. Pantouvaki, H. D'heer, K. Alexander, B. Kuyken, I. Asselberghs, S. Brems, C. Huyghebaert, **L. Abdollahi Shiramin**, C. Alessandri, J. George, J.Beeckman, M. Hsu, C.Merckling, J. Van Campenhout, New materials for modulators and switches in silicon photonics, SPIE , United States, p.paper 10108-3 (2017).
9. **L. Abdollahi Shiramin**, D. Van Thourhout, Graphene devices for outperformed optical interconnects, Proceedings Symposium IEEE Photonics Society Benelux, Belgium, p.203-206 (2016).
10. D. Van Thourhout, Z. Wang, B. Tian, Y. Shi, M. Pantouvaki, C. Merckling, Y. Hu, I. Asselberghs, S. Brems, **L. Abdollahi Shiramin**, C. Alessandri, J. George, J. Beeckman, M. Hsu, P .Absil, J. Van Campenhout, New Materials for Multifunctional Photonic ICs, Nanofotonica (invited), Spain, p.81 (2016).
11. **L. Abdollahi Shiramin**, D. Van Thourhout, Broadband Double layer Graphene Switch Integrated on Silicon and Silicon Nitride Waveguide, Graphene 2016, Italy, (2016).

References

[1] D. A. B. Miller, "Optical interconnects to electronic chips", Applied.Optics, 49, 2010.

[2] D. Janner, D. Tulli, M. Garca-Granda, M. Belmonte, and V. Pruneri, "Micro-structured integrated electro-optic LiNbO3 modulators", Laser & Photonics Reviews 3, 301, 2009.

[3] Xi Xiao, Hao Xu, Xianyao Li, Zhiyong Li, Tao Chu, Yude Yu, and Jinzhong Yu "High-speed, low-loss silicon Mach–Zehnder modulators with doping optimization", Opt. Exp, 21, 4, 2013.

[4] E. Timurdogan, C. M. Sorace-Agaskar, J. Sun, E. S. Hossieni, A. Biber-man, and M. R. Watts, "An ultralow power athermal silicon modulator," Nature Commun., vol. 5, pp. 4008-1–4008-11, 2014.

[5] J. Verbist, M. Verplaetse, A. Srinivasan, P. De Heyn, T. De Keulenaer, R. Vaernewyck, R. Pierco, A. Vyncke, P. Verheyen, S. Balakrishnan, G. Lepage, M. Pantouvaki, P. Absil, X.Yin, G. Roelkens, G. Torfs, J. Van Campenhout, J. Bauwelinck, "Real-Time 100 Gb/s NRZ-OOK Transmission with a Silicon Photonics GeSi Electro-Absorption Modulator", IEEE Optical Interconnects Conference, 2017.

[6] S. Ashwyn Srinivasan, M. Pantouvaki, S. Gupta, H. Tao Chen, P. Verheyen, G. Lepage, G. Roelkens, K. Saraswat, D. Van Thourhout, P. Absil, and J. Van Campenhout, "56 Gb/s Germanium Waveguide Electro-Absorption Modulator", Journal of lightwave technology, 34, 2016.

[7] M. Theurer, H. Zhang, Y. Wang, W. Chen, L. Chen, U. Troppenz, G. Przyrembel, A. Sigmund, M. Moehrle, and M. Schell, "2 × 56 GB/s from a Double Side Electroabsorption Modulated DFB Laser and Application in Novel Optical PAM4 Generation, Journal of light wave technology", 35, 4, 2017.

[8] A. Abbasi, L. Abdollahi Shiramin, B. Moeneclaey, J. Verbist, X. Yin, J. Bauwelinck, D. Van Thourhout, G. Roelkens, G. Morthier, "2 × 56 Gbps Electroabsorption Modulated III-V-on-silicon DFB Laser", ECOC 2017.

[9] H. Zwickel, et al, "100 Gbit/s serial transmission using a silicon-organic hybrid (SOH) modulator and a duobinary driver IC", OFC 2017.

[10] M. Lee, H. E. Katz, C. Erben, D. M. Gill, P. Gopalan, J. D. Heber and D. J. McGee, "Broadband Modulation of Light by Using an Electro-Optic Polymer", Science, 298, 1401-1403, 2002.

[11] S. Lange, M. Gruner, C. Meuer, R. Kaiser, M. Hamacher, K.Velthaus, and M. Schell, "Low Switching Voltage Mach–Zehnder Modulator Monolithically Integrated With DFB Laser for Data Transmission up to 107.4 Gb/s", JLT, Vol. 34, No. 2, 2016.

[12] Y. Matsui, R. Schatz, T. Pham, W. A. Ling, G. Carey, H. M. Daghighian, D. Adams, T. Sudo, and C. Roxlo, "55 GHz Bandwidth Distributed Reflector Laser", JLT, Vol. 35, No. 3, 2017.

[13] A. Abbasi, B. Moeneclaey, J. Verbist, X. Yin, J. Bauwelinck, G.H. Duan , G. Roelkens , G. Morthier, "Direct and electro-absorption modulation of a III-V-on-silicon DFB laser at 56 Gbps", JSTQE, 2017.

[14] D. M. Kuchta, T. N. Huynh, F. E. Doany, L. Schares, C. W. Baks, C. Neumeyr, A. Daly, B. Koge, J. Rosskopf, and M. Ortsiefer, "Error-Free 56 Gb/s NRZ Modulation of a 1530-nm VCSEL Link", JLT, Vol. 34, No. 14, 2016.

[15] H. Petroski, "The Pencil: A History of Design and Circumstance", pp. 36–47, 1989.

[16] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva and A. A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films", Science 306, 666, 2004.

[17] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov and A. K. Geim, "The electronic properties of graphene", Review of modern physics, 81, 2009.

[18] A.V. Rozhkov, A.O. Sboychakova, A.L. Rakhmanov and Franco Noria, "Electronic properties of graphene-based bilayer systems", Physics reports, Volume 648, Pages 1–104, 2016.

[19] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, H. L. Stormer, "Ultrahigh electron mobility in suspended graphene", Solid. State. Commun, 146, 351, 2008.

[20] F. Bonaccorso, Z. Sun, T. Hasan and A. C. Ferrari, "Graphene photonics and optoelectronics", Nat. Photon, Vol4, 2010.

[21] T. Low and P. Avouris, "Graphene Plasmonics for Terahertz to Mid-Infrared Applications", ACS nano,. 8 (2), pp 1086–1101, 2014.

[22] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres and A. K. Geim, "Fine Structure Constant Defines Visual Transparency of Graphene", Science, Vol. 320, Issue 5881, pp. 1308, 2008.

[23] G. Reed, G. Mashanovich, F. Y. Gardes, D. J. Thomson, "Silicon optical modulators", Nat.Photon, 4, 8, 518–526, 2010.

[24] I. A. Young, E. Mohammed, J. T. S. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, P. L.D. Chang, "Optical I/O Technology for Tera-Scale Computing", Solid-State Circuits, IEEE Journal of, 45, 1, 235–248 2010.

[25] D. A. B. Miller, "Energy consumption in optical modulators for interconnects", Opt. Express, 20, A293–A308, 2012.

[26] M. Liu , X. Yin, E. Ulin-Avila, T. Zentgraf, L. Ju, F. Wang, X. Zhang, "A graphene-based broadband optical modulator", Nature, vol. 474, no. 7349, pp. 64-67, 2011.

[27] M. Liu, X. Yin, and X. Zhang, "Double-layer graphene optical modulator", Nano lett,. vol. 12, no.3, pp. 1482-1485, 2012.

[28] M. Mohsin, D. Schall, M. Otto, A. Noculak, D. Neumaier, H. Kurz, "Graphene based low insertion loss electroabsorption modulator on SOI waveguide", Opt. ex, 22, 12, 2014.

[29] C. T. Phare, Y.H. Daniel Lee, J. Cardenas, M. Lipson, "Graphene electro-optic modulator with 30GHz bandwidth", Nat. Photon. 9, 511-514, 2015.

[30] Y. Hu, et al., "Broadband 10Gb/s Graphene Electro-Absorption Modulator on Silicon for Chip-Level Optical Interconnects", IEDM, 2014.

[31] Y. Hu, et al. "Broadband 10 Gb/s operation of graphene electro-absorption modulator on silicon", Laser Photon Rev, 2016.

[32] H. Dalir. Y. Xia, Y. Wang, X. Zhang, "Athermal Broadband Graphene Optical Modulator with 35 GHz Speed", ACS Photonics, 3, 2016.

[33] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene", Nature Nanotechnol. 3, 491–495 (2008).

[34] C. Mattevi, H. Kima and M. Chhowalla, "A review of chemical vapour deposition of graphene on copper", Journal of Materials Chemistry, 21, 3324-3334, 2011.

[35] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils", Science, 324, 1312, 2009.

[36] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.- H. Ahn, P. Kim, J.-Y. Choi and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes", Nature, 457, 706, 2009.

[37] S.Y. Kwon, C. V. Ciobanu, V. Petrova, V. B. Shenoy, J. Bare, V. Gambin, I. Petrov and S. Kodambaka, "Growth of Semiconducting Graphene on Palladium", Nano. Lett., 9, 3985, 2009.

[38] J. Coraux, A. T. N'Diaye, C. Busse and T. Michely, "Structural Coherency of Graphene on Ir (111)", Nano Lett., 2008, 8, 565.

[39] H. Ago, Y. Ito, N. Mizuta, K. Yoshida, B. Hu, C. M. Orofeo, M. Tsuji, K. Ikeda and S. Mizuno, "Epitaxial Chemical Vapor Deposition Growth of Single-Layer Graphene over Cobalt Film Crystallized on Sapphire", 4,12, 7407–7414, 2010.

[40] Kim.Y.; Joo. K.; Jerng. S.; Lee.J.; Yoon. E.; Chun. S, "Direct growth of patterned graphene on SiO_2 substrates without the use of catalysts or lithography", Nanoscale. 6, 10100-10105, 2014.

[41] G. Pan, B. Li. B, M. Heath, D. Horsell, M. Lesley, L. Taan, S. Awan, "Transfer-free growth of graphene on SiO_2 insulator substrate from sputtered carbon and nickel films", Carbon. 65, 349–358, 2013.

[42] D.Q. McNerny, B. Viswanath, D. Copic, F.R. Laye, C. Prohoda, A.C. Brieland-Shoultz, E.S. Polsen, N.T Dee, V.S. Veerasamy, A.J. Hart, "Direct fabrication of graphene on SiO_2 enabled by thin film stress engineering", Sci. Rep, 4, 2014.

[43] www.graphenea.com

[44] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, and P. N. First, "Ultrathin Epitaxial

Graphite: 2D Electron Gas Properties and a Route toward Graphene-based Nanoelectronics" J. Phys. Chem. B 108, 19912–19916, 2004.

[45] P. Blakea, E. W. Hill, A. H. Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, A. K. Geim, "making graphene visible", Appl. Phys. Lett, 91, 063124, 2007.

[46] C. Casiraghi, A. Hartschuh, E. Lidorikis, H. Qian, H. Harutyunyan, T. Gokus, K. S. Novoselov, A. C. Ferrari, "Rayleigh Imaging of Graphene and Graphene Layers", Nano. lett, 2007.

[47] J. Lee, X. Zheng, R. C. Roberts, P. X.L. Feng, "Scanning electron microscopy characterization of structural features in suspended and non-suspended graphene by customized CVD growth", Diamond. Related Materials, 54, 2015.

[48] C. J. Shearer, A. D. Slattery, A. J. Stapleton, J. G. Shapter, C. T. Gibson, "Accurate thickness measurement of graphene", Nanotechnology 27, 2016.

[49] Z. Shen, J. Li, M. Yi, X. Zhang, and S. Ma, "Preparation of graphene by jet cavitation", Nanotechnology, 22, 2011.

[50] L. Dong, Q. Chen, "Properties, synthesis, and characterization of graphene", Mater. Sci, 4, 2010.

[51] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, A. K. Geim, "Raman Spectrum of Graphene and Graphene Layers", PRL, 2006.

[52] C. Casiraghi, S. Pisana, K. S. Novoselov, A. K. Geim, A. C. Ferrari, "Raman fingerprint of charged impurities in graphene", Applied. Phys. lett, 91, 233108, 2007.

[53] A. C. Ferrari, D. M. Basko, "Raman spectroscopy as a versatile tool for studying the properties of graphene", Nat. Nanotech, 8, 2013.

[54] L.M. Malard, M.A. Pimenta, G. Dresselhaus, M.S. Dresselhaus, "Raman spectroscopy in graphene", Physics Reports 473, 51-87, 2009.

[55] A. C. Ferrari, D. M. Basko, "Raman spectroscopy as a versatile tool for studying the properties of graphene", Nat.Nanotech, 8, 235–246, 2013.

2

Design of graphene-based modulators and switches

Contents

An optical transceiver incorporates a transmitter, receiver, and an optical fiber transmission line. The workhorse of the transmitter is an optical modulator. Waveguide-integrated optical modulators are important devices for compact and energy-efficient transceivers, where the electrical signals are converted to optical data. In this chapter, we propose several designs for graphene modulators and switches and outline strategies to improve the performance of these devices. Some of the text in this chapter has been adapted from reference [1].

2.1 Modelling of graphene devices

To understand the interaction of light guided in an integrated waveguide with a graphene layer, the electromagnetic field is numerically simulated. Since graphene is a monolayer film, only the in-plane components of the electric field play a role in the interaction with light. Therefore, in the simulation the graphene layer is defined as a conductive surface. In this thesis, we have used the finite element solver COMSOL (based on finite element method) to obtain the optical modes. For further calculations, the optical modes were imported in MATLAB exploiting the MATLAB Livelink module.

2.2 Graphene conductivity

The conductivity of graphene can be calculated using the so-called Kubo formula [2].

$$\sigma(\omega, \mu c, \Gamma, T) = \frac{-je^2(\omega + j2\Gamma)}{\pi\hbar^2} \left[\frac{1}{(\omega + j2\Gamma)^2} \int_0^\infty \varepsilon \left(\frac{\partial f_d(\varepsilon)}{\partial \varepsilon} - \right. \right.$$

$$\left. \left. \frac{\partial f_d(-\varepsilon)}{\partial \varepsilon} \right) d\varepsilon - \int_0^\infty \frac{f_d(-\varepsilon) - f_d(\varepsilon)}{(\omega + j2\Gamma)^2 - 4(\varepsilon/\hbar)^2} d\varepsilon \right] \tag{2.1}$$

where $-e$ is the charge of an electron, $\hbar = h/2\pi$ is the reduced Plank's constant, $f_d(\varepsilon) = (e^{(\varepsilon - \mu_c)/K_B T} + 1)^{-1}$ is the Fermi-Dirac distribution, and k_B is Boltzman's constant.

The conductivity depends on the wavelength of light, the chemical potential μ_c of the graphene layer (controlled through the applied voltage), the carrier relaxation time ($\tau_r = 1/\Gamma$, which depends on the quality of the graphene) and the temperature. In all simulations in this work, we assumed room temperature conditions $T = 300K$.

Figure 2.1 depicts graphene's conductivity for the scattering rates of 13 fs and 65 fs using equation 2.1, taking into account both inter-band (the transition of an electron from conduction band to the valence band) and intra-band (the transition of an electron in the conduction or in the valence band to an upper state) transitions. The proposed values for the scattering rate were observed in recent experiments [3],[4] and a scattering rate between these two values is expected for experimental CVD-type graphene currently available.
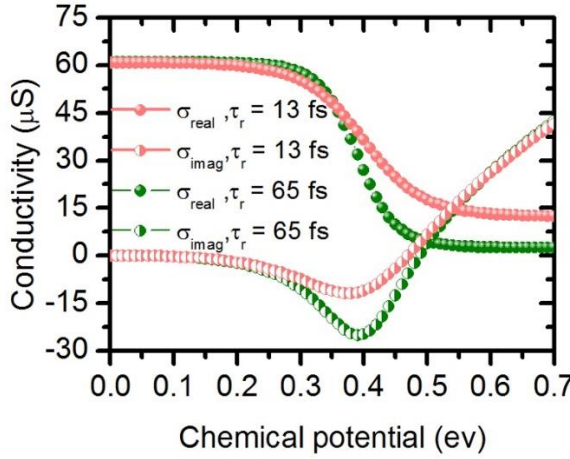
Figure 2.1: Real and imaginary part of graphene conductivity as function of the chemical potential for the scattering time (τ_r) of 13 and 65 fs at optical frequencies.

For an isolated graphene sheet, the chemical potential μ_c is determined by the carrier density n_s,

$$n_s = \frac{2}{\pi \hbar^2 v\_f^2} \int_0^\infty \varepsilon [f_d(\varepsilon) - f_d(\varepsilon + 2\mu_c)] d\varepsilon \tag{2.2}$$

where $v\_f = 9.5 \times 10^5$ m/s is the fermi velocity [2]. The carrier density can be controlled by applying a gate voltage or chemical doping. For the undoped and ungated case at $T = 0$ K, $n_s = \mu_c = 0$.

2.3 Graphene modulators and switches on Si and SiN

In this section, we propose several designs for graphene-based switches and modulators. **Figure 2.2** shows four structures where the first two configurations are based on a silicon waveguide and were originally proposed in [5],[6]. The main difference is that the waveguides are assumed to be planarized by CMP (chemical mechanical polishing) to ease the integration process with the graphene layer (see also [7]). The single layer graphene on silicon configuration (SLG-Si) shown in **Figure 2.2**(a) has a single layer of graphene transferred on the silicon waveguide, with a thin oxide layer in between. The silicon waveguide here serves as the capacitor plate. The double-layer graphene on silicon configuration (DLG-Si) has two layers of graphene separated by a thin dielectric, on the top [**Figure 2.2**(b)]. Typically,

a thin layer of Aluminum Oxide deposited by atomic layer deposition is used as the dielectric in this capacitive stack. The voltage to drive the device is now applied between the top and bottom graphene layer. The double-layer graphene on silicon nitride device (DLG-SiN, **Figure 2.2**(c)) is conceptually identical to the DLG-Si, except for the fact that the waveguide is now formed by a lower index Si_3N_4 strip ($n_{Si3N4} = 2.0$ vs. $n_{Si} = 3.5$). Finally, given that Si_3N_4 is a deposited material, it is possible to embed the double-layer graphene stack within the waveguide core, leading to the double-layer graphene embedded in SiN device (DLG-E-SiN) shown in **Figure 2.2**(d).
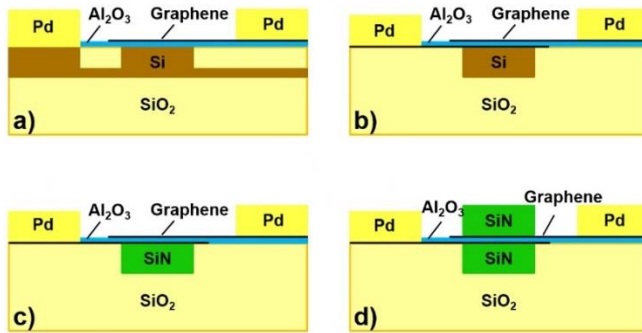
Figure 2.2: Schematics of graphene-based waveguide integrated electro-optical devices. a) SLG-Si, b) DLG-Si, c) DLG-SiN, d) DLG-E-SiN.

2.3.1 Static performance

Figure 2.3 plots the absorption as function of the waveguide width, at the neutrality point (μ_c=0 eV) for the different proposed waveguide configurations. The absorption is a measure for the interaction between the optical mode and the graphene layer, hence a higher value is preferred. **Figure 2.3**(a),(b) shows that for all structures the absorption increases with increasing waveguide width (assuming waveguide height of 220nm for the Si structures and 300nm for the SiN structures) except for TE-polarization on the Si waveguide. However, there are important differences between different configurations. Assuming quasi TM polarization, the DLG-Si devices exhibit almost twice the absorption of the SLG-Si device. For TE-polarization, the absorption in the Si-based devices is considerably lower (up to 0.12 dB/µm and 0.08 dB/µm for DLG-Si and SLG-Si devices respectively). This is related to the interaction with the strong longitudinal electric field component at the top interface of the silicon waveguides (note that the graphene sheet does not interact with the out-of-plane field components [2]). In the SiN-devices on the other hand, the quasi TE-polarized modes exhibit higher interaction with

the graphene film than the quasi TM modes. The DLG-SiN has lower absorption than the DLG-Si device but by embedding the graphene stack within the SiN waveguide, the absorption level of DLG-E-SiN can be increased again, almost to the level of the DLG-Si, albeit at larger waveguide dimensions. The simulations shown in **Figure 2.3**(a),(b) were carried out for a gate oxide d_{Al2O3} = 5 nm. Varying the gate oxide from 1nm to 15nm has very limited impact on the absorption (<0.03 dB/µm). In the case of DLG-E-SiN (TM mode), the mode leaks to the buried oxide and the mode near the interface of the SiN waveguide and graphene is very weak. This leads to very low interaction of the mode with the graphene layer and therefore low absorption.

Finally, it can be seen that, e.g. for the DLG-E-SiN with optimized layer thickness, the absorption at a wavelength of 1310nm is significantly higher than for 1550 nm [**Figure 2.3**(b)]. This is related to a higher overlap of the optical mode with the graphene layer at 1310 nm, rather than to a change in the intrinsic absorption properties of graphene, which are fairly constant over the wavelength interval considered.

Figure 2.4 depicts the effect of the SiN waveguide thickness on the absorption of the DLG-E-SiN device both at a wavelength of 1310 nm and 1550 nm, assuming the graphene layers are embedded symmetrically in the center of the waveguide. At 1550 nm, the absorption peaks for a total waveguide thickness of 300 nm (150 nm bottom layer, 150 nm top layer), while at 1310 nm it reaches its maximum for a 250 nm thick waveguide. In the remainder of the text we assume a 300 nm thick waveguide for both wavelengths. Simulations further also showed that the 220 nm thick silicon waveguide widely used in the industry is close to optimal in terms of height.
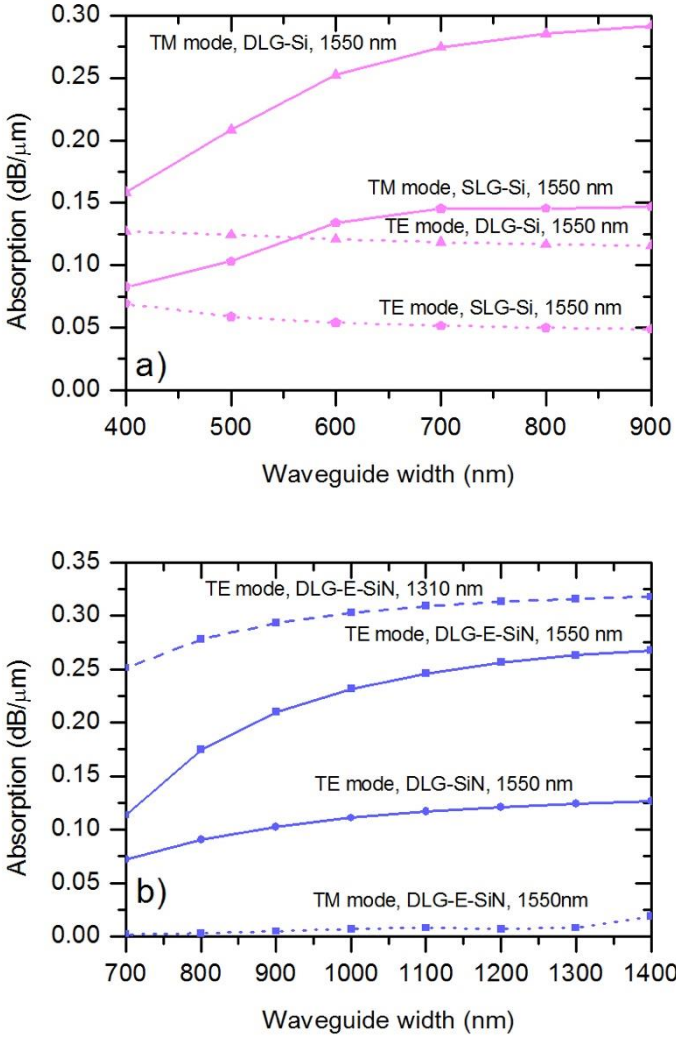
Figure 2.3: a) TE and TM mode absorption in DLG-Si and SLG-Si, as function of waveguide width. b) TE and TM mode absorption in DLG-E-SiN, TE mode absorption in DLG-SiN, as function of waveguide width. All were simulated for τ_r =65 fs, T = 300 K, λ = 1550 nm (and 1310 nm for DLG-E-SiN).
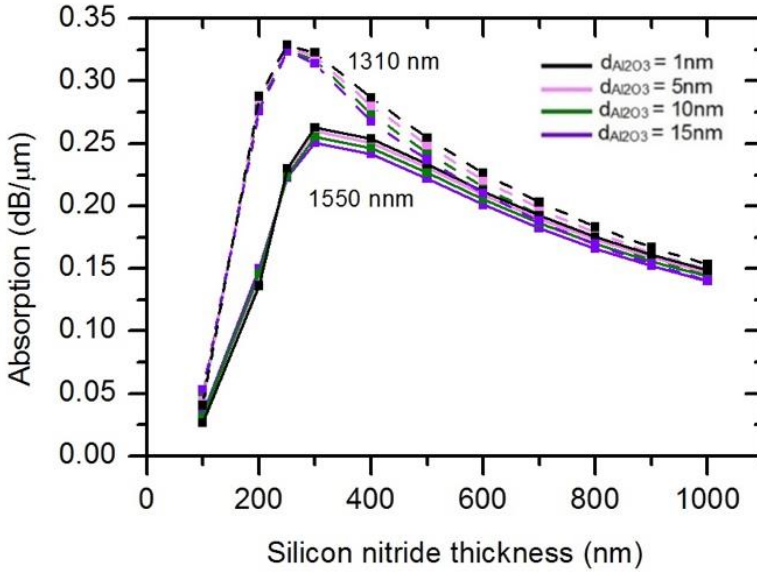
Figure 2.4: TE mode absorption in DLG-E-SiN as function of bottom SiN thickness. All were simulated for τ_r = 65 fs, T = 300 K, λ = 1550 nm and 1310 nm while the waveguide width is 1200 nm.

Table 2.1 shows the parameters selected for each configuration and used further in this work. The widths of 750 nm and 1200 nm for the Si and SiN waveguides respectively are chosen to get high absorption while remaining sufficiently far from the multimode regime.

Table 2.1: Extracted parameters from **Figure 2.3** for both 1310 nm and 1550 nm wavelength.

Structure	Polarization	Width (nm)	Waveguide thickness (nm)
DLG-E-SiN	TE	1200	300
DLG-SiN	TE	1200	300
DLG-Si	TM	750	220
SLG-Si	TM	750	220

Applying a voltage over the graphene layer changes its chemical potential μ_c, equivalent to shifting its Fermi level. This implies higher inter-band transition energy and therefore the absorption of the graphene layer is suppressed. Given the high carrier mobility of graphene ($\sim 10^3$ cm^2 V^{-1} s^{-1} at room temperature, taking into account the fabrication process [8],[9]) this effect is quasi instantaneous. The change in the absorption as function of voltage is illustrated in **Figure 2.5** for an Aluminum Oxide layer as a gate oxide with relative permittivity of 5 and thickness of 1nm, 3nm and 5 nm. In calculating these curves we took into account the geometrical capacitance of the stack, using the approach described e.g. in [7],[2] and V_0 which is the offset induced by the background doping n_b of the graphene with $n_b = \frac{\varepsilon_0.\varepsilon_{ox}}{d_{ox}.e}V_0$ [10], whereby we assumed that both layers are equally but oppositely doped. If this is not the case, e.g. if both layers have the same type of doping, the maximum achievable absorption will decrease, however this reduction is very small (about 10%). The curves are plotted for two values of τ_r, 65 fs and 13 fs respectively, whereby the higher τ_r is equivalent with less scattering and hence higher quality graphene. The change in τ_r has little impact on the maximum absorption but strongly affects the remaining absorption at higher voltages, with strong consequences on the insertion loss and overall figure of merit of the devices as will be discussed later. The shape of the curves is only determined by μ_c. However, the voltage needed to reach a given μ_c in the graphene layer strongly depends on the gate oxide thickness d_{Al2O3} and the graphene doping through the quantum capacitance ($= \frac{2e^2}{\hbar v f \sqrt{\pi}} \sqrt{n_b + n}$) and hence the voltage needed to reach transparency increases for the thicker gate oxides.

From **Figure 2.5**, we can now calculate the modulation efficiency defined as $(\alpha_{90\%}-\alpha_{10\%}).L/(V\alpha_{10\%}-V\alpha_{90\%})$, the insertion loss (*IL*) and extinction ratio (ER) for the different devices. The IL is determined at high forward voltage, where the absorption is quasi-minimal while the ER is calculated as the ratio of the maximum and minimum absorption, multiplied by the device length. The results are shown in **Figure 2.6** and **Figure 2.7**, as function of length of the device for $\tau_r = 65$ fs.
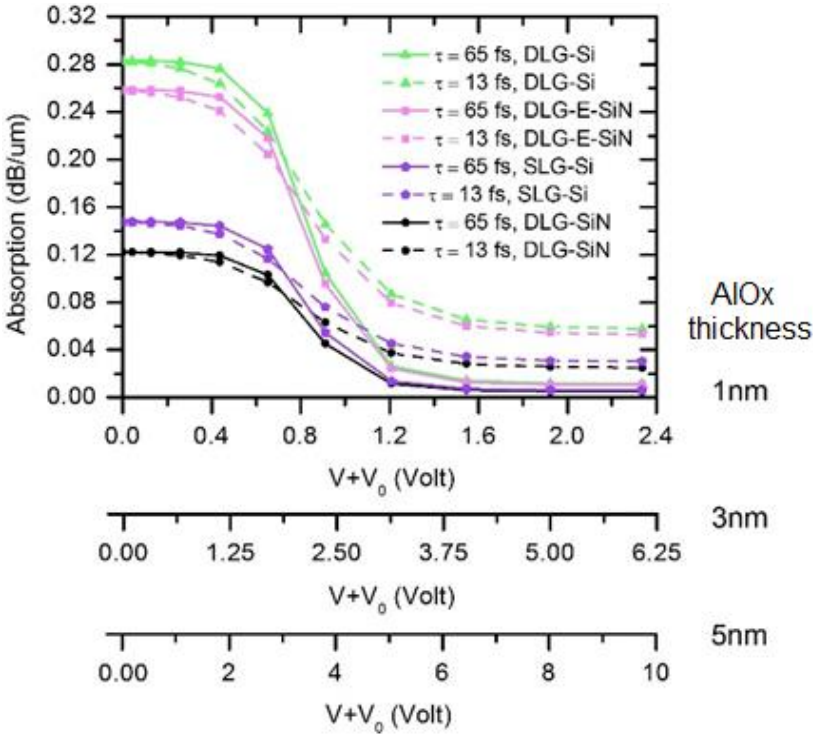
Figure 2.5: TE mode absorption in DLG-E-SiN and DLG-SiN and TM mode absorption in DLG-Si and SLG-Si as function of voltage for τ_r =65 fs and 13 fs at λ =1550 nm with $d_{Al2O3} = 1$ nm, $d_{Al2O3} = 3$ nm and $d_{Al2O3} = 5$ nm.

The modulation efficiency strongly depends on d_{Al2O3} and a 5 nm oxide reduces the modulation efficiency considerably in comparison to a 1 nm oxide [**Figure 2.6** (a),(b)]. IL and ER on the other hand, are nearly independent of d_{Al2O3} (**Figure 2.7**). Further, the modulation efficiency improves for devices that interact stronger with the graphene film (DLG-Si > DLG-E-SiN > SLG-Si > DLG-SiN). This is also true for the *ER* but the *IL* shows an opposite behavior: stronger interacting structures exhibit higher excess loss for a given length (**Figure 2.7**). In chapter 6, the fabrication and characterization of a prototype DLG-E-SiN will be discussed.
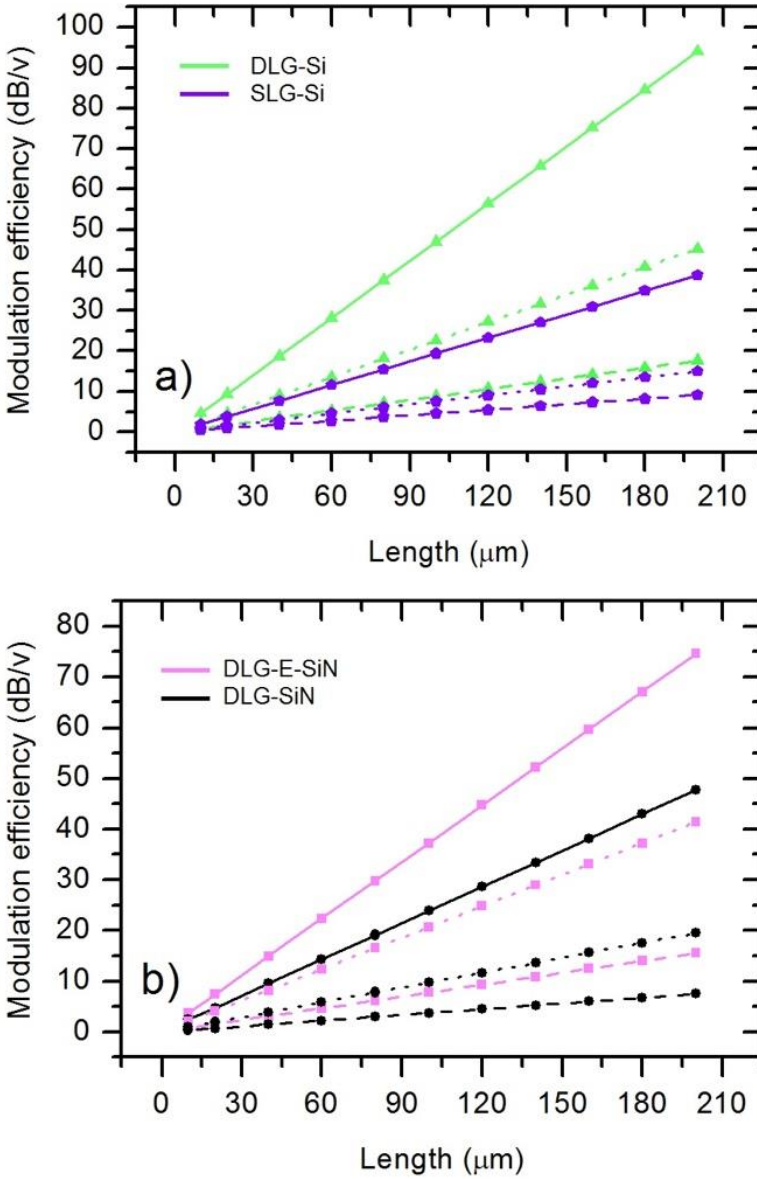
Figure 2.6: a) Modulation efficiency for DLG-Si and SLG-Si and τ_r =65 fs b) Modulation efficiency for DLG-E-SiN and DLG-SiN and τ_r =65 fs, for the oxide thickness of 1 nm, 3 nm and 5 nm.
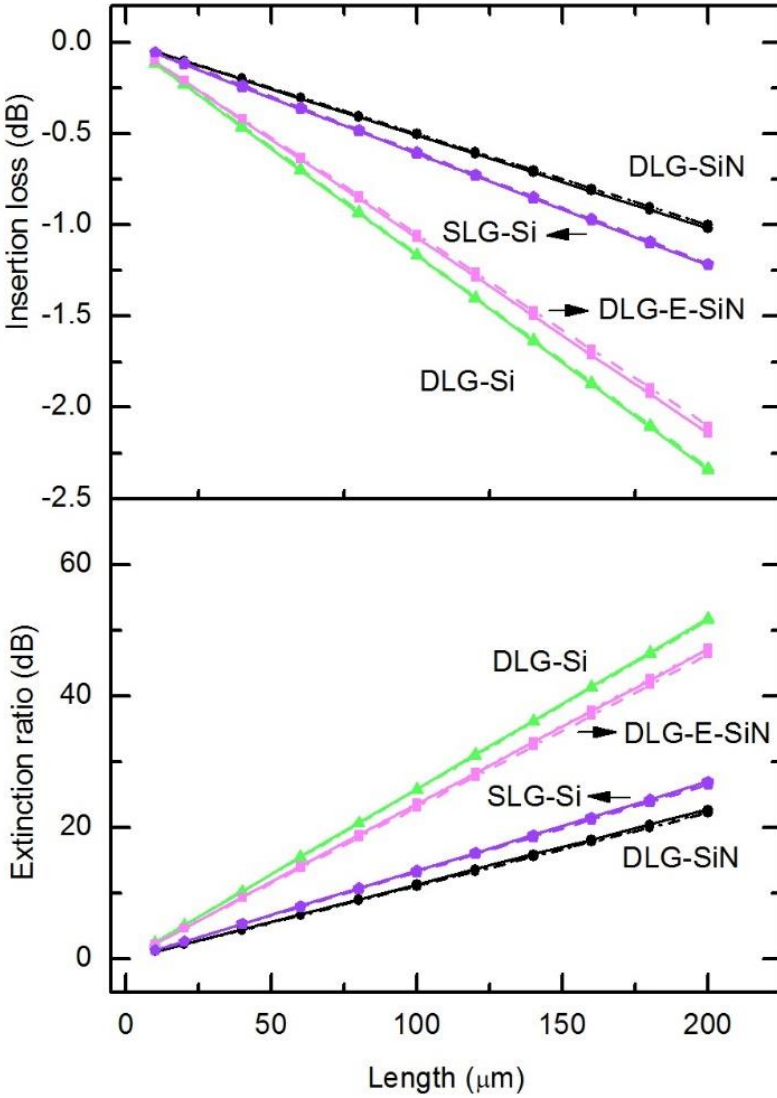
Figure 2.7: Insertion loss and extinction ratio as function of device length for $d_{Al2O3} = 1$ nm, 3 nm and 5 nm and $\tau_r = 65$ fs. The solid line belongs to oxide thickness of 1 nm, dotted to 3 nm and dashed to 5 nm.

To get more insight in this trade-off, we calculate a figure of merit often used for electro-absorption based modulators, $FOM= ER(\alpha_{V1}–\alpha_{V2})/IL(\alpha_{V2})$ as function of the applied drive voltage ΔV (with $\Delta V=V_1- V_2$) and $V_{bias} = (V_1+ V_2)/2$ chosen such that the FOM is maximized. The results are shown in **Figure**

2.8. The FOM strongly depends on d_{Al2O3}, the applied drive voltage and τ_r. Introducing lower quality graphene with shorter scattering time ($\tau_r = 13$ fs vs $\tau_r = 65$ fs) reduces the best achievable *FOM* by almost a factor of five. But, interestingly, the *FOM* is independent of the chosen device configuration. A similar conclusion was reached in a more general context in [11]. Hence, only considering the static performance of the device one should select the thinnest oxide layer technologically feasible while the detailed device configuration can be decided on other grounds, e.g. compatibility with other devices or cost. This conclusion will no longer be correct however when taking also the dynamic response into account as discussed in the next section.
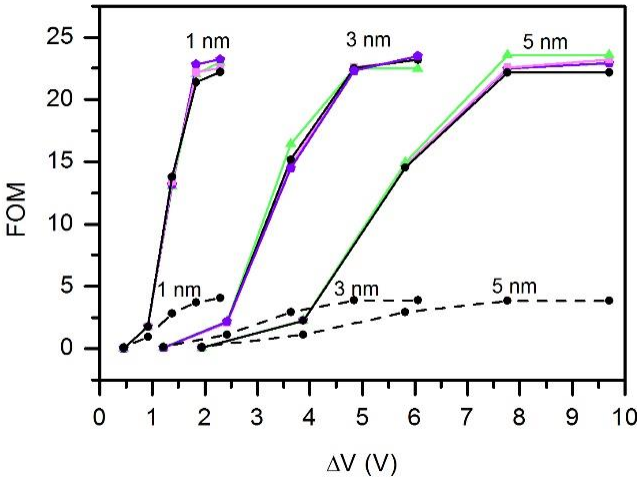
Figure 2.8: *FOM* as function of voltage difference. The solid line is for $\tau_r = 65$ fs, dashed line is for $\tau_r = 13$ fs.

Thus far we only considered the insertion loss related to the graphene layer itself. However, we also have to take into account the losses caused by the metal contacts and by the resistive part of the graphene outside of the capacitive stack (see **Figure 2.9**(a)). Here we have assumed palladium as the contact because of its low contact resistance on graphene [12]-[14]. **Figure 2.9**(b) shows the impact of the metal contacts as function of its spacing (*s*) with the waveguide, assuming, for technological reasons, that the graphene capacitive stack itself extends 300nm besides the waveguide (d_O=300nm). Extending the spacing beyond 0.75µm (DLG-Si) and 1µm (others) is sufficient to suppress the loss of the metal contacts almost completely. The remaining loss then stems from the overlap with the non-transparent graphene (absorber graphene, d_A) outside the capacitive stack. **Figure 2.9**(c) shows the

IL as function of the parameter d_O, which indicates how far the two overlapping graphene layers extend besides the waveguide.

Increasing d_O reduces the loss due to the non-transparent graphene. However, note that this also has a strong impact on the overall capacitance of the device, negatively impacting its modulation speed. Similarly increasing the metal contact spacing *s* [**Figure 2.9**(b)] increases the series resistance of the device again resulting in a reduced modulation speed. Therefore, as will be shown in the next section, in particular for high speed modulators it might be beneficial to tolerate some added *IL* and reduce both d_O and d_A to maximize the speed.
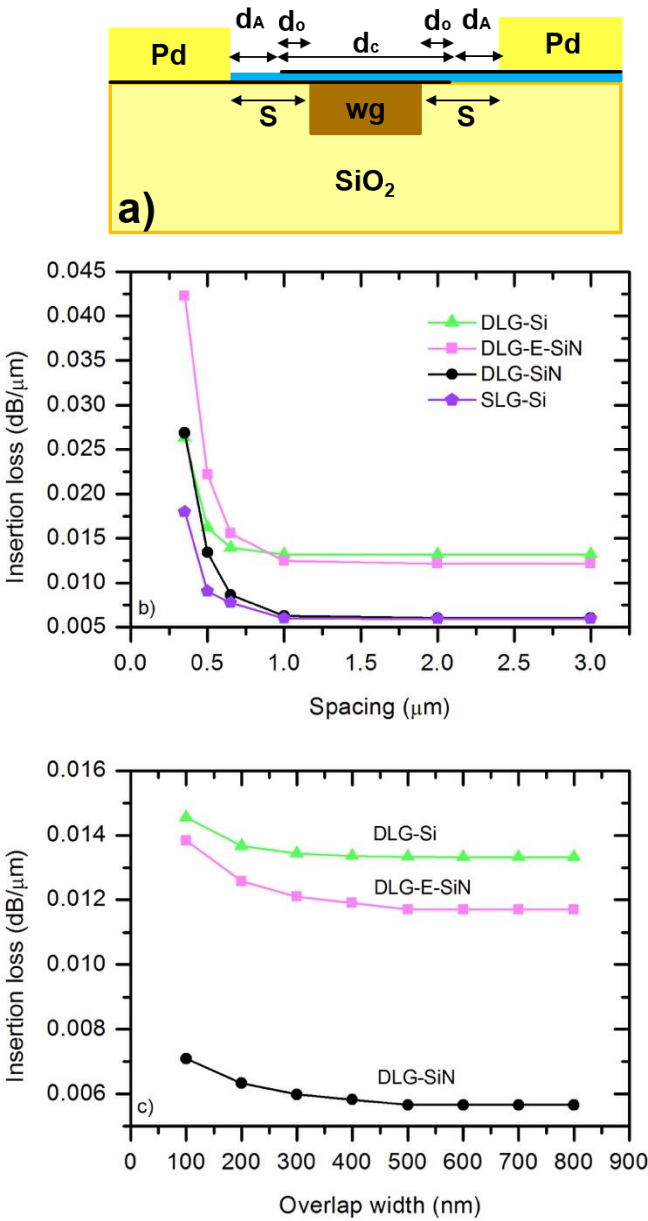
Figure 2.9: a) Schematic figure describing the parameters used in calculating the metal insertion loss b) *IL* as function of metal and waveguide spacing *s* for $d_{Al2O3} = 3$ nm with $\tau_r = 65$ fs and overlap width d_o of 300 nm c) *IL* as function of overlap width d_o for spacing of 1 µm.

All the devices discussed above operate over a wide wavelength range, inheriting the broadband modulation properties of graphene. As an example **Figure 2.10** shows the modulation curves for a DLG-SiN device (d_{Al2O3} = 3 nm, τ_r = 65 fs). Nearly wavelength independent operation is obtained from 1500 nm to 1600 nm and from 1250 nm to 1350 nm. Operating at 1310 nm results in a higher absorption as discussed above but also requires a higher drive voltage.
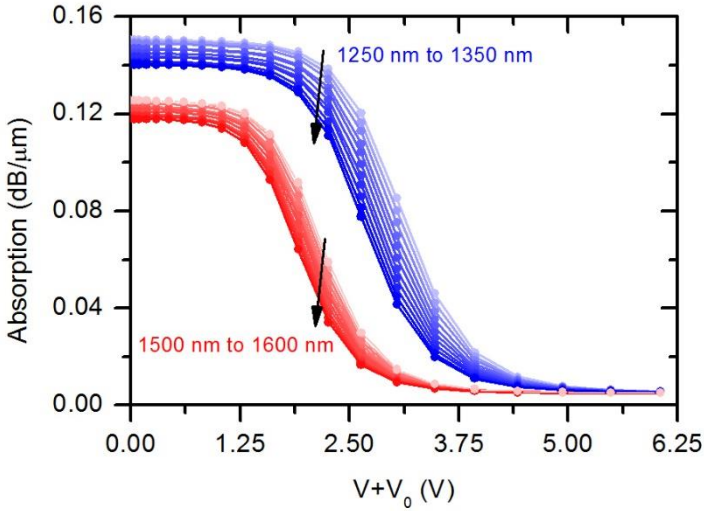
Figure 2.10: TE mode absorption of DLG-SiN as function of voltage for d_{Al2O3} = 3 nm and with the τ_r = 65 fs for the wavelength of 1500 nm to 1600 nm and 1250 nm to 1350 nm.

2.3.2 Dynamic performance

The frequency response of the DLG devices can be calculated using the electrical circuit model shown in **Figure 2.11**(a), similar to the one used in ref [15]. R_{sub} and C_{box} present the substrate resistance and buried oxide capacitance, C_{air} is the capacitance between the electrodes through the air and C_{GIG} is the capacitance of the graphene-insulator-graphene stack. The series resistance, R_s, is the sum of the contact resistance ($R_{g,c}$) and sheet resistance ($R_{g,sh}$) of the first and second graphene layer.

C_{GIG} comprises the oxide capacitance (C_{ox}) and quantum capacitance (C_q) of top and bottom graphene layers [15] where C_{ox} was calculated using a simple parallel plate approximation and C_q is dependent on the carrier density in the graphene sheets. This means C_q and hence the modulation bandwidth f_{3dB} are voltage dependent. Therefore, we calculated f_{3dB} at the bias voltage

exhibiting the highest modulation efficiency (1.6 V, 4.27 V and 6.9 V for 1 nm, 3 nm and 5 nm oxide thickness respectively). C_q was calculated assuming a background doping of $n_b = 9 \times 10^{12}$ cm^{-2} and the doping from bias voltage. The relative permittivity of Aluminum Oxide varies for different fabrication processes, hence in our calculations it is assumed to be 5 or 9. The graphene contact resistance is assumed to be $R_{g,c} = 150$ $\Omega.\mu$m, a value achievable e.g. through edge contacting of graphene [12]-[14]. The graphene sheet resistance $R_{g,sh}$ is varied between 100 Ω/sq and 300 Ω/sq, equivalent with a mobility of 6900 cm^2/V.s and 2300 cm^2/V.s, respectively, assuming the same background doping as used for the C_q calculation ($n_b = 9 \times 10^{12}$ cm^{-2}) and the spacing *s* between the waveguide edge and the metal contact edge was varied between 1 µm and 2 µm. The effect of d_O is included in the capacitance width (d_C), which comprises the waveguide width and twice the overlap region d_O. C_{air}, C_{box} and R_{sub} were taken from ref [17].

The electrical bandwidth was calculated assuming a 50 Ω source resistance [**Figure 2.11** (b),(c)]. **Figure 2.11**(b) shows how the modulation bandwidth changes as function of device length for varying oxide thickness and capacitor width (d_C). Further one notes that a smaller d_C and a thicker oxide lead to higher bandwidth. However, as discussed in the previous paragraph, these also lead to lower modulation efficiency and higher *IL*. A 200 µm long device with $d_C = 1.8$ µm, $d_{Al2O3} = 3$ nm has a bandwidth 2.5 GHz, compatible with 0.4 nanosecond switching time. Assuming a DLG-SiN configuration, and a 3 V drive voltage this device also exhibits a low *IL* (1dB) and a high *ER* (23 dB). Alternatively, a 20 µm long DLG-Si device with $d_C = 0.8$ µm and $s = 0.35$ µm, $d_{Al2O3} = 5$ nm is compatible with 16 GHz modulation (shown in **Figure 2.11**(c)) and exhibits reduced *IL* (0.25 dB) but also a reduced *ER* (5.2 dB).
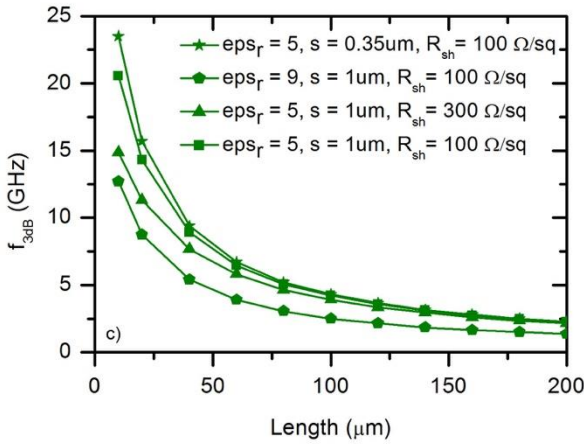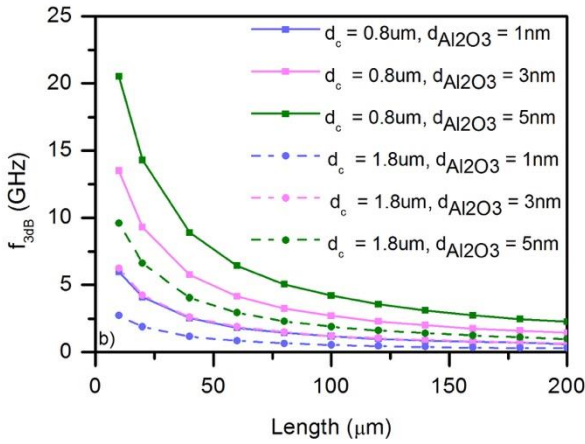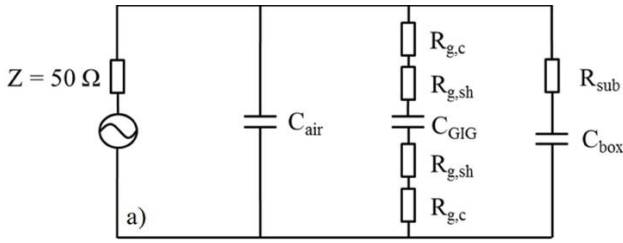
Figure 2.11: a) The equivalent electrical circuit b) Electrical 3-dB bandwidth as function of device length for $d_{Al2O3} = 1$ nm, 3 nm and 5 nm. All for $\varepsilon_r = 5$, s = 1 µm, $R_{sh} = 100$ Ω/sq c) Electrical 3-dB bandwidth as function of device length for different relative permittivity, spacing and graphene sheet resistance all for $d_C = 0.8$ µm and oxide thickness of 5 nm.

Figure 2.11(c) also shows the effect of the sheet resistance $R_{g,sh}$ and the relative permittivity of the oxide layer. Obviously a lower sheet resistance and reduced spacing s are beneficial for the performance of the device. Increasing the relative permittivity of the oxide layer on the other hand is equivalent to decreasing its speed.

2.4 Slot-waveguide structure

The configurations proposed in the previous section or demonstrated in the earlier works are high performance devices. However, in most of the investigated graphene-on-Si waveguide based devices, the quasi-TM mode has the highest interaction with the graphene layer [5]-[7],[18] while the quasi-TE mode is the most common polarization for the guiding mode in other optical devices. Hence, graphene-on-Si based devices that are operating with the TM-like mode lead to a complicated design when integration with other optical components is desired.

In this section, we propose a double-layer graphene-on-Si slot waveguide based optical modulator [19]. Our simulation results show that the TE mode interacts more strongly with graphene in the slot waveguide compared to standard waveguides, which addresses the difficulty of integration with other optical devices. This solves the issue of poor extinction ratio in previous graphene-based devices operating with the TE-mode.

In the next section, we investigate the effect of the waveguide width, capacitor width, polarization, metal pads distance from the waveguide and finally graphene quality on the absorption of the graphene-on-slot modulator. The most important results are compared with Si strip waveguides with double-layer graphene on top (DLG-Si).

The presented structure is a Si slot waveguide with a graphene-dielectric-graphene stack on top. A voltage can be applied through metal contacts on both graphene layers (**Figure 2.12**). The results presented here are for an operating wavelength of 1550 nm and a temperature of 300 K. **Figure 2.13**(a) shows the absorption of the TE mode versus width of the slot waveguide with a double-layer graphene on top. In this design the width of the slot section is fixed to a constant value of 120 nm and the width of the Si is varied. A maximum absorption of 0.27dB/µm is found for a waveguide width of 620 nm. **Figure 2.13**(a) also depicts that the absorption of the TE mode of the DLG-Si-Slot waveguide is much higher than that for the DLG-Si strip waveguide, which is due to the high interaction of the mode with the graphene layers for the slot configuration.

To assess the effect of graphene quality on the absorption, we simulated the graphene loss for two different types of graphene as function of the applied voltage. It is shown in **Figure 2.13**(b), that the high quality graphene has a smaller insertion loss (the smallest absorption for a given voltage) and thus a higher extinction ratio. According to this graph, a remarkably high extinction ratio of 23 dB can be reached with only 1dB insertion loss for a device with

100 µm length. These parameters can be improved linearly for the longer devices.
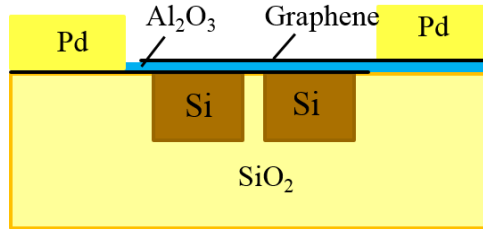
Figure 2.12: Schematic of the double-layer graphene-on-Si slot waveguide.
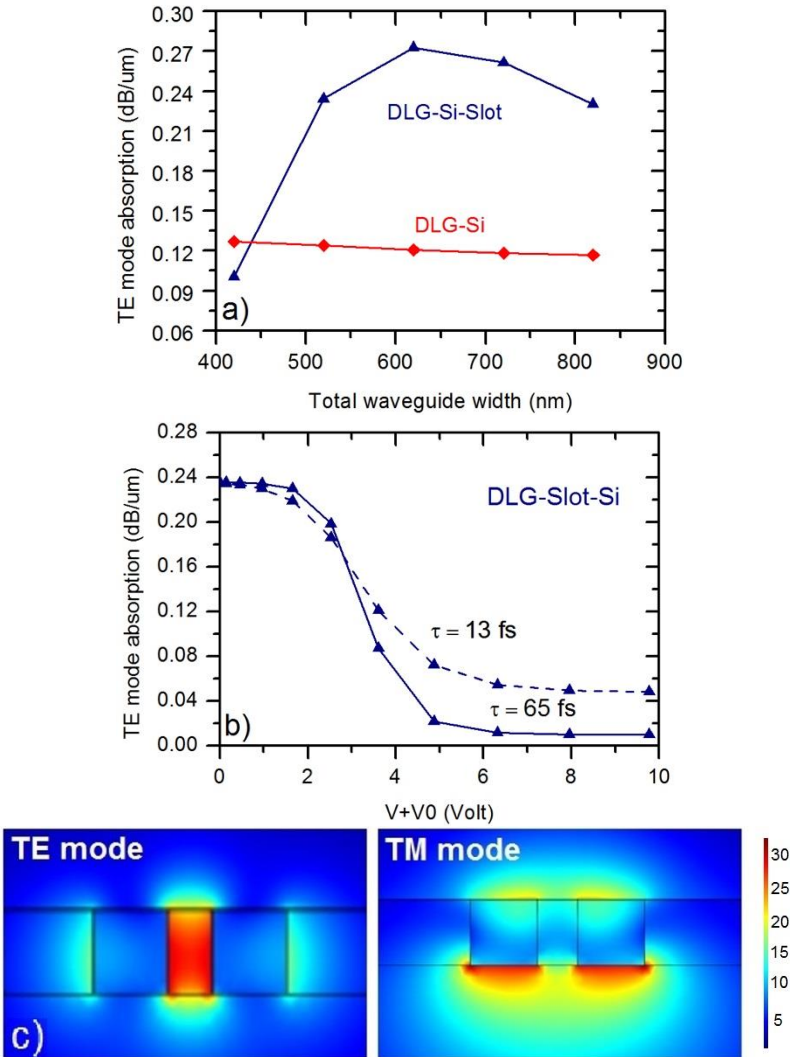
Figure 2.13: a) The TE mode absorption of DLG-Si and DLG-Slot-Si at the Dirac point versus the total waveguide width (in DLG-Slot-Si total waveguide width = 2×Si section width + slot section width), the graphene scattering time is 65 fs b) The TE mode absorption for the scattering time of 65 and 13 fs. Si section width= 200 nm, slot section width = 120 nm, thus the total waveguide width is 520 nm. c) TE and TM mode profile in DLG-Slot-Si.

The capacitor width is another important parameter in the device absorption. The loss (i.e. interaction between light and graphene layer) increases by widening the width of capacitor. For widths more than 1 µm the

increase saturates [**Figure 2.14**(a)]. The minimum point is a configuration where graphene layers are just covering the slot and interestingly the absorption is still a notable value of 0.16 dB/µm. Therefore, for a device with a length of 100 µm the extinction ratio can be 16 dB, a quite large value. The advantage of such a structure is that it considerably decreases the capacitance and hence improves the bandwidth of the device.

For the real device we also have to consider the extra loss due to the metal pads and the resistive part of the graphene. To evaluate this effect **Figure 2.14**(b) plots the influence of the distance between the metal and the waveguide. It is seen that insertion loss originating from the metal pads is suppressed by enlarging the distance between metal and the waveguide over 1 µm. The remaining loss is due to the resistive graphene, which is absorbing. Since the two configurations, the DLG-Si strip and the DLG-Si-Slot, have almost the same length of resistive graphene, their insertion loss evolves to the same value in **Figure 2.14**(b).

The mode profiles for the structures exhibiting maximum and minimum insertion loss for the DLG-Si-Slot waveguide are also shown in **Figure 2.14**(b). These show clearly that the mode tends to confine in the metal area if these pads are close to the waveguide (spacing = 0.35 µm). On the other hand, the mode only exists in the waveguide-graphene section with no leakage towards the metal pads for the low insertion loss state (3 µm spacing).
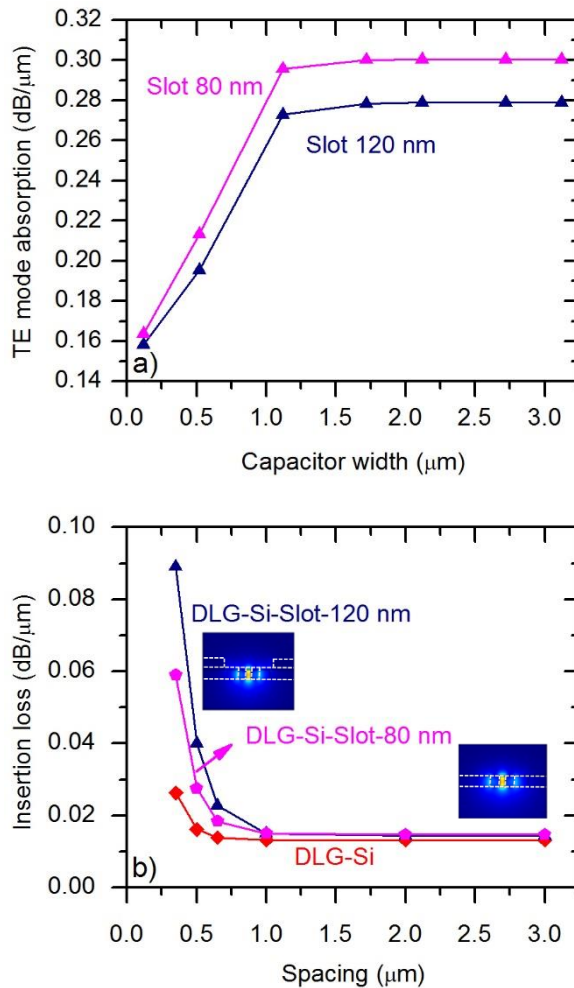
Figure 2.14: a) The TE mode absorption at the Dirac point for the scattering time of 65 fs as function of capacitor width b) The insertion loss as function of the distance of metal edge and the waveguide edge (spacing). In the case of DLG-Si-Slot, the simulation was performed for the slot section width of 80 nm and 120 nm.

Since, a short capacitor width is achievable in this design an improved dynamic performance and a modulation speed of 23 GHz is predicted for a 20 μm device length. In this calculation, we assumed $R_s = 100$ Ω/sq, s = 0.35 μm, $eps_r = 5$, ox thickness = 5nm, $d_c = 520$ nm.

2.5 Graphene saturable absorber for hybrid integration with semiconductor lasers

A typical hybrid III-V on Si laser consists of an optical cavity formed in the silicon layer and a gain section consisting of III-V materials within the cavity. They also contain a taper section where the light is adiabatically coupled from the III-V gain section to the silicon waveguide [20],[21]. Often, there are many modes of the optical cavity falling within the gain band. The total output of such a laser as function of time depends on the amplitude, frequency and relative phase of these oscillating modes. If the oscillating modes are forced to maintain equal frequency spacing with a fixed phase relationship to each other, the output as function of time will vary in a well-defined manner. The laser is then said to be mode-locked or phase-locked. The result is a train of short intense pulses with a repetition rate corresponding to the cavity round trip time. For many applications such as THz generation a high repetition rate mode-locking is a desire.

Passive mode locking is obtained by inserting a saturable absorber (SA) into the laser cavity. A SA is a medium whose absorption coefficient decreases as the intensity of light passing through it increases. Thus, it transmits intense pulses with relatively little absorption and absorbs weak ones.

In [20] a mode-locked laser (MLL) with a III-V SA was demonstrated. However, III-V SA have some drawbacks such as their limited optical bandwidth. It is believed that a graphene SA might overcome these limitations exploiting its broadband and high speed operation. Here, we investigate how a graphene SA can be efficiently integrated on the standard III-V silicon platform. Standard III-V lasers operate with the TE polarization and in the previous sections we observed that the TE polarization has a lower interaction with graphene compared to the TM mode. This will be even weaker, if graphene is integrated on the 400 nm Si waveguide used in the hybrid III-V silicon platform. Therefore, the design should be optimized to enhance the TE-mode interaction with graphene. We propose to embed the graphene layer in the taper section of the laser where the mode has high confinement in the middle.

Figure 2.15 shows the top view and cross section of our structure. The InP epitaxial layers are chosen similar to that of a standard heterogeneously integrated laser design [21]. A single layer of graphene is included on the 400 nm Si rib waveguide. The InP mesa is bonded on top of the graphene layer with an insulating adhesive layer of DVS-BCB in between. The BCB layer

has two roles in our design. First, it serves as the adhesive bonding layer between the III-V and the Si chips. Second, it acts as a dielectric layer for the switch. Applying a voltage between the metal contact on the graphene and the doped bottom InP cladding layer of the laser allows controlling the chemical potential and hence the transparency of the graphene layer [5]-[7],[18]. In **Figure 2.16**, the TE mode absorption is plotted as function of the InP mesa width and Si waveguide width as they vary along the taper. It shows that the absorption level changes drastically along the taper length and can be controlled by varying the respective waveguide widths. The graph also compares the absorption in the modulator with that of a layer of graphene directly deposited on the 400 nm silicon waveguide. In the latter design, the Si waveguide has to be doped in order to apply a voltage over the graphene layer. This increases the complexity of the process and as the graph shows also has considerably lower performance. According to **Figure 2.16**, the TE mode absorption in the taper design is almost 4 times higher than for the standard device. The total absorption for a taper length of 150 µm is about 6 dB in the Dirac point of graphene, sufficient for datacom applications. The figure also shows the effect of the bonding layer thickness. A thicker BCB-layer, pushes the mode toward the Si waveguide and reduces its interaction with the graphene. Thinner bonding thickness not only increases the absorption (and hence the modulation efficiency) but also is beneficial to boost the coupling from the III-V mesa to the Si waveguide and enhance the laser performance [21]. **Figure 2.17** shows how the optical mode evolves in three cross sections along the taper length.
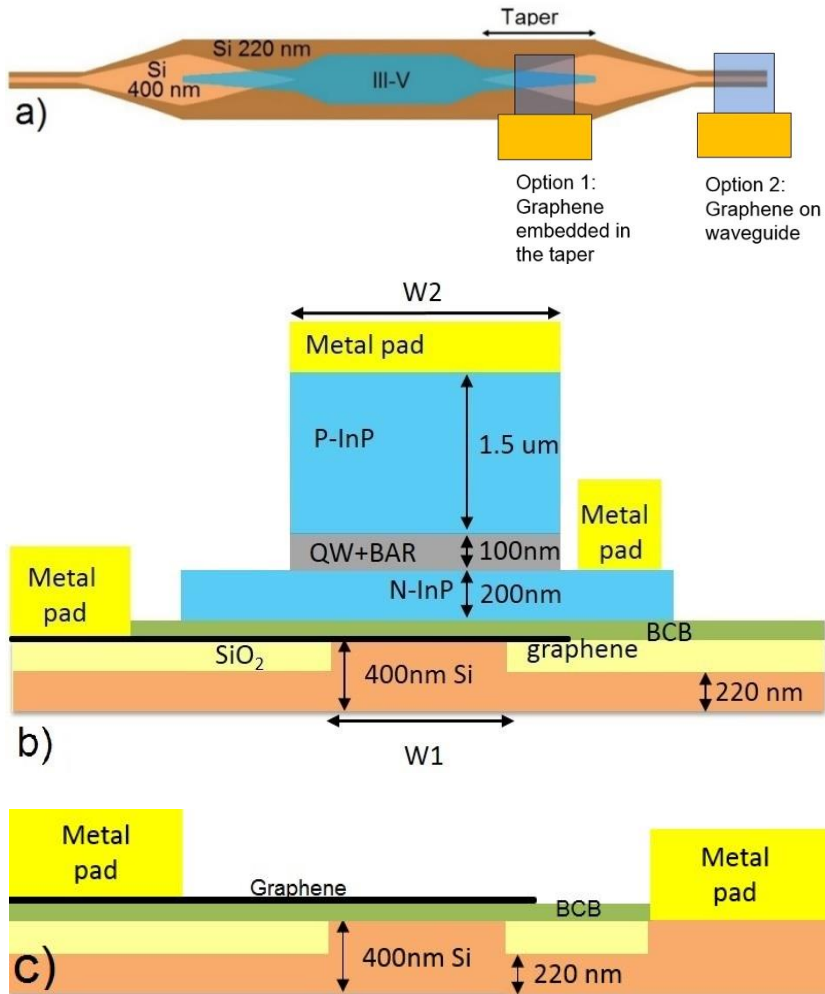
Figure 2.15: a) III-V on Si laser design, top view, b) Schematic of the graphene device integrated with an InP/Si laser. The structure in the option 1 in the image (a) is embedded in the taper section, therefore the width of Si waveguide and P-InP is varied c) The cross section of the graphene in the option 2 in the image (a).
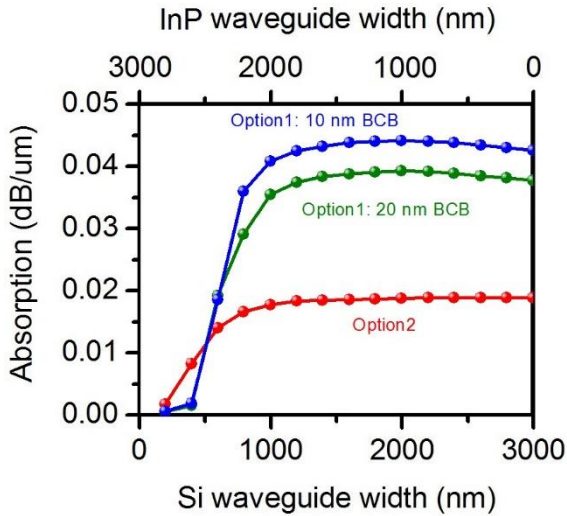
Figure 2.16: The TE mode absorption as function of the InP taper width and Si waveguide width for a design with the graphene embedded in the taper section (blue, green) and a design whereby the graphene is integrated on a standard waveguide, outside the taper region.
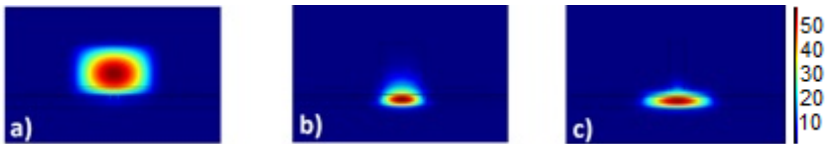
Figure 2.17: Three cross sections from the taper with a) P-InP width 3000nm, Si width 200 nm b) P-InP width 1600nm, Si width 1600 nm c) P-InP width 600nm, Si width 2600 nm.

2.6 Conclusion

In summary, we investigated the performance of four representative configurations, relying either on Silicon or on Silicon Nitride waveguides, for realizing graphene-based switches and modulators operating in the wavelength regions around 1310 nm and 1550 nm. We first studied their properties at static operating conditions, which might actually also be relevant for other types of devices such as detectors. Interestingly we found that the figure-of-merit of these devices, defined as the ratio of the extinction ratio over the insertion loss, is independent of the precise waveguide configuration and only depends on the quality of the used graphene and the gate-oxide thickness. Hence the waveguide configuration can be selected based on other

criteria. For ultimate speed, the high confinement offered by higher index contrast silicon waveguides offers more compact and hence faster devices. For switches, which have less stringent requirements on operating speed, deposited silicon nitride waveguides can provide more versatility and do not suffer from two photon absorption. In all applications accurately controlling the gate-oxide thickness is extremely important as it directly impacts modulation efficiency, power consumption and operation bandwidth.

In addition, we investigated the performance of an optical graphene modulator based on a Si slot waveguide. The proposed structure has absorption of 0.27 dB/µm at the Dirac point for the optimum geometry, a high value compared to that for a standard TE strip waveguide. For the high quality graphene with scattering time of 65 fs and total waveguide width of 520 nm, a 100 µm long device can provide an extinction ratio of above 23 dB. Since the device has high absorption characteristics for a small capacitor width it improves the speed of the device considerably. The metal contacts should be at least 1 µm away from the mode confined region to avoid the extra insertion loss. The device operates with the TE polarization, which enables to integrate this type of switch with other optical components.

In the last section of this chapter, we proposed a design for the hybrid integration of graphene saturable absorber with III-V on Si laser.

References

[1] L. Abdollahi Shiramin, and D. Van Thourhout, "Graphene Modulators and Switches Integrated on Silicon and Silicon Nitride Waveguide," JSTQE, vol. 23, 2017.

[2] G. W. Hanson, "Dyadic Green's functions and guided surface waves for a surface conductivity model of graphene," J. Appl. Phys., vol. 103, 2008.

[3] Y.-C. Chang, C.-H. Liu, C.-H. Liu, Z. Zhong, and T. B. Norris, "Extracting the complex optical conductivity of mono- and bilayer Graphene by ellipsometry," Appl. Phys. Lett. vol. 104, 261909, 2014.

[4] Y. W. Tan, Y. Zhang, K. Bolotin, Y. Zhao, S. Adam, E. H. Hwang, S. Das Sarma, H. L. Stormer, and P. Kim, "Measurement of scattering rate and minimum conductivity in Graphene," Phys. Rev. Lett. vol. 99, 246803, 2007.

[5] M. Liu , X. Yin, E. U.Avila, B. Geng, T. Zentgraf, L. Ju, F. Wang, and X. Zhang., "A graphene-based broadband optical modulator," Nature., vol. 474, no. 7349, pp. 64-67, 2011.

[6] M. Liu, X. Yin, and X. Zhang., "Double-layer graphene optical modulator," Nano lett, vol. 12, no.3, pp. 1482-1485, 2012.

[7] Y. Hu, M. Pantouvaki, J. Van Campenhout, S. Brems, I. Asselberghs, C. Huyghebaert, P. Absil, and D. Van Thourhout., "Broadband 10 Gb/s operation of graphene electro-absorption modulator on silicon," Laser Photonics Rev., pp. 1-10, 2016.

[8] J. W. Suk, A. Kitt, C. W. Magnuson, Y. F. Hao, S. Ahmed, J. H. An, A. K. Swan, B. B. Goldberg, and R. S. Ruoff., "Transfer of CVD-Grown Monolayer Graphene onto Arbitrary Substrates," ACS Nano., vol. 5, pp. 6916–6924, 2011.

[9] Y. D. Kim, M.-H. Bae, J.-T. Seo, Y. S. Kim, H. Kim, J. H. Lee, J. R. Ahn, S. Lee, S.-H. Chun, and Y. D. Park, "Focused-Laser- Enabled p-n Junctions in Graphene Field-Effect Transistors," ACS Nano., vol. 7, pp. 5850–5857, 2013.

[10] J. Gosciniak and D.T. Tan, "Theoretical investigation of graphene-based photonic modulators," Scientific reports, Vol. 3, 2013.

[11] M. Tamagnone, A. Fallahi, JR. Mosig, and J. Perruisseau-Carrier., "Fundamental limits and near-optimal design of graphene modulators and non-reciprocal devices", Nature.Photon.,vol. 8, 556, 2014.

[12] J. T. Smith, A. D. Franklin, and D. B. Farmer, C. D. Dimitrakopoulos, "Reducing Contact Resistance in Graphene Devices through Contact Area Patterning," ACS Nano., vol. 7, pp. 3661 –3667, 2013.

[13] F. Xia, V. Perebeinos, Y. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal–graphene junction resistance," Nature Nanotech., vol. 6, pp. 179–184, 2011.

[14] H. Zhong, Z. Zhang, B. Chen, H. Xu, D. Yu, L. Huang, and L M. Peng., "Realization of low contact resistance close to theoretical limit in graphene transistors", Nano Res., vol. 8, pp. 1–11, 2015.

[15] V. Sorianello, M. Midrio, and M. Romagnoli, "Design optimization of single and double layer Graphene phase modulators in SOI," Opt.Exp., Vol. 23, no.5, pp. 6478-6490, 2015.

[16] S. J. Koester and M. Li., "High-speed waveguide-coupled graphene-on-graphene optical modulators", Appl. Phys. Lett., vol. 100, no. 17,171107-171107-4, 2012.

[17] Y. Hu, X. Xiao, H. Xu, X. Li, K. Xiong, Z. Li, T. Chu, Y. Yu, and J. Yu., "High-speed silicon modulator based on cascaded microring resonators", Opt exp., vol. 20, no. 14, pp. 15079-15085, 2012.

[18] H. Dalir, Y. Xia, Y. Wang, and X. Zhang, "Athermal Broadband Graphene Optical Modulator with 35 GHz Speed," ACS Photonics, 2016.

[19] L. Abdollahi Shiramin, and D. Van Thourhout, "Graphene devices for outperformed optical interconnects", IEEE Photonics Society Benelux, 2017.

[20] S. Keyvaninia, S. Uvin, M. Tassaert, Z. Wang, X. Fu, S. Latkowski, L. Thomassen, and G. Roelkens, "III-V-on-silicon anti-colliding pulse-type mode-locked laser", Opt. Lett. 40, 3057–3060, 2015.

[21] A. Abbasi, J. Verbist, X. Yin, F. Lelarge, G. H. Duan, J. Bauwelinck, G. Roelkens and G. Morthier, "Enhanced Modulation Bandwidth of Heterogeneously Integrated III-V-on-silicon DFB Laser for 40 Gb/s NRZ-OOK Direct Modulation", International Semiconductor Laser Conference (ISLC), Japan, 2016.

3

Graphene process development

Contents

In this chapter, we will discuss the development of the processes to pattern graphene and the fabrication of transmission line measurement (TLM) structures. Fabrication of TLMs is a basic example to learn the tricky graphene processing. The developed process steps discussed in this chapter will be used in the next chapters for realizing more complex devices. Also, here we investigate graphene's properties such as sheet resistance and contact resistance for different contacting schemes. All processes in this

chapter have been carried out starting from graphene transferred on a SiO$_2$/Si substrate by Graphenea [1].

3.1 Process steps for fabrication of TLM devices

The TLM measurement is a two probe measurement technique to determine the resistance of ohmic contacts. The structure consists of several metal pads on a graphene stripe whereby the distance between the individual metal pads gradually increases. The resistance between each two contacts is measured and plotted as function of the contact's distance. The schematic of such TLM structure is shown in **Figure 3.1**.
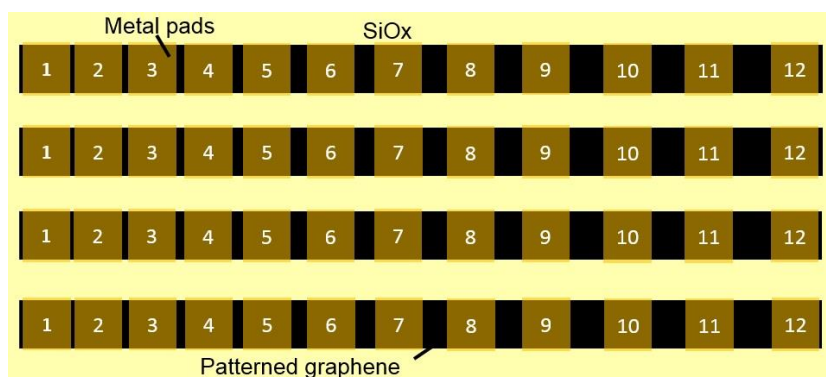
Figure 3.1: TLM design on the graphene stripes.

To start the process, first a 1 cm × 1 cm sample is cleaved from a SiO$_2$/Si wafer with graphene on top. Since this layer of graphene was transferred on a blank substrate, some alignment markers are defined for use in the next steps. After marker definition, the graphene layer is patterned using optical lithography and a reactive ion etching (RIE) process. This step is the most critical one as graphene is very sensitive to chemicals. Following patterning, a second optical lithography is carried out to define metal pad openings in a resist layer. The metal is deposited using evaporation. After lift-off the sample is ready for characterization. In the following sections we describe each process step in detail, and discuss the associated issues and solutions.

3.1.1 Marker definition

On the graphene substrate, a gold (Au) layer has a high contrast and a few tens of nm of Au is clearly visible in the mask aligner. The standard way to create markers is to use an image reversal resist for the optical lithography and deposit a metal film immediately after the development step. The AZ-5214 photoresist is a proper resist with a sub-micron resolution. Note that for the

graphene-based processes increasing the resist adhesion to graphene is not a desire. Remaining resist residuals as a result of using an adhesion promoter can deteriorate graphene's properties. Hence, the use of Ti prime, the standard adhesion promoter for the AZ-5214 photoresist, should be avoided.

3.1.2 Graphene patterning using bilayer resist process

The standard way for defining a pattern using optical lithography is to use a positive resist, which is directly developed after exposure. However, for the graphene patterning this conventional method is not practical and it leads to the graphene detachment from its substrate as seen in **Figure 3.2**. In this figure, two samples after developing and rinsing with DI water are shown. Following several tests, I concluded it is important to keep graphene away from both the aqueous developer and DI water.
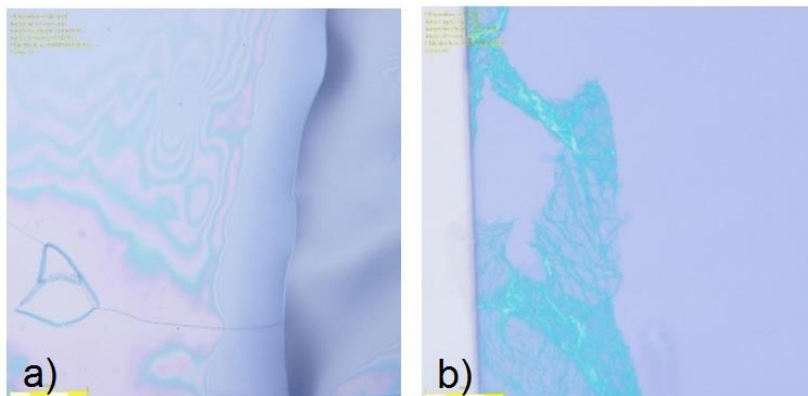
Figure 3.2: Graphene delaminated from the SiO_2 substrate. a) Developer and DI water have penetrated below graphene b) Graphene has been removed from the right side of the image. Cyan color shows the damaged graphene, violet is SiO_2 where graphene is completely gone.

To solve this issue, we developed a bilayer resist process, which effectively protects graphene during development. Such an approach is typically used for substrates with a large topography or for substrates which are highly reflective [2]. In this method, two different photoresists are spin coated on the sample and the first coated photoresist acts as a protection layer. To avoid dissolving the protective resist, two resists with a sufficiently different development rate should be chosen. The first coated resist should have a slower development rate compared to the second resist to be used as a protection layer. In our process, we used AZ-MIR-701 (the thinnest resist

available in the lab) and AZ-5214 as the first and second layer respectively. The procedure is described in **Figure 3.3**. First the AZ-MIR-701 resist is coated on the graphene substrate (graphene/300 SiO$_2$/Si). A layer of AZ-5214 resist is then coated on the AZ-MIR-701. Subsequently, illumination and development are carried out to pattern the AZ-5214 layer. Since the development rate in the AZ-400K developer of AZ-MIR-701 is much slower than that of AZ-5214, after patterning of the AZ-5214, the protection resist remains almost untouched. The final step is to etch the graphene layer using an O$_2$ plasma with a pressure of 100 mTorr, 75 Watt RF power and 50 sccm O$_2$ flow. As we have the protection layer of AZ-MIR-701 on the graphene layer, the sample should be exposed to the O$_2$ plasma to first etch AZ-MIR-701 and then graphene. After O$_2$ plasma etching, the sample is cleaned with acetone to remove the resist and obtain a patterned graphene.
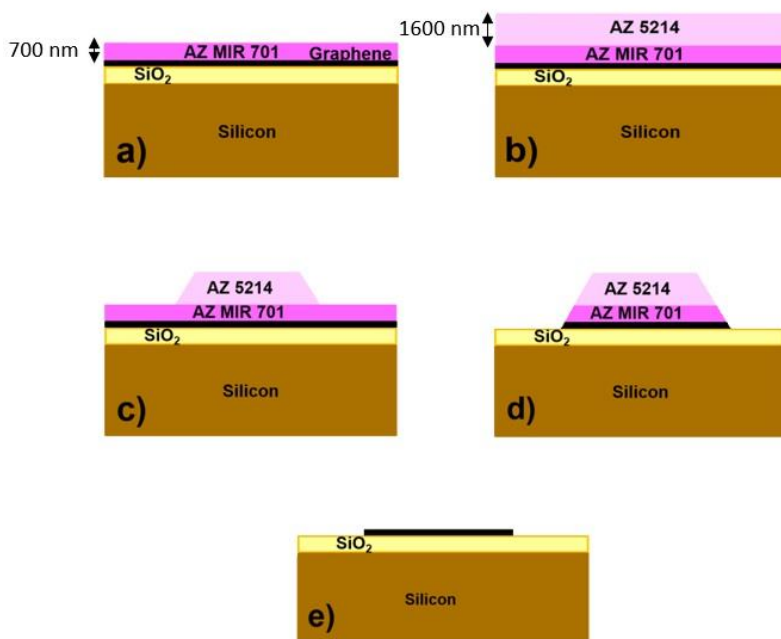
Figure 3.3: Bilayer resist for the graphene patterning a) AZ-MIR-701 is coated on the graphene/SiO$_2$/Si b) AZ-5214 is coated on the AZ-MIR-701/graphene/SiO$_2$/Si c) Illumination and developing of the AZ-5214 d) Etching the AZ-MIR-701 resist together with the graphene layer e) Removing the unexposed resist with acetone.

Figure 3.4 shows a graphene layer successfully patterned using the above explained process flow. The size of the graphene patterns is $100 \times 1200 \ \mu m^2$.
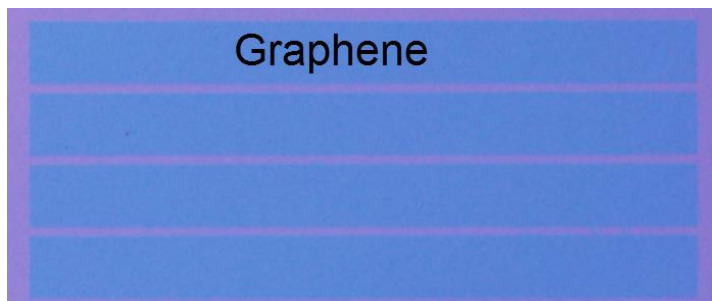
Figure 3.4: Graphene sample patterned with the bilayer resist process. The blue area is graphene and the violet color indicates the SiO_2 substrate.

3.1.3 Metallization on the patterned graphene

To fabricate the metal contacts on the patterned graphene, an image reversal resist (using contact lithography and a single layer resist) can be used and a metal layer (Pd or Cr) is then deposited. After lift-off the sample is ready for measurement.

3.2 Contact resistance on the graphene stripes

To achieve high speed graphene-based electro-optical components, the realization of low contact resistance on graphene is of paramount importance. Several research groups have already investigated different techniques to reduce the contact resistance. Most proposed methods are either based on the introduction of defects in the overlapping region of the graphene and metal or based on the use of different metals as a contact. **Figure 3.5** expresses the contact resistance values obtained for the CVD graphene in recent years. According to this figure, the best value of the contact resistance is 84 $\Omega.\mu m$. In this work defects are created on the graphene layer underneath the metal pad by an energetic electron beam before the metal deposition. This approach increases the number of transport channels between the metal and graphene considerably.
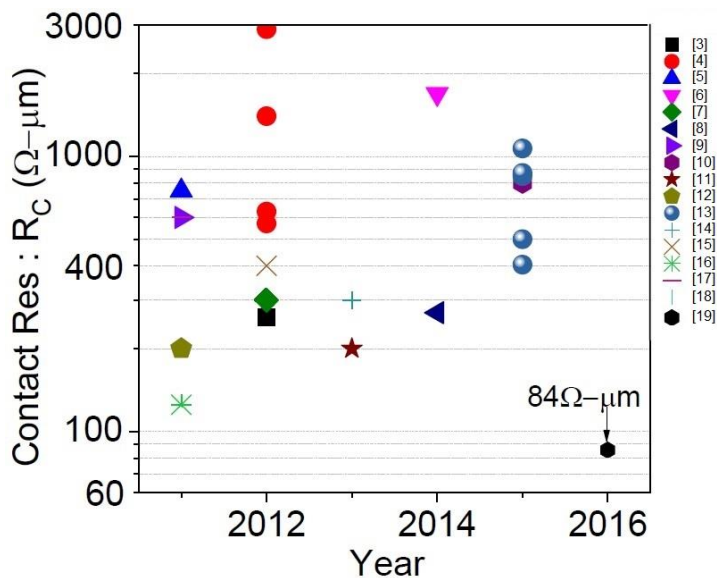
Figure 3.5: Graphene contact resistance from 2011 to 2016 reported by different research groups (modified figure from [19]).

Figure 3.6 is another review showing the reported contact resistance versus the graphene sheet resistance. As can be seen, there is a large scattering in the R_c and R_{sh} values in both **Figure 3.5** and **Figure 3.6**. The main reason for this data scatter is believed to be the invasive fabrication process steps which alter graphene's properties.
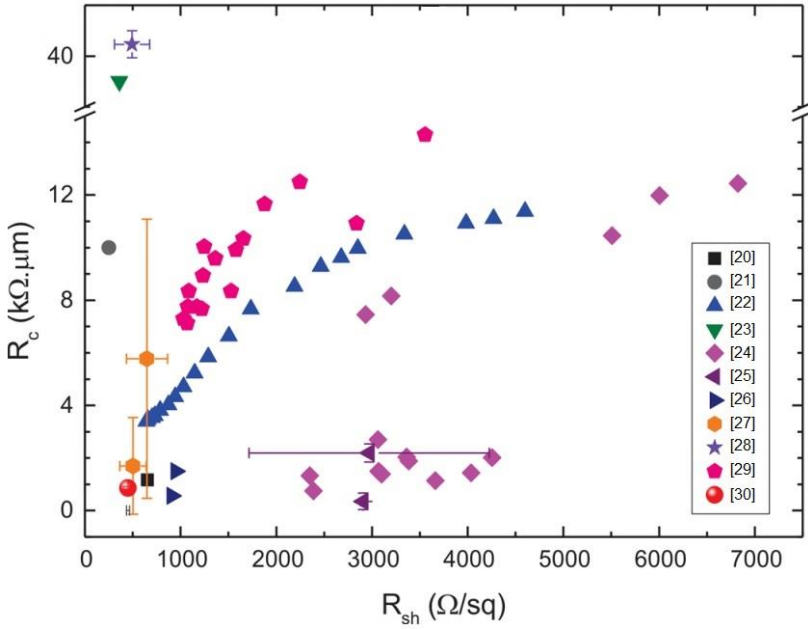
Figure 3.6: Overview of the reported R_c values versus R_{sh} for devices based on CVD graphene transferred onto silicon wafer with a SiO_2 layer on top (figure from [30]).

In our experiment, the fabricated TLM structures (as explained in previous sections) with Pd metal pads on one sample and with a Cr/Au/Ti/Au stack on another sample are used to evaluate graphene's properties. **Figure 3.7** shows the total resistance versus the metal spacing in the TLM structures for the samples with Pd and Cr metal pads. The contact resistance and the sheet resistance are then extracted from these figures and summarized in **Figure 3.8**. This figure shows a low contact resistance for Pd (400-900 $\Omega.\mu m$) compared to the Cr stack (1100-2100 $\Omega.\mu m$). The low contact resistance of pd compared to Cr is discussed in [31]. The sheet resistance of graphene varies from 330 to 460 $\Omega/\square$ for both samples. These results are comparable to some of the reported results (**Figure 3.5** and **Figure 3.6**), but there is room for improvement to reach to the state-of-the-art values, below 100 $\Omega.\mu m$.
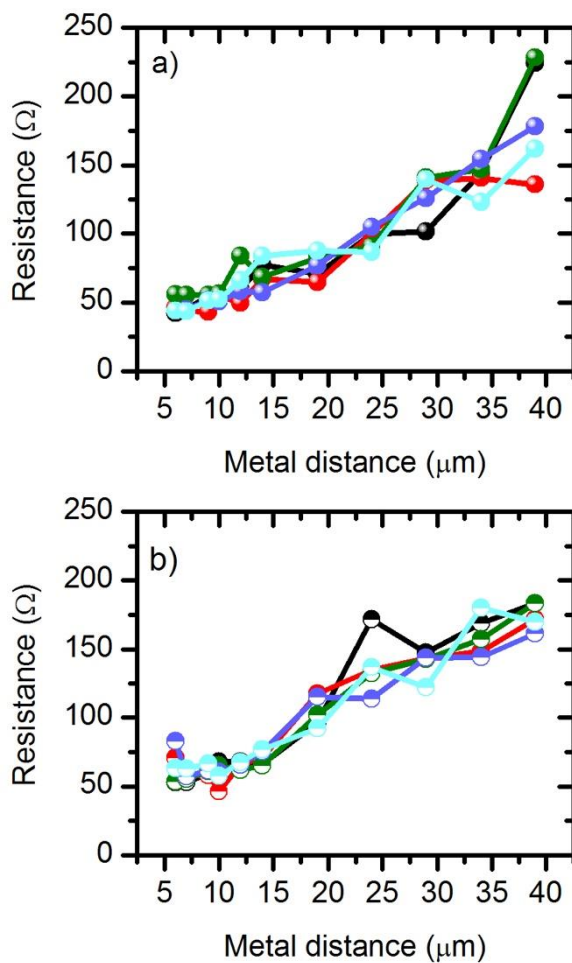
Figure 3.7: Resistance versus the contact's distance. a) for the sample with the Pd pads, b) for the sample with the Cr stack. Each color presents a separate location and separate TLM structure on the sample.
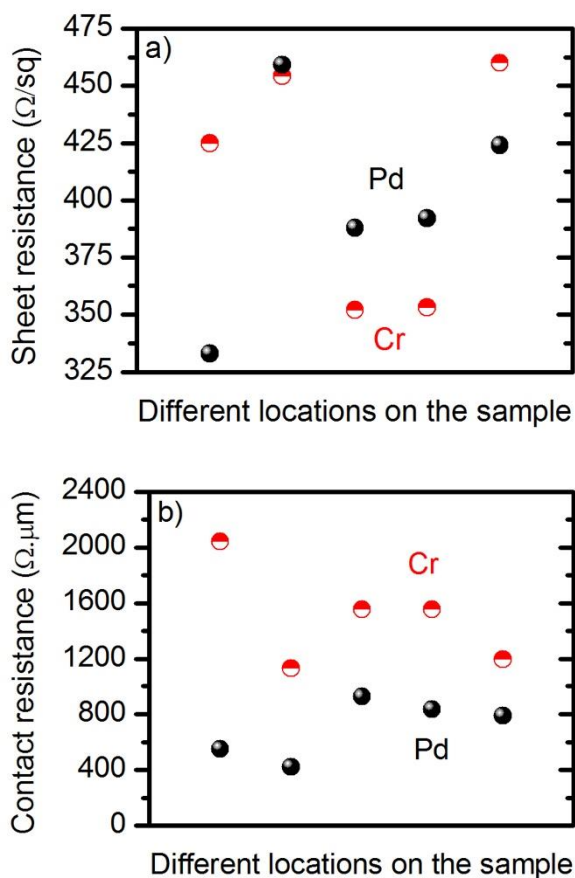
Figure 3.8: Comparison of the graphene sheet resistance a) and contact resistance b) for two samples with the palladium (black, filled circle) and chromium (red, half-filled circle) pads.

3.3 Contact resistance on the discrete graphene patterns

In this section, similar TLM measurements as carried out in the previous section will be presented. The difference is that the graphene patterns underneath the metal pads are isolated from each other as is shown in **Figure 3.9**. The importance of this design relies in the fact that in this thesis we will transfer micron-size graphene patterns (chapter 4). Hence, the TLM design with the discrete graphene patterns discussed in this section is an evaluation of the micron-size graphene contacting.
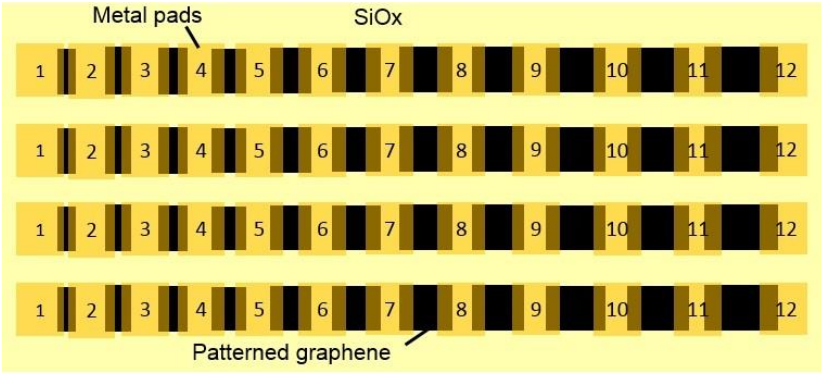
Figure 3.9: Schematic of TLM devices with the discrete graphene patterns.

Figure 3.10 shows the total resistance versus the metal spacing with the Pd contacts for 3 sets of the TLM structures. As is seen, the data is widely scattered and does not follow a linear trend. The contact resistance and sheet resistance are of the order of 5 kΩ.µm and 1000 Ω/□. This is explained as follows. Since in this design the graphene patterns are smaller than the metal pads, the graphene edges are exposed to the aqueous developer and DI water during the last lithography for metallization. Intercalation of water might be the reason for the large data scatter and the high contact and sheet resistance.
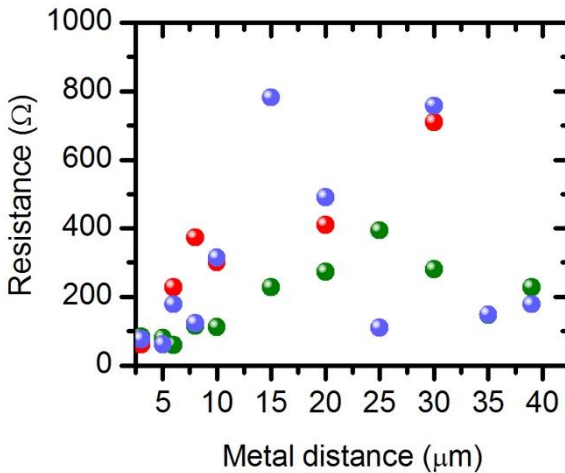
Figure 3.10: Resistance versus the metal pad distance for the sample with the Pd pads on the discrete graphene patterns. Each color presents a separate location and separate TLM structure on the sample.

3.4 Contact resistance on the contact area patterned graphene

The authors of [32] proposed an alternative contacting approach whereby the graphene layer was patterned with cuts prependicular to the contact edge. In their case, the graphene was integrated with a SiC substrate and the patterns were defined by e-beam lithography. In the case of standard contacts (contacts on graphene uniform stripes), they observed a reduction in R_c from 263 to 184 $\Omega.\mu m$ when the sample was annealed in vacuum. For graphene with cuts, the annealing improved R_c from 650 to 125 $\Omega.\mu m$.

To evaluate this approach, we fabricated TLM structures with lithographically defined cuts in graphene to enhance the carrier injection from the contact metal to the graphene layer. The patterns are perpendicular to the channel, such that the perimeter of the graphene edges is maximized and accessible for contact with the metal pads [**Figure 3.11**(a)]. In this design, the width of the cuts is denoted as W, and the density of the cuts is defined by the duty cycle, i.e., the ratio of the uncut-graphene width over the cut-graphene width (W′ /W).

Unfortunately, our contact resistance measurements did not show a clear trend. In some cases, the contact resistance was higher than that of the design without cuts [**Figure 3.11**(c)]. Differences in the substrates used and the fact that the injection length of 1 µm is large are presumably the main reasons for this result. Realizing a smaller injection length requires e-beam lithography, which at the time of this experiment was not availbale in the lab.

In this experiment, the contact resistance is plotted versus duty cycle. One might think to plot the contact resistance versus the contacted area or the contacted perimeter. In this case, after some simple calculations, it is observed that the only important parameter is the number of patterns and because the number of patterns versus duty cycle is almost linear, the conclusion remains the same.
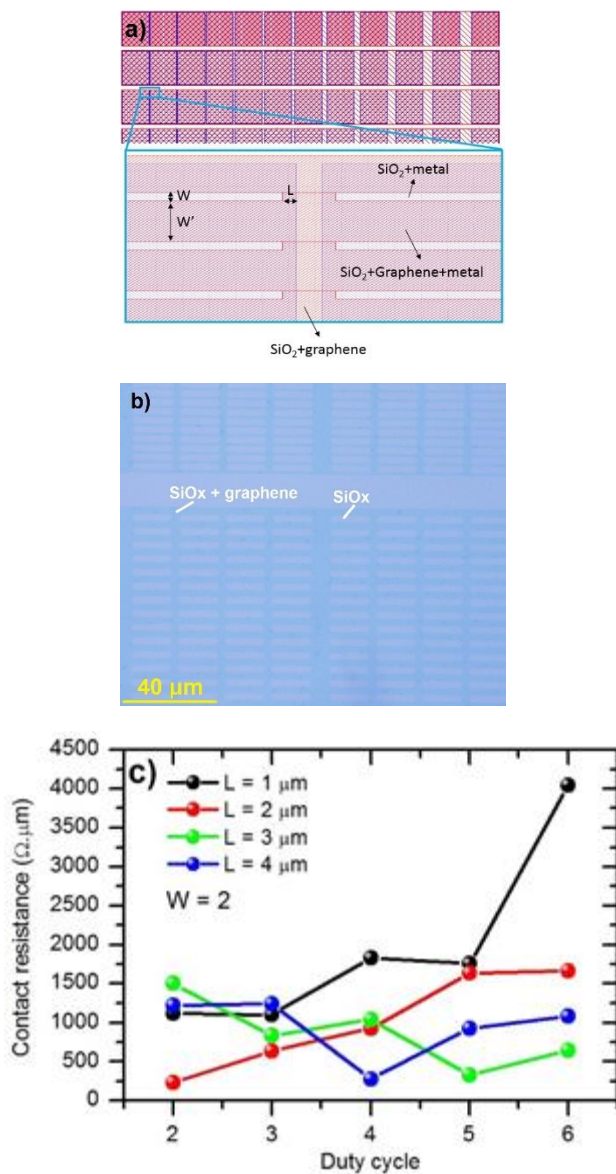
Figure 3.11: a) Design of graphene TLM with patterned graphene in the contact region. b) A graphene stripe with cuts on the contact area fabricated on a SiO_2/Si substrate. c) Contact resistance versus duty cycle for a sample with Pd contacts. Duty cycle is the ratio of W'/W, and L is the spacing between the metal edge and graphene cut edge.

3.5 Contact resistance on the Al_2O_3-capped graphene

In the above experiments, the graphene layer is not protected during the fabrication, which might result in resist residual on the graphene having a direct impact its properties. To avoid this, the graphene layer can be covered with a thin ALD Al_2O_3 layer. **Figure 3.12:** a) Image of the fabricated device after Al2O3 removal. b) and c) Contact resistance versus duty cycle for patterns with widths of 2 µm and 4 µm, respectively.

(a) shows an image of the fabricated TLM structure after Al_2O_3 etching, focused on the contact region.

The process flow starts with marker definition, followed by Al_2O_3 wet etching by phosphoric acid. The Al_2O_3 is removed in patterns perpendicular to the channel in the contact area (width = W) and also between the two TLM structures. Subsequently, lithography and Pd deposition, followed by a lift-off process, are performed on the sample. After lift-off, the remaining graphene between the TLM structures is removed by an O_2 plasma process to isolate the TLM devices.

The results are presented in **Figure 3.12:** a) Image of the fabricated device after Al2O3 removal. b) and c) Contact resistance versus duty cycle for patterns with widths of 2 µm and 4 µm, respectively.

(b),(c) for openings with widths of 2 and 4 µm, respectively. We observed a reduction in the contact resistance by reducing the duty cycle (i.e., increasing the number of patterns in the contact region) with a minimum R_c value of approximately 2000 Ω.µm. No clear trend was observed for either the width of the patterns (W) or the carrier injection length (L). Although the contact resistance in this configuration is higher than that of un-protected graphene (section 3.2), the fabrication process is more stable.
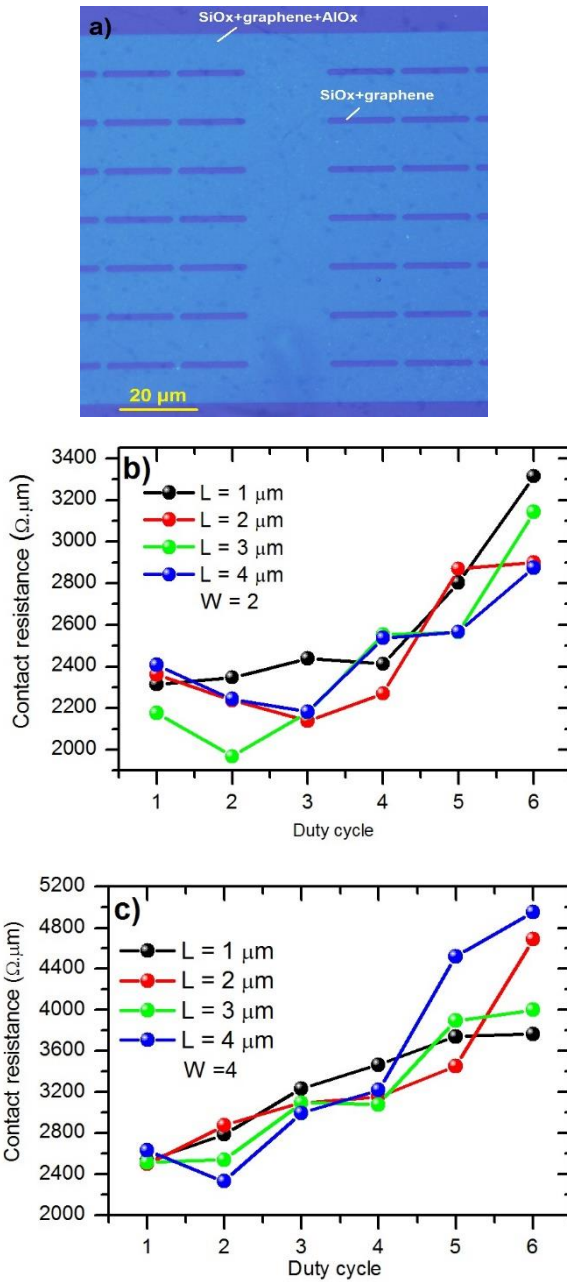
Figure 3.12: a) Image of the fabricated device after Al_2O_3 removal. b) and c) Contact resistance versus duty cycle for patterns with widths of 2 µm and 4 µm, respectively.

3.6 Contact resistance on the Al$_2$O$_3$-capped graphene through graphene edge contacting

In the final experiment, we fabricated a device similar to that described in the previous section; however, in this device, the graphene sheet is completely etched where the Al$_2$O$_3$ layer is removed [**Figure 3.13**(a)]. Thus, the metal electrodes are connected to the graphene layer along the 1D graphene edge. A similar idea has already been reported for graphene encapsulated in HBN, where the entire multilevel stack was etched in the contact area [33]. In another work, the edge contacting approach was applied to un-capped graphene by AMO, and a low contact resistance of 130 Ω.µm was obtained [34].

Our results showed a decrease in the contact resistance with a lower duty cycle [**Figure 3.13**(b)]. The values for the contact resistance obtained from this device were similar to those for un-capped graphene (the best result in this work), with minimum values of 300–1000 Ω.µm. Hence, this design is presented as a configuration with a decent contact resistance, stable processing, and no contamination on the graphene surface. The contact resistance is expected to be reduced, if the photoresist is removed after Al$_2$O$_3$ etching and the Al$_2$O$_3$ layer is used as a hardmask for the graphene etching (for the current device the photoresist was removed only after the graphene etching).
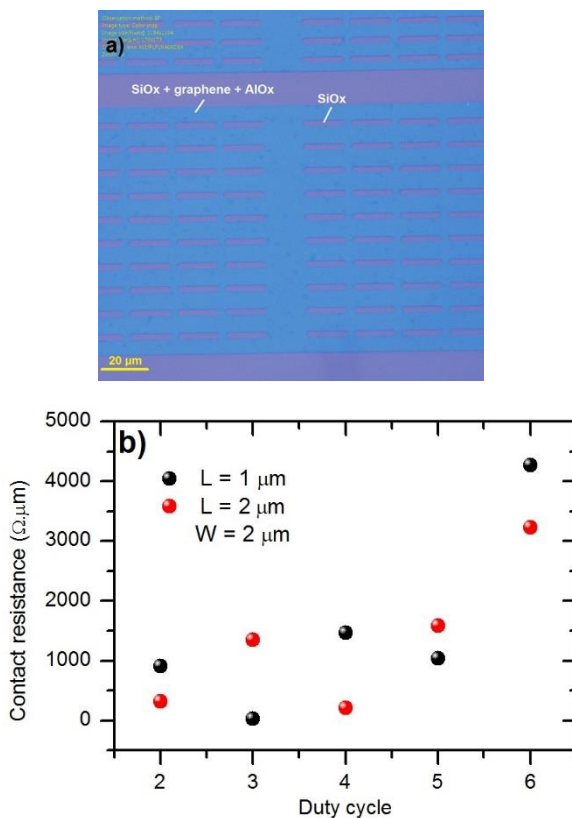
Figure 3.13: a) Image of the fabricated device after Al$_2$O$_3$ and graphene etching. b) Contact resistance versus duty cycle for patterns with widths of 2 µm.

3.7 Conclusion

Since fabrication of graphene-based devices is not straight forward, in this chapter we presented each processing step required for the fabrication of TLM structures. We fabricated TLM devices to achieve two targets. The first one was to develop the main processing steps required for the next chapters. By coating a bilayer resist on graphene, we overcame the graphene delamination issue typically occurring during the graphene patterning step. The second goal was to characterize the graphene sheet resistance and contact resistance. To this end we designed and fabricated TLM structures using five different process flows. The measurement results showed that two types of flows result in decent contact resistance: TLM structures with graphene stripes and TLM structurers with an Al$_2$O$_3$-capped graphene combined with edge contacting. On the graphene stripes, the Pd contact has lower resistance compared to the

Cr contact, with a reasonable graphene sheet resistance of about 400 $\Omega/\square$ and a contact resistance of 400-900 $\Omega.\mu m$. We observed almost the same values for the Al_2O_3-capped graphene combined with graphene edge contacting. The latter is very interesting in the fabrication of graphene based optical devices, since it provides acceptable resistance while the graphene is protected from any environmental influence.

References

[1]   www.graphenea.com

[2]   H. J. Levinson, "Principles of Lithography", 2001.

[3]   A. D. Franklin, S. Han, A. A. Bol, V. Perebeinos, "Double Contacts for Improved Performance of Graphene Transistors", IEEE EDL, 33, 2012.

[4]   O. Balci, C. Kocabas, "Rapid thermal annealing of graphene-metal contact", Appl. Phys. Lett. 101, 243105, 2012.

[5]   B. Huang, M. Zhang, Y. Wang, J. Woo, "Contact resistance in top-gated graphene field-effect transistors", Appl. Phys. Lett. 99, 2011.

[6]   S. Gahng, C. Ho Ra, Y. Jin Cho, J. Ah Kim, T. Kim, "Reduction of metal contact resistance of graphene devices via CO_2 cluster cleaning", Appl. Phys. Lett. 104, 223110, 2014.

[7]   N. Petrone, C. R. Dean, I. Meric, A. M. van der Zande, P. Y. Huang, L. Wang, D. Muller, K. L. Shepard, J. Hone, "Chemical Vapor Deposition-Derived Graphene with Electrical Performance of Exfoliated Graphene", Nano Lett, 12, 6, 2012.

[8]   M. Tanzid, M. A. Andersson, J. Sun, J. Stake, "Microwave noise characterization of graphene field effect transistors", Appl. Phys. Lett. 104, 013502, 2014.

[9]   Y. Wu, Y. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon", Nature, 472, 74–78, 2011.

[10] Chunhum Cho, et al., "Contact resistance improvement by the modulation of peripheral length to area ratio of graphene contact pattern", Appl. Phys. Lett., 106, 2015.

[11] W. Li, Y. Liang, D. Yu, L. Peng, K. P. Pernstich, "Ultraviolet/ozone treatment to reduce metal-graphene contact resistance", Appl. Phys. Lett. 102, 183110, 2013.

[12] A. Hsu, H. Wang, K. Kang Kim, J. Kong, Tomás Palacios, "Impact of Graphene Interface Quality on Contact Resistance and RF Device Performance", IEEE EDL, 32, 8, 2011.

[13] A. Gahoi, V. passai, S. Kataria, S. Wagner, A. Bablich, M.C. Lemme, "Systematic comparison of metal contacts on CVD graphene", Solid State Device Research Conference, 2015.

[14] N. Petrone, I. Meric, J. Hone, K. L. Shepard, "Graphene Field-Effect Transistors with Gigahertz-Frequency Power Gain on Flexible Substrates", *Nano Lett.*, 13,1 , pp 121–125, 2013.

[15] A. Badmaev, Y. Che, Z. Li, C. Wang, C. Zhou, "Self-Aligned Fabrication of Graphene RF Transistors with T-Shaped Gate", *ACS Nano*, 6, 4, pp 3371–3376, 2012.

[16] O. M. Nayfeh, "Radio-Frequency Transistors Using Chemical-Vapor-Deposited Monolayer Graphene: Performance, Doping, and Transport Effects", IEEE TED, 58, 9, 2011.

[17] Y. Wu, Yu-ming. Lin, Ageeth. A. Bol, Keith. A. Jenkins, Fengnian. Xia, "High-frequency, scaled graphene transistors on diamond-like carbon", Nature, 2011.

[18] K. Nagashio, T. Nishimura, K. Kita, A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact", Appl. Phys. Lett. 97, 143514, 2010.

[19] A. Meersha, H. B. Variar, K. Bhardwaj, A. Mishra, S. Raghavan, N. Bhat, M. Shrivastava, "Record Low Metal – (CVD) Graphene Contact Resistance Using Atomic Orbital Overlap Engineering", IEDM, 2016.

[20] C. E. Malec, D. Davidovic, "Vacuum-Annealed Cu Contacts for Graphene Electronics", Solid State Commun, 151, 1791−1793, 2011.

[21] C. W. Chen, F. Ren, G. C. Chi, S. C. Hung, Y. P. Huang, J. Kim, I. I. Kravchenko, S. J. Pearton, U. V. Ozone, "Treatment for Improving Contact Resistance on Graphene", J. Vac. Sci. Technol, 30, 060604, 2012.

[22] O. Balci, C. Kocabas, "Rapid Thermal Annealing of GrapheneMetal Contact", Appl. Phys. Lett., 101, 243105, 2012.

[23] W. Li, Y. Lianf, D. Yu, L. Peng, K. P. Pernstich, T. Shen, A. R. Hight, G. Cheng, C. A. Hacker, C. A. Richter, Q. Li, D. J. Gundlach, X. Liang, "Ultraviolet/Ozone Treatment to Reduce Metal-Graphene Contact Resistance", Appl. Phys. Lett, 102, 183110, 2013.

[24] B. C. Huang, M. Zhang, Y. Wang, J. Woo, "Contact Resistance in Top-Gated Graphene Field-Effect Transistors" Appl. Phys. Lett. 99, 032107. 2011.

[25] A. Hsu, H. Wang, K. K. Kim, J. Kong, T. Palacios, "Impact of Graphene Interface Quality on Contact Resistance and RF Device Performance" IEEE EDL, 32, 1008−1010, 2011.

[26] J. Lee, Y. Kim, H. J. Shin, C. S. Lee, D. Lee, C. Y. Moon, J. Lim, S. C. Jun, "Clean Transfer of Graphene and its Effect on Contact Resistance", Appl. Phys. Lett. 103, 103104, 2013.

[27] J. Choi, H. Kim, J. Park, W. Iqbal, Z. Iqbal, J. Eom, J. Jung, "Enhanced Performance of Graphene by Using Gold Film for Transfer and Masking Process" Curr. Appl. Phys. 14, 1045−1050, 2014.

[28] W. Li, C. A. Hacker, G. Cheng, Y. Liang, B. Tian, A. R. Hight Walker, C. A. Richter, D. J. Gundlach, X. Liang, "Highly Reproducible and Reliable Metal/Graphene Contact by Ultraviolet-Ozone Treatment", J. Appl. Phys., 115, 114304, 2014.

[29] G. Fisichella, S. Di Franco, P. Fiorenza, R. Lo Nigro, F. Roccaforte, C. Tudisco, G. G. Condorelli, N. Piluso, N. Sparta, S. Lo Verso, C. Accardi, C. Tringali, S. Ravesi, F. Microand, "Nanoscale Electrical Characterization of Large-Area Graphene Transferred to Functional Substrates" J. Nanotechnol, 4, 234−242, 2013.

[30] K. Asadi, E. Timmering, T. Geuns, A. Pesquera, A. Centeno, A. Zurutuza, J. H. Klootwijk, P. M. Blom, D. de Leeuw, "Up-Scaling Graphene Electronics by Reproducible Metal−Graphene Contacts", ACS Appl. Mater. Interfaces, vol. 7, 9429, 2015.

[31] S. Min Song, J. Kyung Park, O. Jae Sul, and B. Jin Cho, "Determination of Work Function of Graphene under a Metal Electrode and Its Role in Contact Resistance", Nano.Lett, 12, 2012.

[32] J. T. Smith, A. D. Franklin, D. B. Farmer, C. D. Dimitrakopoulos, "Reducing Contact Resistance in Graphene Devices through Contact Area Patterning", ACS Nano, 7, 4, 2013.

[33] L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard, C. R. Dean, "One-Dimensional Electrical Contact to a Two-Dimensional Material", Science, 2013.

[34] M. Shaygan, M. Otto, A. A. Sagad, C. A. Chavarin, G. Bacher, W. Mertin , D. Neumaier, "Low resistive edge contacts to CVD-grown graphene using a CMOS compatible metal" submitted, 2017.

4

Development of micron-size graphene transfer printing

Contents

In this chapter, we will discuss the development of a novel graphene transfer printing method. Following a brief literature review of transfer techniques for large and micron-scale graphene layers, we will focus on the development of a procedure for the printing of micron-size graphene layers using an automated transfer method. Both single and multiple layer transfer will be presented and characterized using Raman spectroscopy. Finally, the absorption of graphene

transferred on silicon nitride waveguides and resistivity measurements will be discussed. Some of the text in this chapter has been adapted from reference [1].

4.1 Graphene transfer in literature

In recent years, an enormous amount of effort has been devoted to the development of high quality graphene growth, mainly on metal substrates [2]-[4] but also on dielectric substrates [5]-[8]. Integrated photonic devices on the other hand are often fabricated by patterning silicon, III-V semiconductors or silicon nitride layers, not compatible with direct graphene growth. Therefore there is a need for transferring graphene or other 2D materials from its original growth substrate to another substrate [9]-[13]. Thus far, in most cases large size CVD-grown graphene films or individual flakes of exfoliated material are thereby transferred [14]-[21], using different approaches.

In [9], a PMMA layer is spin coated on the graphene substrate (graphene/300nm SiO_2/Si). After that, the surface of SiO_2 is partially etched. The 300 nm SiO_2 is not completely etched and etching of the SiO_2 surface is enough to release the PMMA/graphene layer. Next step is to put the substrate in water and peel off the PMMA/graphene layer manually to detach from the substrate. Lastly, the PMMA/graphene is transferred on the target substrate and PMMA is removed.

In [10], a polymer-free graphene transfer technique is developed. In this method, the graphene-coated copper foil is placed at the interface between hexane (low-viscosity liquid organic layer) and an etching solution of ammonium persulfate to etch the copper foil. Hexane supports the freestanding graphene layer obtained during the copper etching and water rinsing processes. The graphene layer with hexane on top is scooped out with a SiO_2/Si substrate and transferred to a second hexane/water solution to remove copper residuals. From this solution, the graphene layer is transferred on the target substrate (**Figure 4.1**).
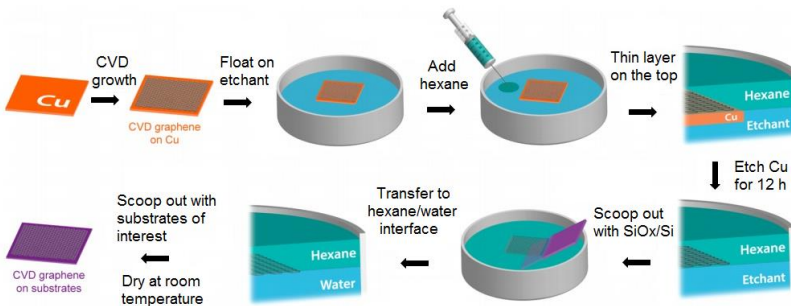
Figure 4.1: Schematic of polymer-free graphene transfer (figure from [10]).

In [11], the graphene transfer relies on nascent gas bubbles and capillary bridges between the graphene film and the underlying substrate during etching of the metal catalyst. In this method, after the N_2 plasma treatment of the substrate (SiO_2/Si), Cu is deposited on the surface and CVD graphene is grown on top. The graphene/Cu/SiO_2/Si wafer is then coated with PMMA and immersed in an etchant solution. The Cu film is then etched and the PMMA/graphene film adheres to the underlying substrate (**Figure 4.2**).
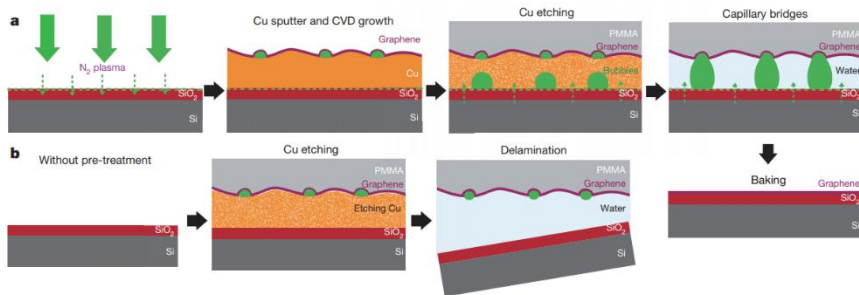
Figure 4.2: Illustration of face-to-face transferring graphene mediated by capillary bridges. a) Schematic of the transfer steps showing 'bubble seeding' by plasma treatment, CVD growth, Cu film etching, formation of capillary bridges and removal of water and PMMA. b) Schematic of the transfer steps showing that in the absence of plasma treatment, the film is delaminated (figure from [11]).

In [12], a 30 inch graphene film transfer for flexible transparent electrodes was developed where a CVD graphene grown on the roll type Cu substrate with a polymer support on top was used. After etching the Cu substrate, the graphene films are transferred from the polymer support onto a target substrate by removing the adhesive force on the polymer support (**Figure 4.3**).
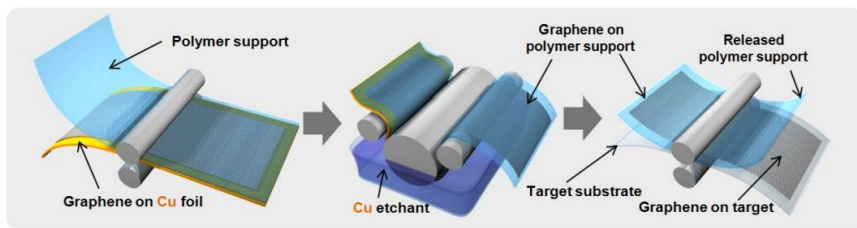
Figure 4.3: Schematic of the roll-based transfer of large graphene films grown on a Cu foil, including adhesion of polymer support, Cu etching and dry transfer on a target substrate (figure from [12]).

In [13], MoS_2 flakes are transferred on a predefined site on the target substrate by using a viscoelastic stamp. MoS_2 is deposited onto the viscoelastic layer by mechanical exfoliation of the bulk layered crystal with Nitto tape. The stamp is

then brought in contact with the target substrate and slowly peeled off to print the MoS$_2$ flakes. The method is strong enough for printing 2D materials and has the advantage of dry process and deterministic printing. However, it does not serve as a deterministic pick up method.

Although all of the above described methods resulted in a successful transfer, they have considerable drawbacks. They lead to an inefficient use of the graphene film, especially on large scale photonic integrated circuits, requiring only graphene in a small area of the entire circuit. In some cases, e.g. on preprocessed substrates with large topography, it might even be impossible to transfer full films of 2D-materials. Therefore, it is essential to develop a method to transfer small patches of graphene to dedicated locations on a target wafer.

Though many such techniques have been proposed, a scalable approach allowing automated dry transfer printing of graphene patches at a given set of locations on a target wafer substrate has not yet been demonstrated. To date, the methods employed for the transfer of micron-size graphene layers rely on manual processes derived from the conventional wet transfer [14]-[16], using home-built tools, and are strongly dependent on the handling skills of the operator. In most cases they are difficult to upscale to full wafer processing.

Figure 4.4 from [22] is an example for the micron-size graphene transfer where the transfer is done by putting a glass fiber into the hole made in the PMMA/graphene.
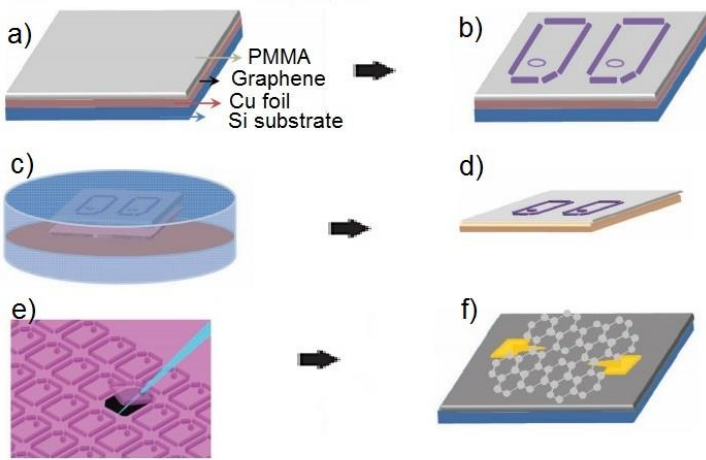
Figure 4.4: Process steps of graphene transfer. a) PMMA coated on graphene grown on copper foil. b) Pattern transfer to PMMA and graphene by e-beam lithography and plasma etching. c) Dissolve copper in $FeCl_3$+HCl solution and clean graphene in deionized water. d) Fished out PMMA/graphene from DI water and suspended on copper grid. e) Dry PMMA/graphene stamps that can be transferred under microscope. f) Print PMMA/graphene stamp to targeted position then dissolve PMMA (modified figure from [22]).

Reference [23] is another work on the micron-size graphene transfer. The method is based on a conventional wet transfer process where the PMMA layer is replaced by a thin layer of Au. Au is deposited on the patterned graphene/copper foil. After cu removal, the graphene layer with Au protection layer is transferred on the target substrate. Finally, the Au layer is etched away.

The main drawback of these methods is that the released graphene layers are transferred to the target substrate by a fiber tip [22] or manually [23], which makes it difficult to scale up to the massive transfer on a wafer. In our approach this drawback is solved by using an automated tool. In addition, a higher transfer printing yield is expected compared to the method introduced in [22]-[23].

In this chapter, we present a new method that allows transfer of micron-size graphene towards any desired site on a target substrate, relying on a commercially available tool used also in the solar, display and electronics industry [24]-[27] and more recently also for the transfer of III-V semiconductors on silicon waveguides [28]. We demonstrate the transfer of patterned monolayer CVD graphene from a SiO_2/Si substrate to different types of target substrates including silicon substrates with a planar SiO_2 film, Si_3N_4 waveguides and palladium (Pd) contacts. Since the transfer is carried out using an automated tool, the graphene quality is not influenced by the operator skills. Hence, our technique allows for a repeatable and

high quality graphene transfer. The presented approach has the capability of transferring micron-size graphene films one by one but allows also transferring multiple films in parallel. This property suggests an efficient way for the wafer scale integration of graphene with other optical components in a photonic chip. Moreover, our technique has the advantage of efficient material use. The graphene can be transferred from a densely populated source substrate to a sparsely populated target substrate. In addition, as after preparing them, the graphene coupons are dry, they can be kept on the source wafer for a long time, allowing the reuse of the source wafer to populate multiple target wafers.

4.2 Developed transfer printing procedure

In this section, we discuss our graphene transfer printing method. First, we introduce the transfer printer and its operation. Then the process flow for the fabrication of the source sample consisting of an array of suspended graphene coupons is discussed. Subsequently, we show the process steps on the real device. Finally, we evaluate the quality of the transferred graphene using different characterization methods.

4.2.1 Transfer printer

The transfer printer (X-Celeprint, model μTP-100) consists of several stages carrying respectively the source sample (a sample with suspended graphene patterns covered by photoresist), the target sample and a cleaning pad (**Figure 4.5**). A patterned PDMS stamp fabricated using a patterned silicon substrate as a master mold is installed on a glass plate and then attached to the stamp holder above the stages. The stage is motorized and has the capability of moving with sub-micrometer accuracy. The different components of the tool were described in detail in [29].

The alignment of the stamp with the source and target samples is visualized on a camera looking through the transparent stamp and stamp holder. A 3-sigma alignment accuracy of 1.5 µm has been reported for this tool [29].
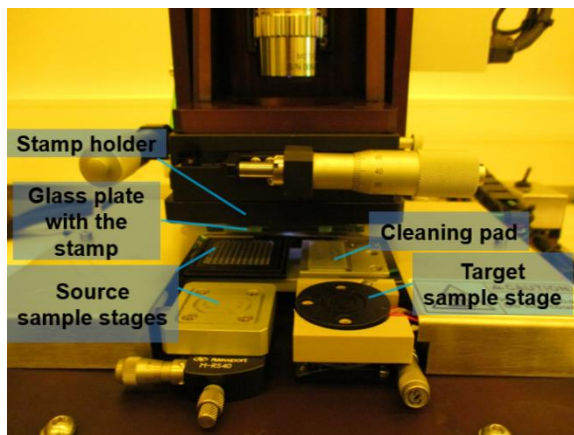
Figure 4.5: The transfer printer machine showing the source sample stage, target sample stage, and cleaning pad. The glass plate with the attached PDMS stamp in the stamp holder is indicated as well.

The stamps were fabricated by X-celeprint using a PDMS mold coated on a Si master wafer. The desired patterns are fabricated on the Si substrate by lithography. The PDMS layer is then casted on the master wafer. After curing, the stamp is separated from the master wafer while the patterns of the master wafer have been transferred on the PDMS. **Figure 4.6** presents the process flow of the PDMS fabrication [30].
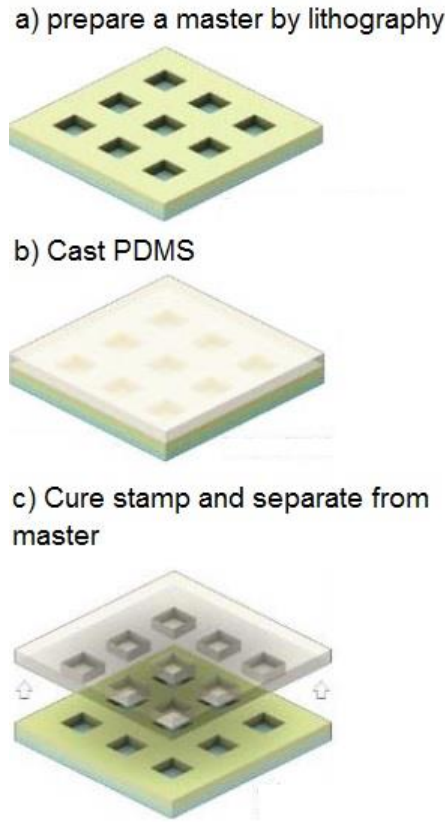
Figure 4.6: Stamp fabrication process flow (figure from [30]).

Pickup and printing are based on controlling the adhesion between the stamp and the graphene structures. Graphene coupons can be picked up from the source substrate by moving up the stamp at high speed thus exerting a force on the coupon exceeding the photoresist tether's strength. They are then printed to the target chip and stay attached while releasing the stamp slowly. This leads to a reduced adhesion between the PDMS and the photoresist, which is now lower than the adhesion of the coupon to the target substrate (**Figure 4.7**) [31],[32]. The tool has a fully automated operation mode whereby the user defines the origin of the first coupon, the horizontal and vertical pitch of the coupons on the source sample, the origin of the first device on the target sample and the pitch between devices on the target sample. From this information the machine is then able to transfer all coupons fully automatically without user intervention. If even higher placement accuracy is required, an additional pattern recognition step with respect to predefined markers on the source and target sample can be added.
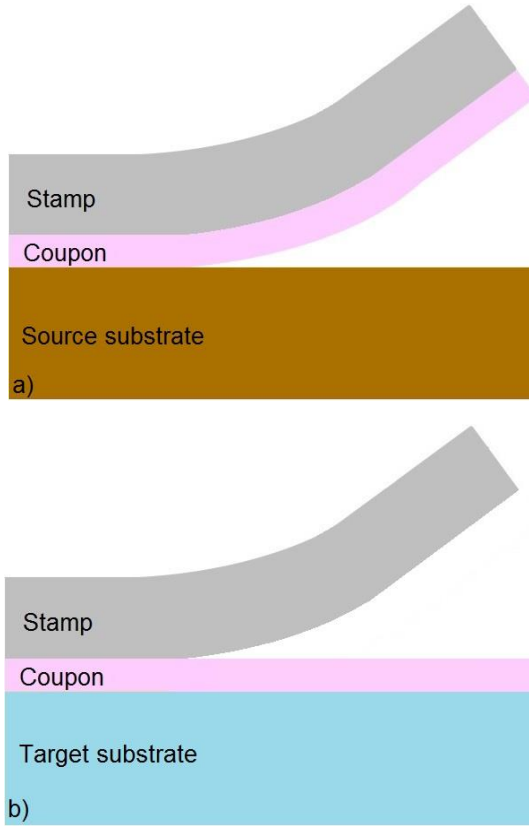
Figure 4.7: Schematic diagrams of the pickup (a) and printing (b) of a coupon.

4.2.2 Source sample preparation

The process flow for preparing the source substrate is illustrated in **Figure 4.8**. The starting point is a CVD grown graphene film on a 300 nm SiO_2 layer on a Si substrate, obtained from Graphenea (www.graphenea.com). First an array of graphene coupons is defined by UV lithography followed by an oxygen plasma, **Figure 4.8**(a). After patterning, the resist is removed with acetone. Then a trench is etched in the 300 nm SiO_2 layer, 10 µm away from the graphene coupons, using a second lithography step, (**Figure 4.8**(b) top view and **Figure 4.8**(c) side view). Following resist removal a new photoresist mask shielding the graphene coupons and forming tethers to the silicon substrate is formed (**Figure 4.8**(d) top view and **Figure 4.8**(e) side view). The used photoresist was TI 35E, a relatively thick resist that can withstand the buffered oxide etch (BOE) needed in the next step. The width of the tethers is a crucial parameter in controlling the under-etch process and avoiding collapse of the coupon while still allowing for easy fracturing during

the pick-up process. For 10×250 µm^2 graphene coupons, we used 2 µm wide tethers. The next step is to under-etch the sacrificial SiO$_2$ layer in a BOE solution, **Figure 4.8**(f). To avoid damaging the photoresist during the BOE etch, the sample was baked 5 min at 150 °C to harden the photoresist. After under-etching, the sample is gently rinsed by DI water and dried by a nitrogen flow. In this stage, the graphene coupons are suspended by the photoresist tethers and ready for pick-up. Now the source and target samples are loaded in the transfer printer. **Figure 4.9**(a) illustrates the pickup of the graphene coupons protected by photoresist, being attached to the stamp and the tethers breaking as expected. **Figure 4.9**(b),(c) are images of the graphene transferred to the target device before and after photoresist removal.

4.2.3 Single coupon transfer

The graphene coupons were defined in an array with x-pitch of 400 µm and y-pitch of 60 µm. After a first pick-up and print of a coupon on the target substrate, the stamp is moved to the cleaning pad to remove any remaining photoresist or other debris from the stamp. To pick up the next coupon, the stamp is moved back to the source substrate, landing on a second graphene coupon. A new coupon is picked up and printed on the desired spot on the target sample, with a pitch not related to that of the coupons on the source wafer, ensuring economical use of the graphene. In this work a semi-automatic mode is used, which is identical to the automatic mode described above, except for the fact that for every transfer the source coupon and target location are selected separately in the user interface. The transfer itself, including pick-up and release speeds are fully controlled by the tool, ensuring reliable operation independent of the operator skills. Note that the size of the post on the patterned PDMS stamp should be close to the size of the oxide etch mask shown in **Figure 4.8**(b) to avoid touching neighboring coupons by the stamp. With a suitable stamp design, containing multiple posts, also multiple coupons can be transferred at the same time. This will be demonstrated in the next section.
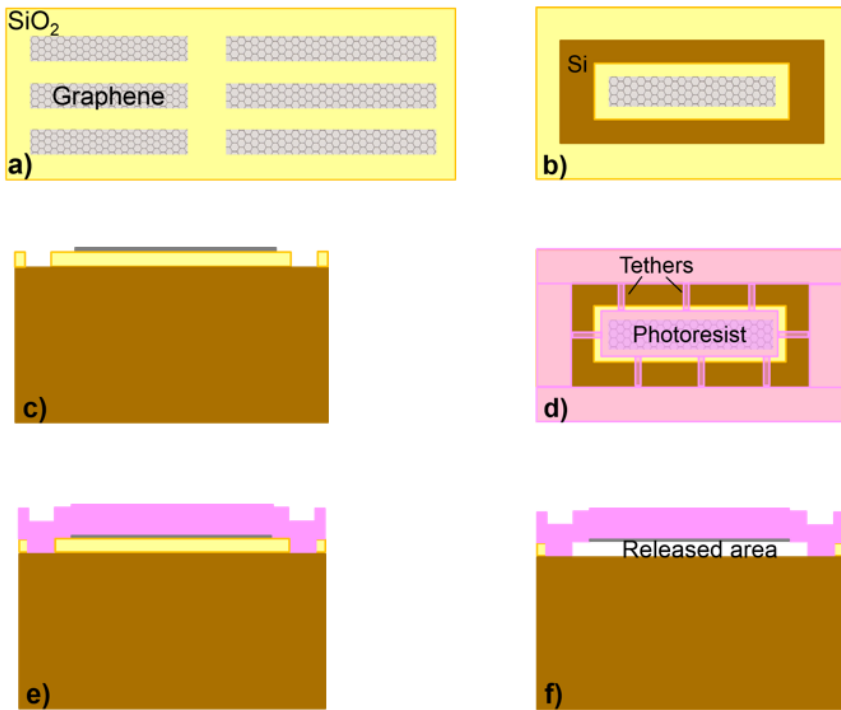
Figure 4.8: Process flow for preparing the source substrate and the actual transfer printing process. a) Top view of array of graphene patterns. b) Top view after SiO_2 patterning. c) Side view after SiO_2 patterning. d) Top view after tether definition. e) Side view after tether definition. f) Side view after under-etching.
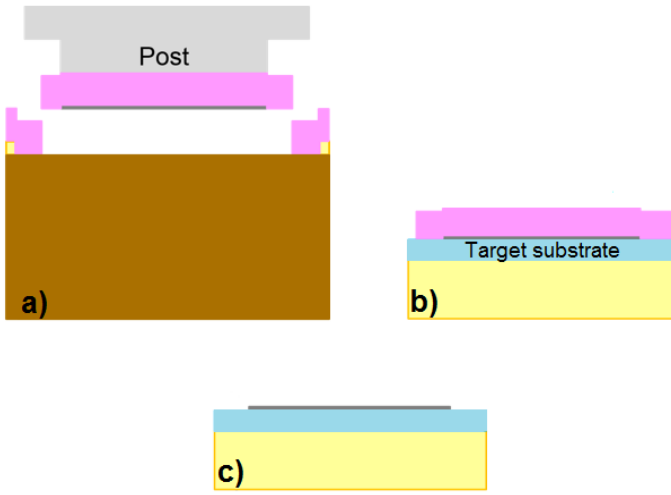
Figure 4.9: a) Pickup of the resist-covered graphene coupon. b) Resist-covered graphene coupon after printing. c) After resist removal.

Figure 4.10 shows the microscope images of the source sample from the graphene patterning step to pickup. One should notice that sometimes after SiO_2 etching (step d) resist at the edge of SiO_2 patterns is cross-linked and it is difficult to remove it with acetone. In this case, the resist remaining at the edge of the SiO_2 patterns is also transferred to the target substrate. However, it can be removed by another lithography step and an O_2 plasma.
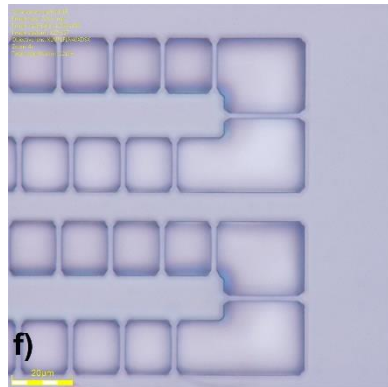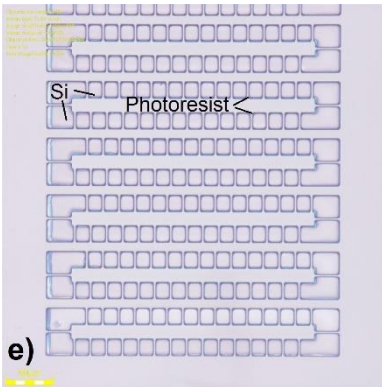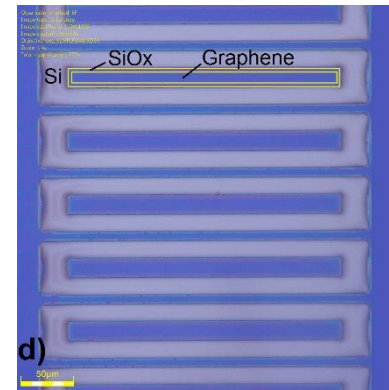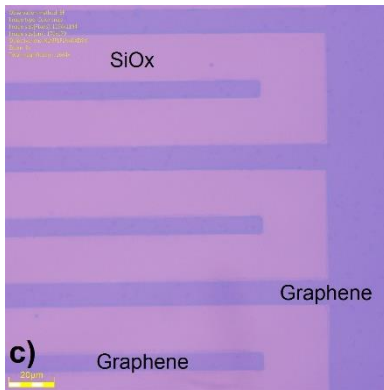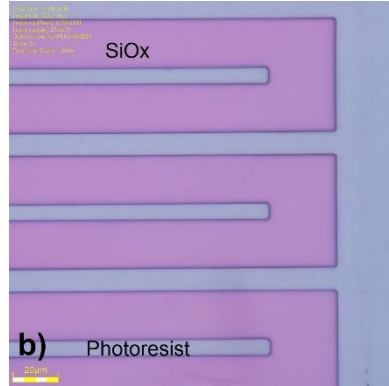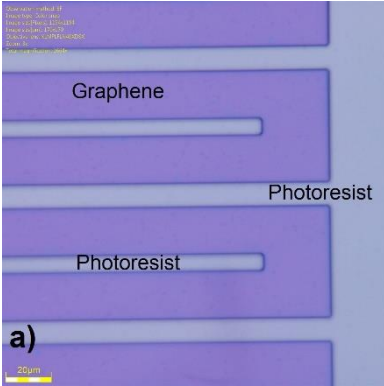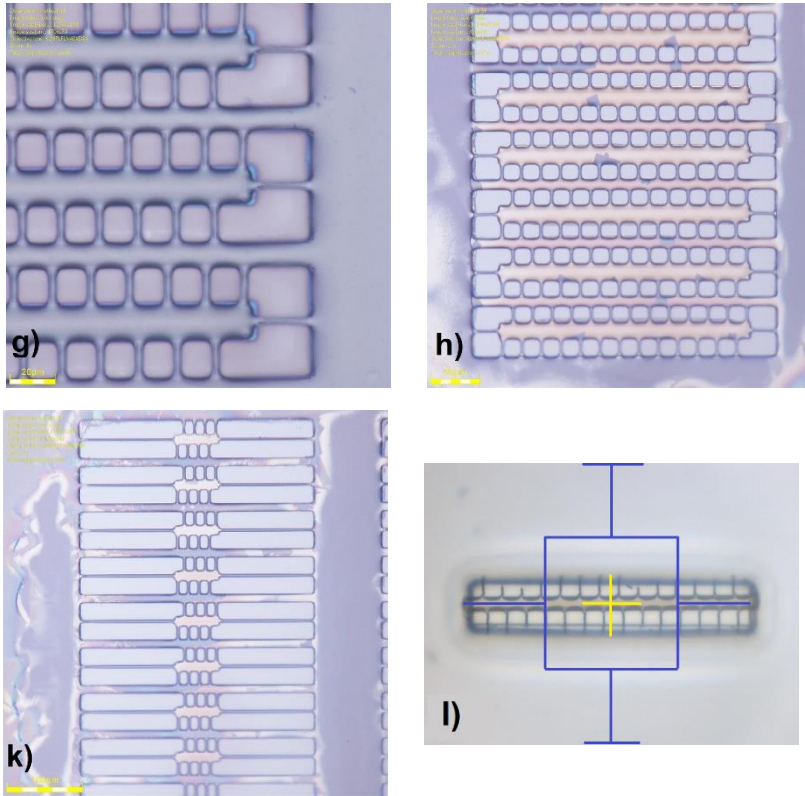
Figure 4.10: Microscope images of the source sample during processing. a) Graphene sheet covered with photoresist, after development, showing graphene in the unprotected region. b) The sample after O$_2$ plasma process. Graphene has been removed in the unprotected region. c) Array of graphene patterns after resist removal. d) Etched SiO$_2$, 10 µm away from graphene. e) Fabricated tethers. f) Zoomed in image of e showing the successful tethers development without breaking. g) Patterns after hard bake. Dark color appears after baking. h,k) Two sets of released coupons with 10 µm and 5 µm width. The yellowish color indicates the coupon is released. l) Coupon on the stamp, the cross and square are used for the alignment.

For preliminary evaluation of the process and the quality of the transferred layers, we transferred graphene to a silicon substrate covered with a 300nm thick SiO$_2$ layer. **Figure 4.11** shows that the Raman spectrum (532 nm excitation source) of the transferred graphene remains very similar to that of the reference sample. For the reference sample the Full Width at Half Maximum (FWHM) of the 2D and G bands are 34 cm^{-1} and 15 cm^{-1} respectively with $I_{2D}/I_G = 2.17$. For the transferred graphene we found a 2D band FWHM of 30 cm^{-1}, a G band FWHM of 16 cm^{-1} and $I_{2D}/I_G = 2.173$ in good agreement with the reference sample. No D band, indicative of defects in the sample is introduced, attesting of the fact that the proposed transfer technique does not degrade the graphene quality. The only

difference with the reference sample is that the small peak close to 2400 cm^{-1} in the reference sample is not observed in our measurement. The reason is not fully clear, but it probably relates to the several process steps carried out during the coupon preparation. Another reason could be the high level of noise observed in the transferred graphene.
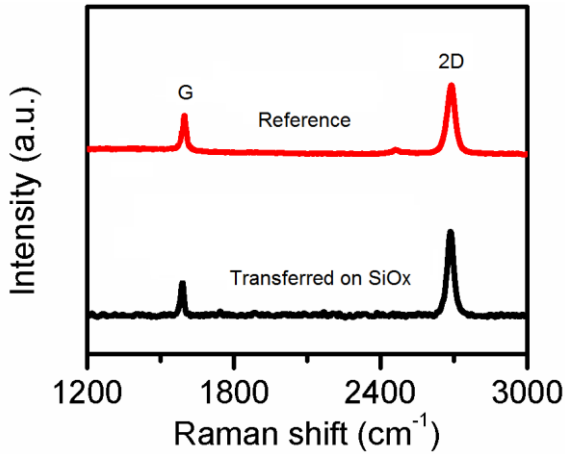
Figure 4.11: The Raman spectrum of a graphene coupon transfer printed on SiO$_2$ compared with the Raman spectrum of the reference sample.

4.2.4 Multiple coupon transfer

To demonstrate the possibility of transferring multiple coupons of graphene simultaneously, a stamp with a 2×2 pattern of posts is used. It consists of a bulk PDMS layer patterned with 4 posts of 40×40 µm^2 with x-pitch of 250 µm and y-pitch of 350 µm [**Figure 4.12**(a)]. **Figure 4.12**(b) shows a schematic cross section of the stamp.
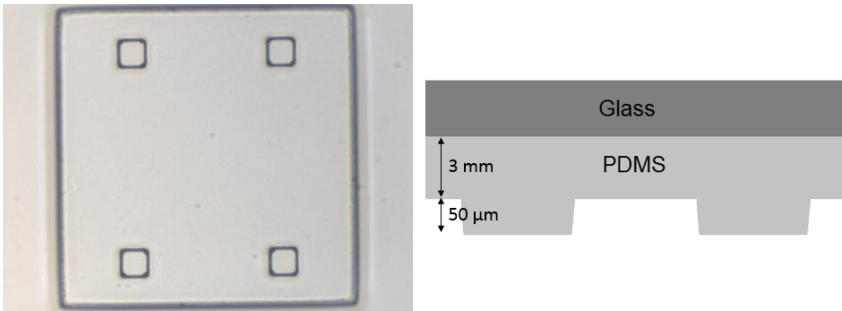
Figure 4.12: a) PDMS-stamp with 4 posts for parallel transfer. b) Schematic cross section of the stamp showing two post in the top part of image a).

The pitch of this stamp was chosen to be an integer multiple of the pitch of the graphene coupons on the source wafer, such that in every pick and print operation four graphene coupons are being transferred. We carried out 20 transfer steps (80 graphene coupons total) of which 17 were fully successful. In the other 3 cases at least one of the coupons was not printed. Although not tried here such a failure can in principle be corrected by printing another coupon. The yield could be improved with optimization of the tether design ensuring the tethers break such that there is no tether debris underneath the graphene. **Figure 4.13**(a) and **Figure 4.13**(b) show the transferred graphene coupons before and after removing the protective photoresist. The Raman spectrum in **Figure 4.13**(c), clearly proves the transfer was successful.
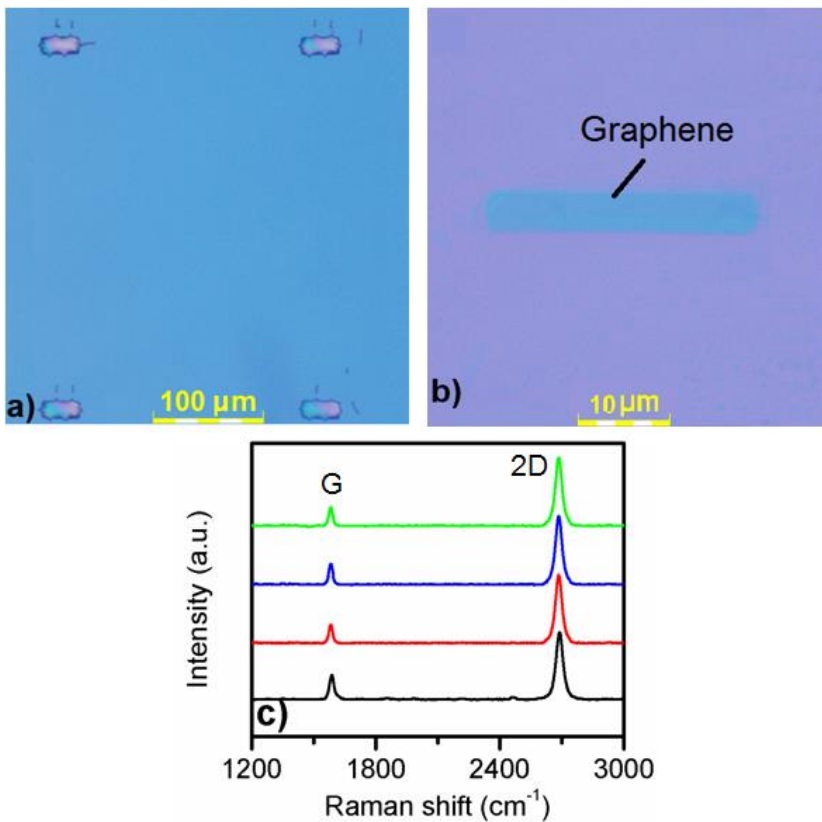
Figure 4.13: a) Microscope image of 4 resist-covered graphene coupons simultaneously transferred using the stamp shown in Figure 4.12. b) Zoomed-in image of the graphene after photoresist removal. c) Raman spectra of 4 simultaneously transferred graphene coupons.

4.2.5 Transferred graphene absorption

To characterize the optical loss of the printed graphene, we transferred several graphene coupons on planarized silicon nitride waveguides (width = 800 nm, height = 300 nm) with a surface topography of 20 nm, as shown in **Figure 4.14**(a). **Figure 4.14**(b) shows a magnified image from one of the resulting patterns, showing a clean graphene film covering the waveguide. **Figure 4.14**(c) shows the excess loss of the different graphene covered waveguides with respect to a reference waveguide. The extracted loss of 0.054 dB/µm is in line with simulations [33]. **Figure 4.14**(d) shows a series of Raman measurements taken at different points on a line orthogonal to the waveguide, starting and ending just outside the rectangular graphene area. Therefore, in the recorded spectra, we expect to see peaks associated with monolayer graphene for the central measurement points and no peaks for the outer points (traces number 1 and 10). For the edge traces (number 2 and 9) there is a D band, associated with defects, visible in the spectra. The central traces do not show this band however and for the central trace (number 6) the 2D and G band exhibit a FWHM equal to 33 cm^{-1} and 15 cm^{-1} respectively with I_{2D}/I_G =2.36, again comparable with the reference graphene.
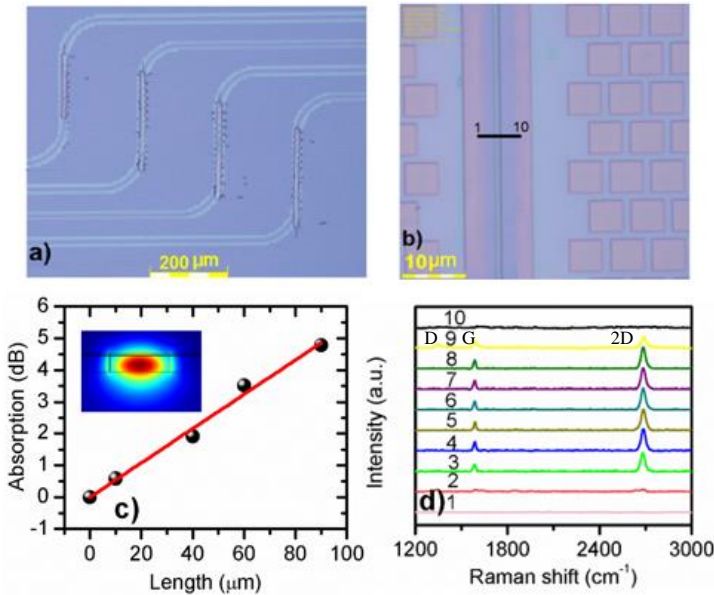
Figure 4.14: a) Resist-covered graphene coupons transferred on Si$_3$N$_4$ waveguides. b) Zoomed-in image after photoresist removal. c) Excess loss as function of graphene length. Inset image is the optical mode profile of a graphene integrated Si$_3$N$_4$ waveguide. d) Raman spectra taken at different points along the line orthogonal with the waveguide as shown in b).

4.2.6 Transferred graphene resistivity

In a final experiment to assess the developed process, we measured the electrical resistivity of transfer printed graphene by a two-probe measurement. To this end we defined Pd electrode patterns on a SiO_2/Si substrate using a standard lift-off process. After resist patterning on the target wafer but before metal deposition the SiO_2 was slightly etched such that after the Pd lift-off the sample was planarized with a surface topography of 2 nm. Then graphene coupons were transferred on the Pd contacts. Finally, the photoresist on top of the graphene was removed. The result, before and after removing the resist is shown in **Figure 4.15**(a) and **Figure 4.15**(b) respectively. The size of the graphene patterns was fixed at 4×25 μm^2. The contact pad separation was varied from 3 to 25 μm.

   The sheet and contact resistance were extracted by applying a voltage between both contacts and measuring the resistance as a function of the contact separation (**Figure 4.16**). From the intercept and slope of this curve, the sheet and contact resistance of graphene were found to be 398 Ω/sq and 2990 $\Omega.\mu m$, respectively. The contact resistance and sheet resistance measured for conventional TLM structures fabricated on samples from the original source wafer are 352 Ω/sq and 928 $\Omega.\mu m$ respectively, similar to other reported values for CVD graphene [34]. This shows that the sheet resistance, and accordingly the graphene quality, is almost not affected by the graphene process but that contacting process is open for further improvement. One reason for the high contact resistance could be contamination by the use of photoresist in several steps. As such, I believe the contact resistance could be improved by using encapsulated graphene and an edge contact scheme.
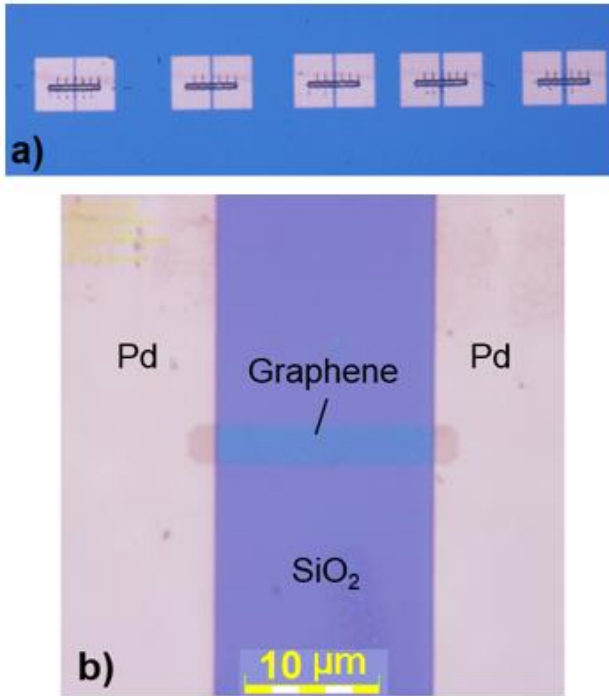
Figure 4.15: a) Transferred graphene sheets on the Pd contact patterns with different contact distance (graphene photoresist encapsulation still present) b) zoomed-in image of graphene on Pd after photoresist encapsulation removal. The distance between contacts is 20 µm.
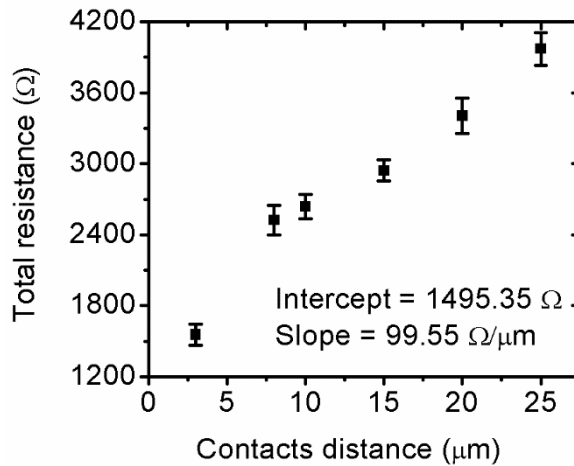
Figure 4.16: Resistance as a function of separation between Pd contacts.

4.3 Conclusion

In summary, we presented a new method for transferring multiple micron-size monolayer CVD graphene coupons to a desired site on a target substrate in a reproducible and scalable way using a commercial tool (model µTP-100 from X-Celeprint). The processing steps for preparation of the source substrate including graphene patterning, SiO_2 etching and the realization of a photoresist encapsulation layer were discussed. The encapsulation layer including tethers that support the free-hanging graphene coupons enables us to release the latter by under-etching the SiO_2 substrate. The tether size was shown to play an important role in successfully suspending the graphene layers. The pickup and printing speed were optimized to reach a 100% pickup yield and print yield of 95% (in the single coupon transfer). The root cause for the lower print yield is believed to be related to residues originating from the tethers getting underneath the graphene layer. The yield could be improved with further optimization of the tether design ensuring the tethers break such that there is no tether debris underneath the graphene. In addition, an oxygen plasma treatment of the target sample might result in a cleaner target surface and therefore improve the print yield. Raman measurements on the printed graphene coupons and a reference graphene structure indicate the quality of the graphene is preserved after printing. Graphene coupons printed on Pd contact pads allowed us to measure the contact and the sheet resistance of the transferred graphene, which are in line with other reported values for CVD graphene. Similar results were observed for TLM devices. In the next chapters we will use this process to realize a silicon photonic crystal based switch and an electro-absorption modulator integrated with a SiN waveguide.

References

[1] L. Abdollahi shiramin, A. Bazin, S. Verstuyft, S. Lycke, P. Vandenabeele, G. Roelkens, D. Van Thourhout, "Transfer printing of micron-size graphene for photonic integrated circuits and devices", ECS J. Solid State Sci. Technol., 6, 7, 2017.

[2] H. Wang, Yu. G, "Direct CVD Graphene Growth on Semiconductors and Dielectrics for Transfer-Free Device Fabrication", Advanced Materials,. 28, 4956-4975, 2016.

[3] M. Losurdo, M. Michela, P. Capezzuto, G. Bruno, "Graphene CVD growth on copper and nickel: role of hydrogen in kinetics and structure", Phys. Chem. Chem. Phys,. 13, 20836-20843, 2011.

[4] L. Gao, W. Ren, H. Xu, L. Jin, Z. Wang, T. Ma, L. Ma, Z. Zhang, Q. Fu, L. Peng, X. Bao, H. Cheng, "Repeated growth and bubbling transfer of graphene with millimetre-size single-crystal grains using platinum", Nature Communications, 3, 1-7, 2012.

[5] Y. Kim, K. Joo, S. Jerng, J. Lee, E. Yoon and S. Chun, "Direct growth of patterned graphene on SiO_2 substrates without the use of catalysts or lithography", Nanoscale,. 6, 10100-10105, 2014.

[6] G. Pan, B. Li, M. Heath, D. Horsell, M. Lesley, L. Taan and S. Awan, "Transfer-free growth of graphene on SiO_2 insulator substrate from sputtered carbon and nickel films", Carbon,. 65, 349–358, 2013.

[7] D. McNerny, B. Viswanath, D. Copic, F. Laye, C. Prohoda, A.C. Brieland-Shoultz, E.S. Polsen, V.S. Veerasamy and A.J. Hart, "Direct fabrication of graphene on SiO_2 enabled by thin film stress engineering", Scientific Reports,. 4, 2014.

[8] A. Ismach, C. Druzgalski, S. Penwell, A. Schwartzberg, M. Zheng, A. Javey, J. Bokor and Y. Zhang, "Direct Chemical Vapor Deposition of Graphene on Dielectric Surfaces", Nano Lett,. 10, 5, 1542–1548, 2010.

[9] A. Reina, H. Son, L. Jiao, B. Fan, M.S. Dresselhaus, Z. Liu and J. Kong, "Transferring and Identification of Single- and Few- Layer Graphene on Arbitrary Substrates", Physical chemistry C, 112, 17741–17744, 2008.

[10] G. Zhang, A. G. Güell, P. M. Kirkman, R. A. Lazenby, T. S. Miller, P. R. Unwin, "Versatile Polymer-Free Graphene Transfer Method and Applications", ACS Appl. Mater. Interfaces, 8, 8008–8016, 2016.

[11] L. Gao, G. Ni, Y. Liu, B. Liu, A.H. Neto and K.P. Loh, "Face-to-face transfer of wafer-scale graphene films", Nature,. 505, 190–194, 2014.

[12] S. Bae et al, "Roll-to-roll production of 30-inch graphene films for transparent electrodes", nature nanotechnology,. 5, 2010.

[13] A. Castellanos-Gomez, M. Buscema, R. Molenaar, V. Singh, L. Janssen, H. S J van der Zant, G. Steele, "Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping", 2D materials, 1, 2014.

[14] M. Liu, X. Yin, E. Ulin-Avila, B. Geng, T. Zentgraf, L. Ju, F. Wang, X. Zhang, "A graphene-based broadband optical modulator", Nature, 474, 2011.

[15] M. Liu, X. Yin, X. Zhang, "Double-layer graphene optical modulator", Nano.Lett, 12, 2012.

[16] N. Youngblood, Y. Anugrah, R. Ma, S. J. Koester, M. Li, "Multifunctional graphene optical modulator and photodetector integrated on silicon waveguides", Nano Lett, 14, 2741–2746, 2014.

[17] Y. Hu et al., "Broadband 10 Gb/s operation of graphene electro-absorption modulator on silicon", Laser Photon. Rev., 1, 1–10, 2016.

[18] H. Dalir, Y. Xia, Y. Wang, X. Zhang, "Athermal Broadband Graphene Optical Modulator with 35 GHz Speed", ACS Photonics, 3, 2016.

[19] Z. Sun, A. Martinez, F. Wang, "Optical modulators with 2D layered materials", Nat.Photon, 10, 2016.

[20] X. Wang, Z. Cheng, K. Xu, H. Tsang, J. Xu, "High-responsivity graphene/silicon-heterostructure waveguide photodetectors", Nat.Photon, 7, 2013.

[21] J. Wang, Z. Cheng, Z. Chen, X. Wan, B. Zhu, H. Tsang, C. Shu, J. Xu, "High-responsivity graphene-on-silicon slot waveguide photodetectors", Nanoscale,. 8, 13206-13211, 2016.

[22] Y. Bie, Y. Zhou, Z. Liao, K. Yan, S. Liu, Q. Zhao, S. Kumar, H. Wu, G.S. Duesberg, G.L.W. Cross, J. Xu, H. Peng, Z. Liu and Yu. D, "Site-Specific Transfer-Printing of Individual Graphene Microscale Patterns to Arbitrary Surfaces", Adv. Mater, 23, 3938–3943, 2011.

[23] X. Chen, Z. Liu, W. Jiang, X. Yan, F. Xing, P. Wang, Y. Chen and J. Tian, "The selective transfer of patterned graphene", Sci. Rep, 3, 2013.

[24] S. Cha, M. Cha, S. Lee, J. Hyoun Kang, C. Kim, "Low-Temperature, Dry Transfer-Printing of a Patterned Graphene Monolayer", Sci. Rep, 2015.

[25] J. Yoon, S. Jo, I. Chun, I. Jung, H. Kim, M. Meitl, E. Menard, X. Li, J. Coleman, U. Paik, J. A. Rogers, "GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies", Nature., 465, 2010.

[26] S. Park, Y. J. Xiong, R. H. Kim, P. Elvikis, M. Meitl, D. H. Kim, J. Wu, J. Yoon, C. J. Yu, Z. J. Liu, Y. G. Huang, K. Hwang, P. Ferreira, X. Li, K. Choquette, J.A. Rogers, "Printed Assemblies of Inorganic Light-Emitting Diodes for Deformable and Semitransparent Displays", Science, 325, 977–981, 2009.

[27] C. Bower, E. Menard, S. Bonafede, J. Hamer, S. Cok, "Transfer-Printed Microscale Integrated Circuits for High Performance Display Backplanes", IEEE Trans. Compon. Pack. Manufac. Technol. 1, 1916-1922, 2011.

[28] A. De Groote, P. Cardile, A. Subramanian, A.M. Fecioru, C. Bower, D. Delbeke, R. Baets and G. Roelkens, "Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters", Opt. Exp, 27, 13754-13762, 2016.

[29] A. Carlson, A. M. Bowen, Y. Huang, R. G. Nuzzo, J. A. Rogers, "Transfer Printing Techniques for Materials Assembly and Micro/Nanodevice Fabrication", Adv. Mater, 24, 5284–5318, 2012.

[30] D. Gomez, K. Ghosal, A. Meitl, S. Bonafede, C. Prevatte, T. Moore, B. Raymond, D. Kneeburg, A. Fecioru, A. Jose Trindade, C. A. Bower, "Process Capability and Elastomer Stamp Lifetime in Micro Transfer Printing", IEEE 66th Electronic Components and Technology Conference, 2016.

[31] C. Bower, D. Gomez, K. Lucht, B. Cox, D. Kneeburg, "Transfer-printed integrated circuits for display backplanes", in Proceedings of International Display Workshop, 1203–1206, 2010.

[32] L. A. Meitl, Z. Zhu, V. Kumar, K. Lee, X. Feng, Y. Y. Huang, I. Adesida, R. G. Nuzzo, J. A. Rogers, "Transfer printing by kinetic control of adhesion to an elastomeric stamp", Nat.Mat, 5, 33 – 38, 2006.

[33] L. Abdollahi Shiramin and D. Van Thourhout, "Graphene Modulators and Switches Integrated on Silicon and Silicon Nitride Waveguide", JSTQE, 23, 2017.

[34] K. Asadi, E. Timmering, T. C. T. Geuns, A. Pesquera, A. Centeno, A. Zurutuza, J. H. Klootwijk, P. W. M. Blom and D. M. de Leeuw, "Up-Scaling Graphene Electronics by Reproducible Metal−Graphene Contacts", ACS Appl. Mater. Interfaces, 7, 9429, 2015.

5

Graphene-Si photonic crystals switches

Contents

In this chapter, we will present the results on the fabrication and characterization of graphene-based switches where graphene is integrated on a Si PhC cavity. Two types of devices will be discussed: graphene integrated on a front-coupled cavity and graphene integrated on a side-coupled cavity. Some of the text in this chapter has been adapted from reference [1].

5.1 Graphene-based switch integrated on a Si PhC cavity

To demonstrate the versatility of the transfer printing method developed in the previous chapter we integrate graphene with PhC cavities to realize ultra-compact switches. Integrating graphene with resonant structures such as ring resonators or photonic crystal (PhC) cavities enhances the interaction of the optical field with the graphene layer [2]-[4], resulting in a reduced size of the required graphene layer, and the associated capacitance. In this chapter, we first present the fabrication of a graphene-based integrated switch using the transfer printing process developed in chapter 4. We thereby use an automated commercial transfer printer to integrate a micron-scale graphene layer with a 1D silicon photonic crystal. Next, we present the experimental results, demonstrating a voltage dependent transmission for the hybrid graphene SOI-PhC nano-cavity. The graphene Fermi level is tuned from its intrinsic state to beyond the transparency region by gating the graphene layer using a polymer electrolyte [5]. Finally, we link these results with a theoretical model and predict possible improvements to the design.

5.2 Front-coupled PhC cavity

5.2.1 Design and fabrication

Figure 5.1 illustrates the design of the proposed device. It consists of a 1-D SOI front-coupled PhC nano-cavity with a patterned graphene layer deposited on top. Metal contacts are deposited at both sides of the graphene layer, 1 μm away from the edges of the cavity. The SOI-PhC nano-cavities consist of two mirror sections with a taper section in between. The radius of the holes gradually decreases from the center to both sides. Geometric parameters of the cavity are listed in **Table 5.1**. The cavities were designed by Weiqiang Xie.
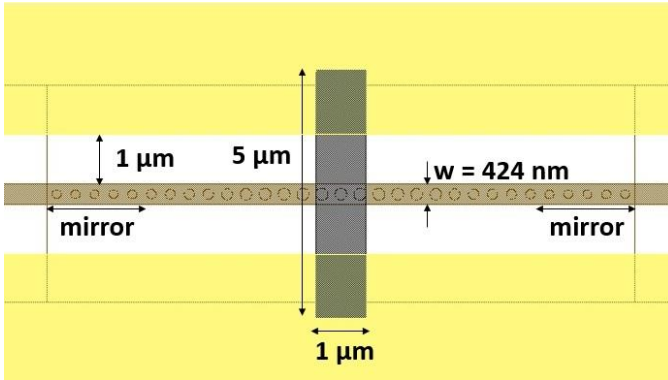
Figure 5.1: Schematic of the graphene-based switch showing the graphene layer on three central holes only and metal pads with 1 µm spacing from the cavity.

Table 5.1: Design parameters of the front-coupled cavity.

Front-coupled cavity	Waveguide width (nm)	Coupling gap (nm)	Height (nm)
	424	-	220
Mirror section	Length (µm)	Hole diameter (µm)	Distance between holes (µm)
	1.92	0.178	0.208
Taper section: Hole	Length (µm)	Hole diameter (µm)	Distance between holes (µm)
1	8.08	0.187	0.203
2		0.197	0.193
3		0.207	0.183
4		0.215	0.174
5		0.221	0.167
6		0.227	0.161
7		0.233	0.155
8		0.237	0.150
9		0.239	0.147
10		0.241	0.145
11 (central hole)		0.241	0.145

The devices are fabricated on a 300 mm SOI wafer in a CMOS pilot line using 193 nm immersion lithography. The holes and waveguides are etched in a 220 nm-thick silicon layer on top of a 2 μm buried silicon oxide layer. The devices are planarized by SiO_2 deposition and chemical mechanical polishing (CMP). The cavity IL and Q-factor were 5 dB and 40,000 before integration with graphene. After fabrication of the SOI-PhC nano-cavity, graphene is transfer printed on top using the process described in chapter 4 [**Figure 5.2**(a)]. The next step is to fabricate the palladium contact pads on the graphene layer, 1 µm away from the cavity edges. After the lift-off process, a polymer electrolyte layer consisting of LiClO4 and polyethylene oxide (PEO) in a weight ratio of 1:10 is spin coated on the Si chip. This layer will allow to control the graphene Fermi-level [6]. **Figure 5.2**(b) shows a microscope image of the fully fabricated device.
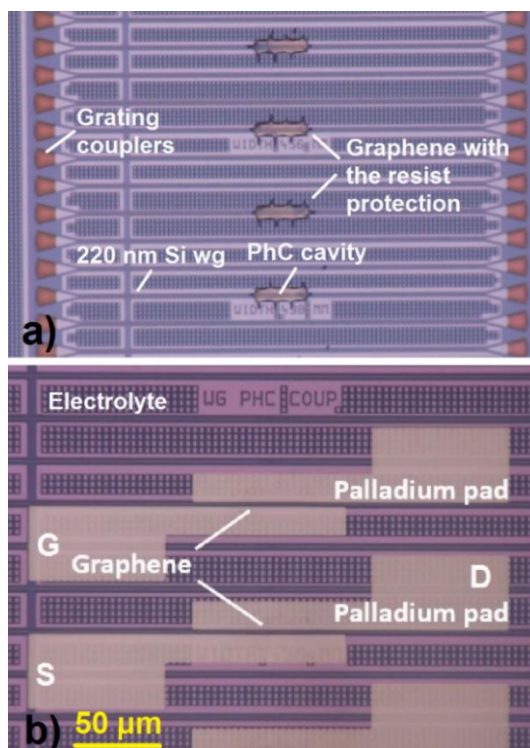
Figure 5.2: (a) Top view of the Si sample with the transferred coupons on top. To provide enough space for contacts, only a subset of the cavities is covered with a graphene layer. (b) Top view of a fully fabricated device. An electrolyte layer has been coated on the sample to gate the graphene layer. Given its small size and transparency, the graphene layer is not visible in this image.

5.2.2 Characterization of the device performance

The 1D PhC device is connected to single mode access waveguides integrated with grating couplers for optical characterization. The graphene Fermi level is tuned by applying a gate voltage V_{gs} between one of the contacts of the device under study and a contact of an identical device directly next to it, with the electrolyte serving as the gate dielectric. **Figure 5.3** plots the measured transmission for applied gate voltages varying from +1.2 V to -1.2 V. The transmission increases and the linewidth narrows as the voltage becomes more negative. This indicates the graphene layer becomes more transparent, as expected. For positive voltages this effect is weaker as the transferred graphene is intrinsically p-doped (originating from the PMMA used by Graphenea in the transfer process and doping from water absorption from the environment).
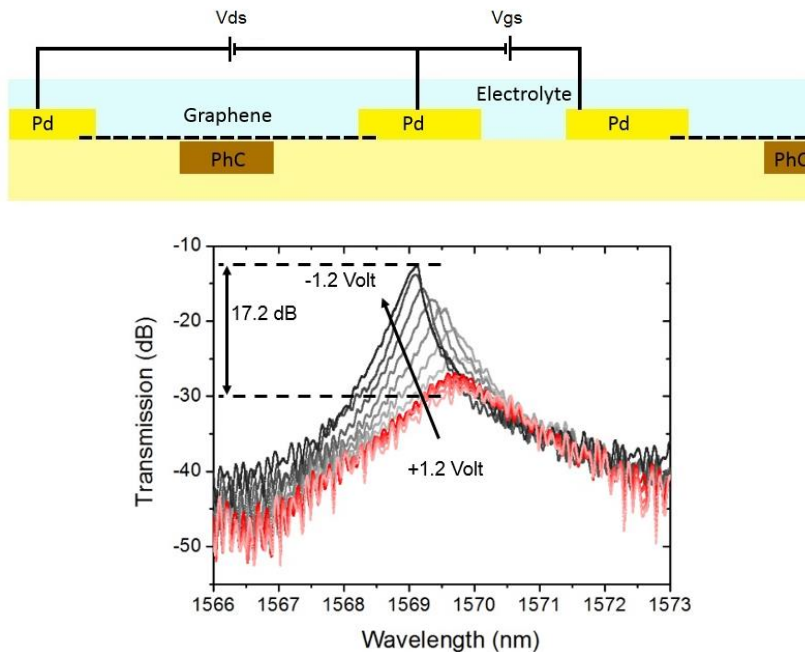
Figure 5.3: top) Cross section of the device. bot) Transmission spectrum of the hybrid graphene SOI-PhC cavity for different gate voltages. The grating couplers loss has been extracted in this figure.

Figure 5.4 shows the *ER*, measured at 1569.07 nm, the wavelength of maximum transmission for an applied voltage of -1.2 V. This figure shows that applying only -1.2 V results already in an extinction ratio (*ER*) as high as

17.2 dB. Increasing the drive voltage to 2 V, from -1.2 to 0.8 V (the neutrality point of graphene), the *ER* further increases to 19 dB.
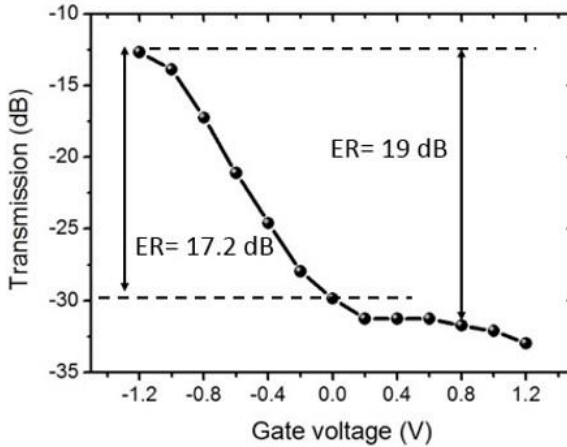
Figure 5.4: Transmission at the resonance wavelength of -1.2 V versus gate voltage.

The gate voltage dependent quality factor is extracted by fitting a Lorentzian function to the transmission spectra. It increases from 2000 at positive voltages to about 6000 at -1.2 V (**Figure 5.5**). The corresponding wavelength shift is 0.8 nm. The *Q* factor enhancement with the gate voltage originates from the decrease in the graphene absorption coefficient. The strong blue shift indicates there is not only a strong modulation of the imaginary part of graphene's dielectric constant but also of its real part, resulting in a phase shift. In line with what is expected from theory [4], this change in the real part is in particular relevant if the chemical potential comes close to 0.4 eV, or for gate voltages below 0 V.

Using a perturbative approach, the cavity resonance and its line width can be expected to vary linearly with the gate-dependent dielectric constant of graphene:

$$\Gamma_R = \Gamma_R{}^0 + \alpha Im[\varepsilon_g(\omega)] \tag{5.1}$$

for the cavity line width and

$$\lambda_R = \lambda_R{}^0 + \beta Re[\varepsilon_g(\omega)] \tag{5.2}$$

for the cavity resonance wavelength [2]. To link the experimental data to a theoretical model for the graphene dielectric constant [7], we need to relate the actually applied gate voltage to the fermi level of the graphene layer, using the following formula [2], also used in chapter 2:

$$E_f = \hbar v_f \sqrt{n_b + \pi \left(\frac{C|V|}{q}\right)} \tag{5.3}$$

In this case however, C is the capacitance related to the depletion layer induced in the ionic gel [5]. The intrinsic carrier density n_b and the fermi velocity v_f are defined as before. Fitting the experimental data to the theoretical model gives us the following values for the different parameters: $\alpha \sim 0.12$, $\beta \sim 0.4$, $C \sim 27$ mF/m^2, $n_b \sim$ 9e12 cm^{-2} and $\Gamma \sim 26$ fs with Γ the scattering time. The NMSE (normalized mean square error) for the Q factor fitting and cavity resonance fitting is 0.03 and 1.2e-8, respectively. In **Figure 5.6** we plot the corresponding relation between E_f and V, showing the neutrality point at 0.6 V. Another observation is that for positive voltages the Fermi level does not reach the transparency region (<0.4 eV) explaining the absorptive behavior of graphene in the transmission spectra for positive voltages (**Figure 5.3**). The mobility of our graphene is 2000 cm^2/V.s corresponding to a scattering time of 26 fs at the Dirac point.
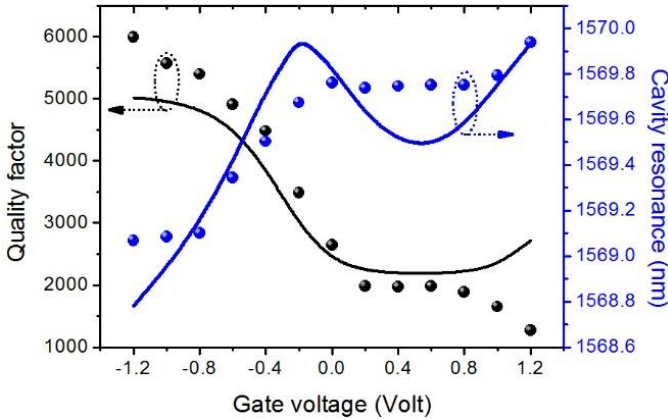
Figure 5.5: Quality factor and resonance wavelength versus gate voltage. Solid lines and scatter data represent the theoretical model and measurement data, respectively.

We also measured the gate voltage dependent resistance using the source and drain contact pads on both side of the graphene layer (**Figure 5.7**). A maximum resistance of 17 KΩ is measured for a gate voltage of 0.8 V, corresponding to the neutrality point. The slight difference in the voltage correspond to the neutrality point obtained from the optical data and from the resistance measurement is related to the error in the cavity resonance and quality factor fitting. Also, the result with the ionic gel are not always 100% reproducible.
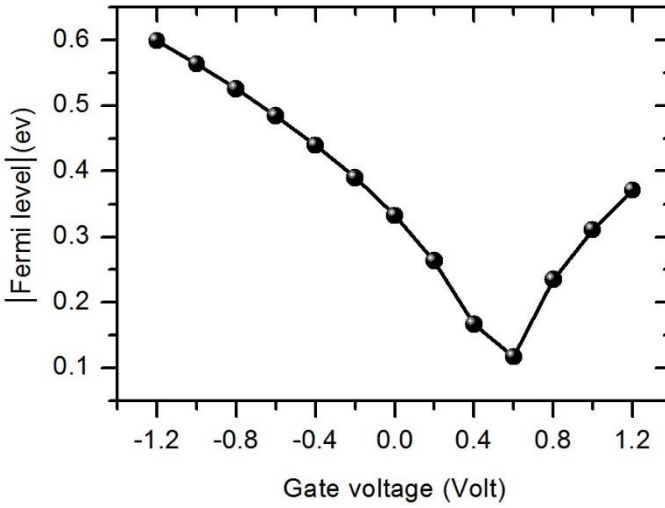
Figure 5.6: Fermi level versus gate voltage.
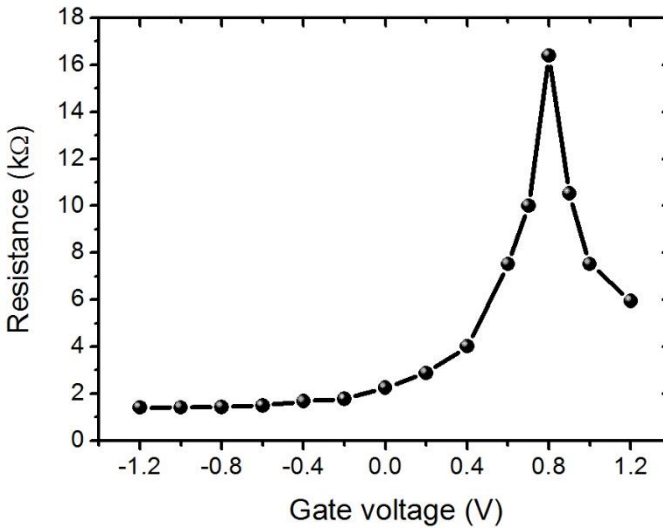
Figure 5.7: Resistance as function of gate voltage. The maximum resistance indicates the neutrality point, where graphene has minimum conductivity and minimum carrier density.

The current device exhibits an excellent *ER* but also a relatively large *IL*. To get insight in this trade-off and evaluate possible design improvements we used a model based on standard coupled mode theory [8]. The measured *Q*-factor can be written as:

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_g} + \frac{1}{Q_i} \qquad (5.4)$$

Q_i is related to intrinsic scattering losses of the cavity and found to be very large for the devices under study. Q_i will hence be neglected in the remainder of this discussion. Q_c is a design parameter and related to the strength of the mirror sections of the 1D PhC. Q_g is related to the absorption loss in the graphene layer and hence voltage dependent. To extract the actual values for Q_c and Q_g we fit the voltage dependent maximal transmission to the following model:

$$T(V) = \left| \frac{1/\tau_c}{j\Delta\omega + 1/\tau_c + 1/\tau_g(V)} \right|^2 \qquad (5.5)$$

in which τ_c and τ_g are cavity photon lifetimes corresponding to coupling loss and graphene loss, respectively. $T_{max}(V)$ is then calculated from

$$T_{max}(V) = \left| \frac{1/Q_c}{1/Q_c + 1/Q_g(V)} \right|^2 \qquad (5.6)$$

We find

$$Q_g(V) = 1/(\frac{1}{Q} - \frac{1}{Q_c}) \qquad (5.7)$$

and Q_g varies from about 1000 to 8000 for the voltage varying from +1.2 to -1.2 V (**Figure 5.8**). We also find $Q_c = 25600$ from the following equation

$$Q_c = Q/\sqrt{T_{max}(V)} \qquad (5.8)$$
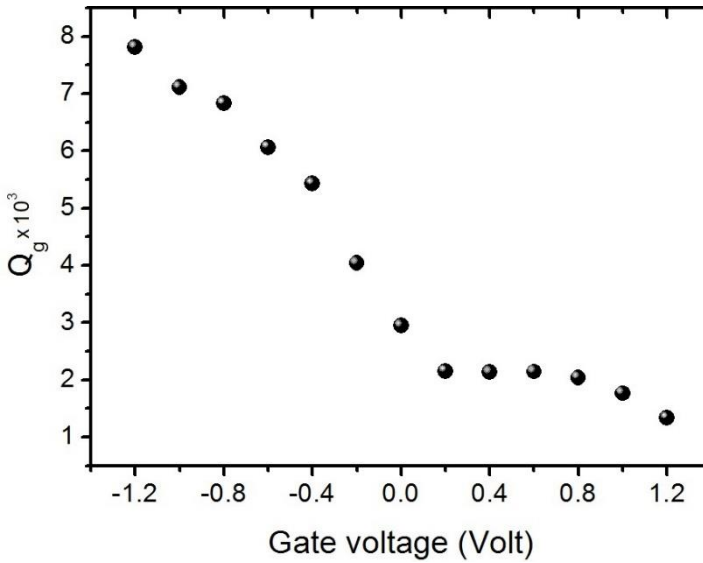
Figure 5.8: Q_g versus gate voltage.

Using the experimental data for $Q_g(V)$ we can now calculate how the *ER* and *IL* would vary for an optimized Q_c, using the model derived from coupled mode theory described above (equation 5.5). The results are plotted in **Figure 5.9**. One can observe that *ER* increases steeply for small values of Q_c but then remains almost constant for $Q_c > 2\times10^4$. The *IL* on the other hand continuously increases with Q_c. Therefore, the design of the cavity can be optimized by reducing the strength of the mirror section. E.g. for $Q_c = 3500$, it is possible to obtain a good *ER* ~ 10 dB while reducing the *IL* below 3 dB, taking into account the current quality of the graphene layer. Further improvements are expected for higher quality graphene.
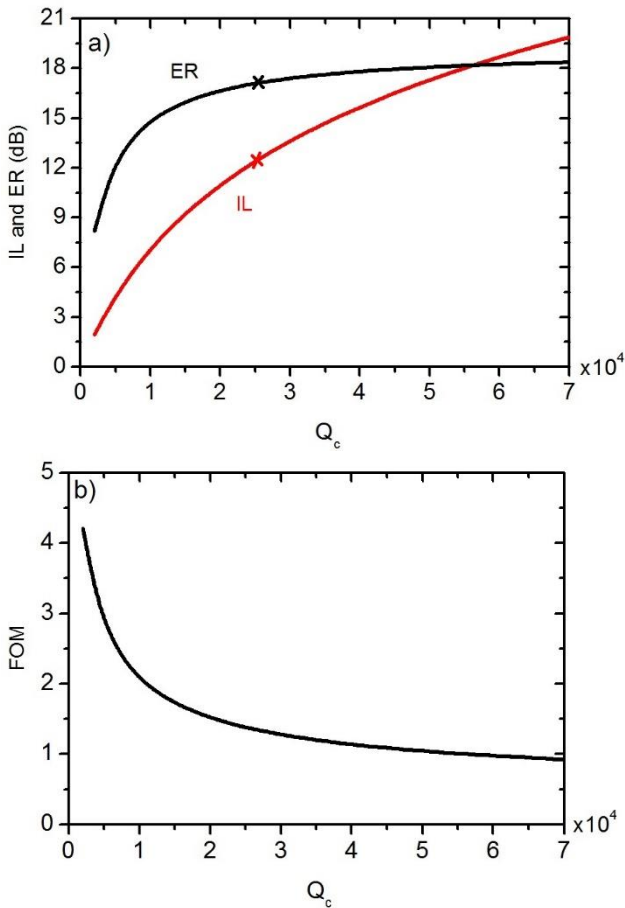
Figure 5.9: a) *ER* and *IL* versus Q_c calculated from the coupled mode theory. Black and red cross show the ER and IL for the current device. b) *FOM* (= *ER* over *IL*) versus Q_c.

To estimate the device energy consumption, the energy $E = CV^2/2$ required to charge (discharge) the graphene capacitor, where C is the device capacitance and V is the swing voltage can be calculated [2]. With the parameters obtained from fitting the cavity resonance and Q factor to the theoretical models, we find the electrolyte induces a capacitance density of 27 mF/m^2 on the graphene sheet. The graphene area is 5 μm^2, finally resulting in a switching energy of 97 fJ for a swing voltage of -1.2 V (equivalent with 17.2 dB extinction ratio).

5.3 Side-coupled cavity

5.3.1 Design and fabrication

In this section we present the results on the fabrication and characterization of the gated graphene on a side-coupled PhC cavity. Contrary to the front-coupled design, this device acts as a notch-filter. The main differences in the design of the side-coupled PhC compared to the front-coupled PhC are the width of the cavity, the length of the mirror sections and the size of holes. In addition, for this device only one metal pad was fabricated on the graphene layer to avoid overlapping of the second metal pad with the waveguide. The spacing between the metal contact and the side-coupled cavity is only 0.4 µm. Schematic of the design is illustrated in **Figure 5.10** and the design parameters are summarized in **Table 5.2**.
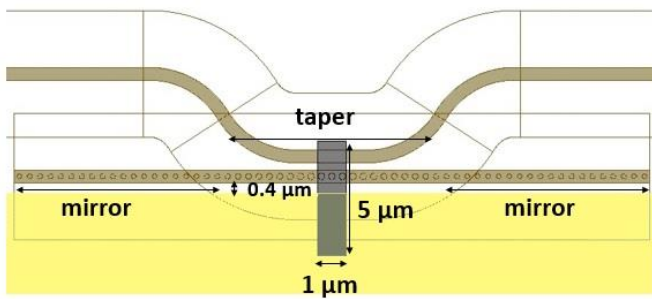
Figure 5.10: Schematic of the graphene-based switch showing the graphene layer on three central holes only and metal pads with 0.4 µm spacing from the side-coupled cavity.

Table 5.2: Design parameters of the side-coupled cavity.

Side-coupled cavity	Waveguide width (nm)	Coupling gap (nm)	Height (nm)
	456	250	220
Mirror section	Length (µm)	Hole diameter (µm)	Distance between holes (µm)
	7.66	0.168	0.198
Taper section: Hole	Length (µm)	Hole diameter (µm)	Distance between holes (µm)
1	7.3	0.176	0.193
2		0.186	0.183
3		0.196	0.174
4		0.204	0.166
5		0.210	0.158
6		0.216	0.152
7		0.220	0.147
8		0.224	0.142
9		0.226	0.139
10		0.228	0.137
11 (central hole)		0.228	0.136

Figure 5.11 is the microscopic image of the fabricated device, showing the source and the gate contacts on graphene.
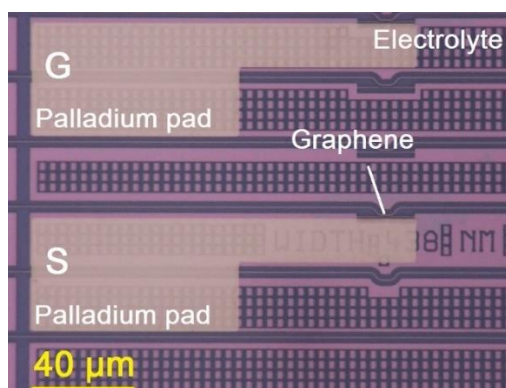
Figure 5.11: Top view of a fully fabricated device.

5.3.2 Characterization of the device performance

Similar to the previous device, the transmission was measured with different gate voltages. **Figure 5.12** shows the voltage dependent spectra of the device illustrating the shift of the resonance wavelength and also the change in the transmission with voltage. The transmission at 1560.9 nm, the wavelength of minimum transmission for an applied voltage of -1.2 V spectrum is extracted for all voltages from **Figure 5.12** and shown in **Figure 5.13**. As can be seen in this figure, an ER of 4.7 dB is obtained by applying -1.2 V. Increasing the drive voltage to 1.4 V (from -1.2 to 0.2 V), the ER increases to 7 dB but no further improvement in the ER was observed with increasing voltage (due to graphene intrinsic p-doping).
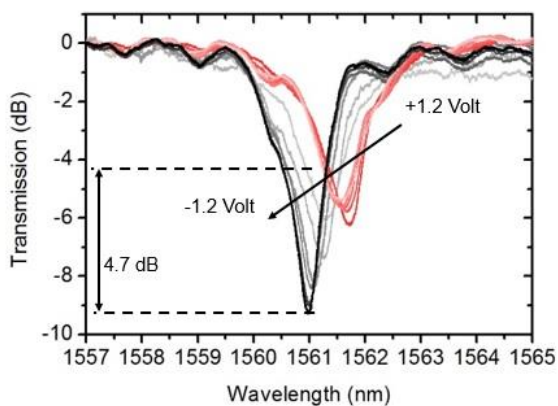
Figure 5.12: Transmission spectrum of the side-coupled cavity for different gate voltages.
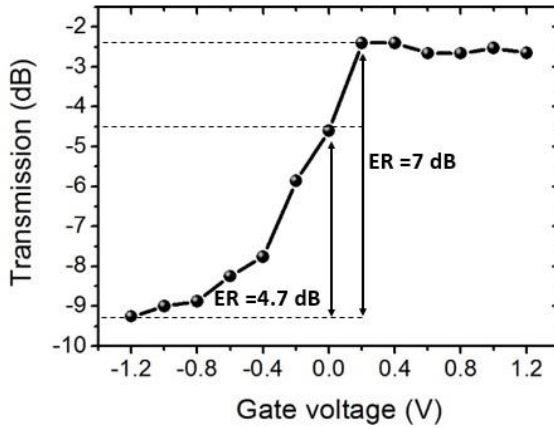
Figure 5.13: Transmission at the resonance wavelength of -1.2 V versus gate voltage for the graphene-integrated side-coupled cavity.

The quality factor and shift of the cavity resonance are extracted by fitting a Lorentzian function to the transmission spectra. We observed a *Q* factor increasing from 1000 to 1400 and a 0.7 nm shift in the cavity resonance. The theoretical data was calculated from the same model described in previous sections for the front-coupled cavity (**Figure 5.14**). Fitting the experimental data to the theoretical model gives us the following values for the different parameters $\alpha \sim 0.105$, $\beta \sim 0.3$, $C \sim 27$ mF/m^2, $n_b \sim 12e12$ cm^{-2} and $\Gamma \sim 26$ fs. From the fitting parameters of C and n_b, the fermi level is then calculated (**Figure 5.15**).
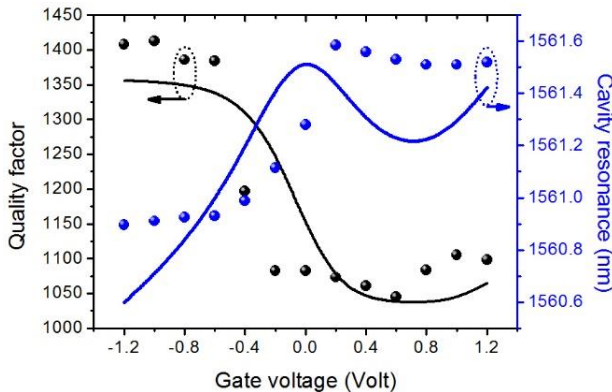
Figure 5.14: Quality factor and resonance wavelength versus gate voltage for the graphene-integrated side-coupled cavity. Solid lines and scatter data indicate the theoretical and measurement data, respectively.

Although the two presented devices in this chapter (front-coupled and side-coupled cavities) were fabricated on the same chip, the graphene fermi level in these two devices is slightly different. According to the fitting parameters extracted from the measured data, we observe the side-coupled cavity has a higher intrinsic carrier density ($12e12$ cm^{-2}) compared to the front-coupled cavity ($9e12$ cm^{-2}). This might be related to the difference in the fabrication of the metal pads. As we have already discussed, in the front-coupled cavity metal pads are fabricated on both sides of the graphene layer while in the side-coupled cavity the metal pad is on one side of graphene only. Therefore, one side of the graphene is unprotected during the process and might be contaminated by chemicals or particles resulting in higher graphene doping.
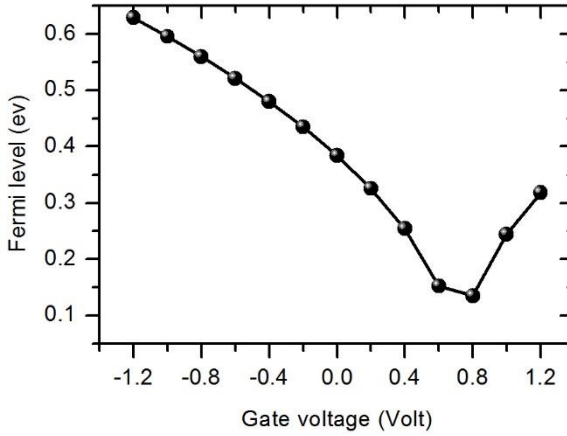
Figure 5.15: Fermi level versus gate voltage for the graphene-integrated side-coupled cavity.

Lastly, we calculated the *ER* and *IL* for a given Q_c in similar way as front-coupled cavity (**Figure 5.16**). The measured *Q*-factor can be written with the equation 5.2 with the same assumption for Q_i. Gate dependent minimum transmission (this device is a reflection based device and therefore the minimum transmission is important) can be fitted to the following equation

$$T_{min}(V) = |-1 + \frac{1/Q_c}{1/Q_c + 1/Q_g(V)}|^2 \tag{5.9}$$

Q_g and Q_c can be calculated as

$$Q_g(V) = 1/(\frac{1}{Q} - \frac{1}{Q_c}) \tag{5.10}$$

and

$$Q_c = Q/\left(1 - \sqrt{T_{min}(V)}\right) \tag{5.11}$$

We find Q_g varies from about 2000 to 4000 for the voltage varying from +1.2 to -1.2 V.

According to **Figure 5.16**, the IL for low Q_c is about 19 dB. Increasing Q_c reduces the IL to below 3 dB. However, the ER is also decreased to 5 dB. Beyond this point, it seems that the device figure of merit is not dependent on the design parameters.

As explained above, in this device the metal and cavity spacing is 0.4 µm. Increasing this spacing is one way to further improve the device performance. As we have already mentioned for the front-coupled device the graphene quality also is another effective parameter to obtain higher ER and lower IL.
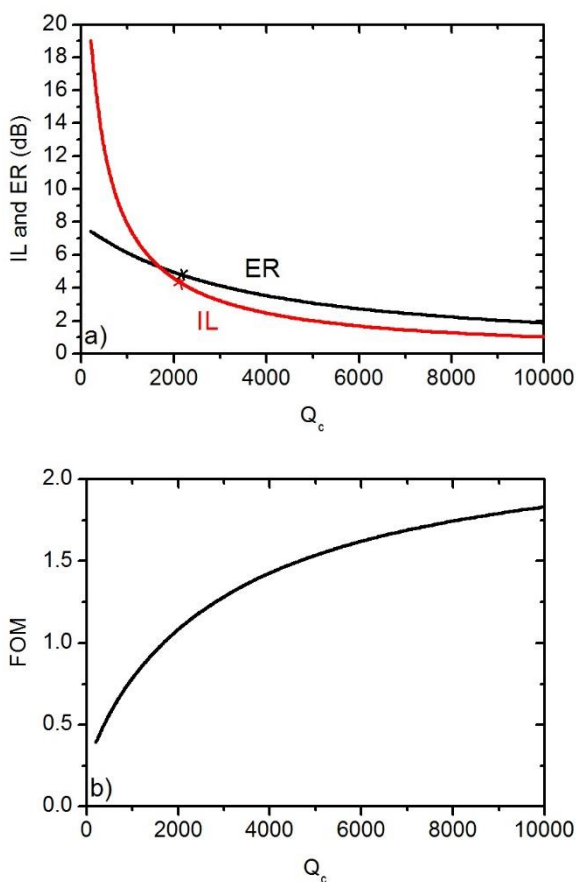
Figure 5.16: a) *ER* and *IL* versus Q_c calculated from the coupled mode theory for the graphene-integrated side-coupled cavity. Black and red cross show the ER and IL for the current device. b) *FOM* (= *ER* over *IL*) versus Q_c.

5.4 Conclusion

We fabricated a wavelength selective switch by integrating graphene with a 1D Si PhC cavity. Graphene was transferred using a new transfer printing method exploiting a commercial transfer printer. Next, we demonstrated switching of the hybrid graphene PhC device demonstrating an *ER* of 17 dB for a voltage swing of only 1.2 V for a gated graphene on the front-coupled cavity. In addition, a 0.75 nm shift in the cavity resonance and an increase in the *Q* factor from 2000 to 6000 were observed for the same device. The

experimental results were fitted to a theoretical model allowing us to extract the intrinsic parameters of the device. By combining these with a model based on coupled mode theory we predict how design improvement can result in an improved tradeoff between *IL* and *ER* for the device. Another important feature of the device is the small size of the graphene capacitor, offering potential for low power consumption and high speed operation. The same experiment was carried out on a side-coupled PhC cavity. An *ER* of 4.7 dB for a voltage swing of 1.2 V was demonstrated. A 0.7 nm shift in the cavity resonance wavelength was observed and the *Q* factor was increased from 1000 to 1400 by applying 1.2 V. Further investigation about the design improvement was carried out using the coupled mode theory and *ER* and *IL* were calculated for different Q_c. We noticed a $Q_c \sim 4000$ is the most suitable design parameter, but further enhancement in the device performance requires fabrication optimization including the better graphene growth and transfer.

References

[1] L. Abdollahi Shiramin, W. Xie, B. Snyder, P. De Heyn, P. Verheyen, G. Roelkens, D. Van Thourhout, "High Extinction Ratio Hybrid Graphene-Silicon Photonic Crystal Switch", submitted to PTL, 2017.

[2] A. Majumdar, J. Kim, J. Vuckovic, F. Wang, "Electrical Control of Silicon Photonic Crystal Cavity by Graphene", Nano. Let., 13, 2013.

[3] X. Gan, R. Shiue, Y. Gao, K. Fai Mak, X. Yao, L. Li, A. Szep, D. Walker, J. Hone, T. F. Heinz, D. Englund, "High-Contrast Electrooptic Modulation of a Photonic Crystal Nanocavity by Electrical Gating of Graphene", Nano. Let., 13, 2013.

[4] L. Abdollahi Shiramin, W. Xie, B. Snyder, P. De Heyn, P. Verheyen, G. Roelkens, D. Van Thourhout, "Electrically Tunable Absorption in Graphene-Integrated Silicon Photonic Crystal Cavity", accepted for publication in Group IV conference, 2017.

[5] V. Thareja, J. Kang, H. Yuan, K. M. Milaninia, H. Y. Hwang, Y. Cui, P. G. Kik, M. L. Brongersma, "Electrically tunable coherent optical absorption in graphene with ion gel", Nano. Lett, 15, 2015.

[6] M. Mohsin, D. Schall, M. Otto, B. Chmielak, S. Suckow, and D. Neumaier, "Towards the Predicted High Performance of Waveguide Integrated Electro-Refractive Phase Modulators based on Graphene", IEEE Photonics Journal, 9, 2016.

[7] G. W. Hanson, "Dyadic Green's functions and guided surface waves for a surface conductivity model of graphene," J. Appl. Phys., 103, 2008.

[8] S. Fan, W. Suh, J. D. Joannopoulos, "Temporal coupled-mode theory for the Fano resonance in optical resonators", J. Opt. Soc. Am. A, 20, 2003.

6

Double-layer graphene-based switch embedded in SiN waveguide

Contents

In this chapter, we will present results of an electro-optical device fabricated by embedding a double-layer graphene stack in a SiN waveguide, fabricated using the transfer printing method developed in chapter 4. First, we will present the process flow for the device fabrication. Next, the processing steps that have been developed to fabricate the designed structure will be discussed in detail. Then, the characterization results will be presented.

6.1 DLG-E-SiN electro-optical switch

As we derived in chapter 2, a device consisting of a double-layer graphene stack embedded in a SiN waveguide is of particular interest for its high performance, but also because of the wide transparency of SiN and because of using a deposited material, with possible cost savings with respect to crystalline silicon. The fabrication starts with the SiN photonic circuit design. The waveguide structures are designed at the Photonics Research Group based on simulation results (see chapter 2) and manufacturing is done at IMEC facilities using deep UV lithography and dry etching. After that, the post processing is performed on these waveguides in the Photonics Research Group's clean room. **Figure 6.1** is a schematic of the DLG-E-SiN electro-optic device whose fabrication is discussed in the following sections. The device consists of a double-layer graphene with a thin dielectric in between lying on a 300 nm SiN waveguide. It also includes a 300 nm SiN on top to make a symmetric structure and enhance the confinement of the electric filed in the graphene layers. The voltage is applied over the graphene layers through the metal contacts integrated with both graphene layers.
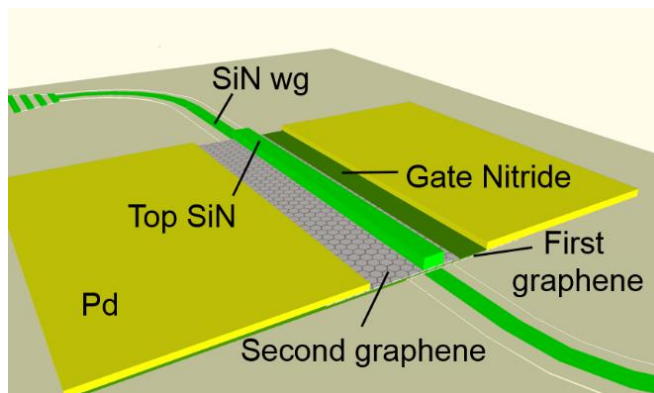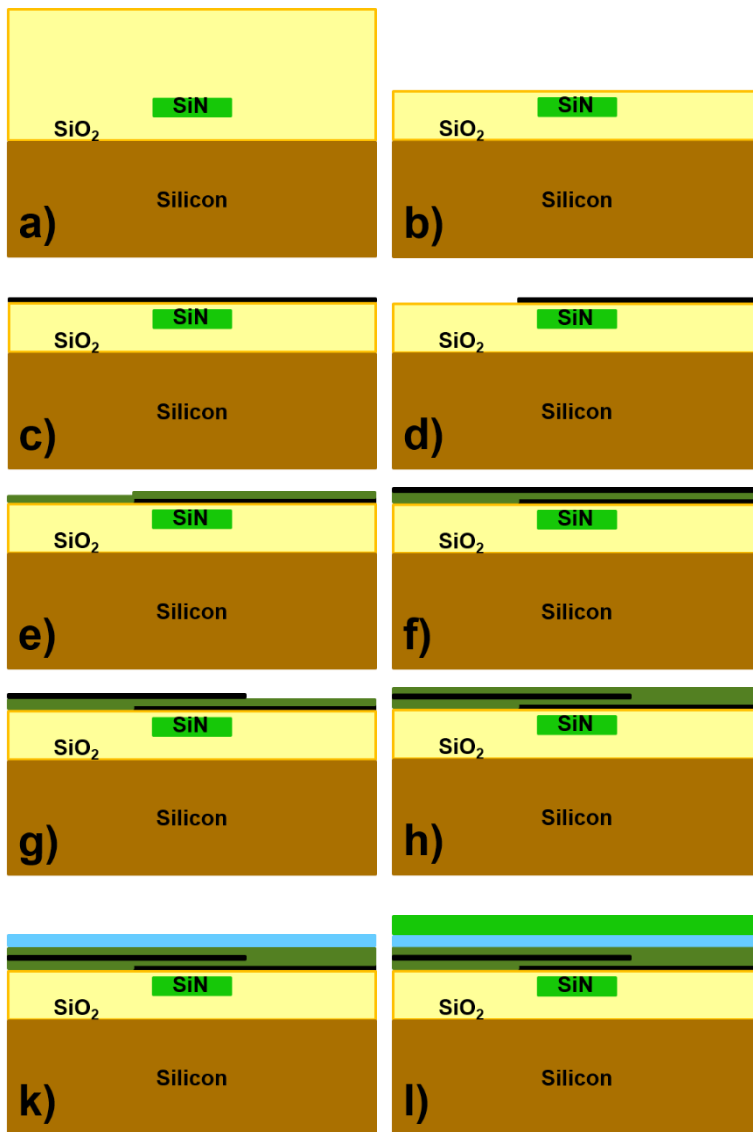
Figure 6.1: Schematic of DLG-E-SiN graphene-based switch.

6.2 Process flow

The outline of the fabrication process is shown in **Figure 6.2** and discussed in detail in the coming subsections.
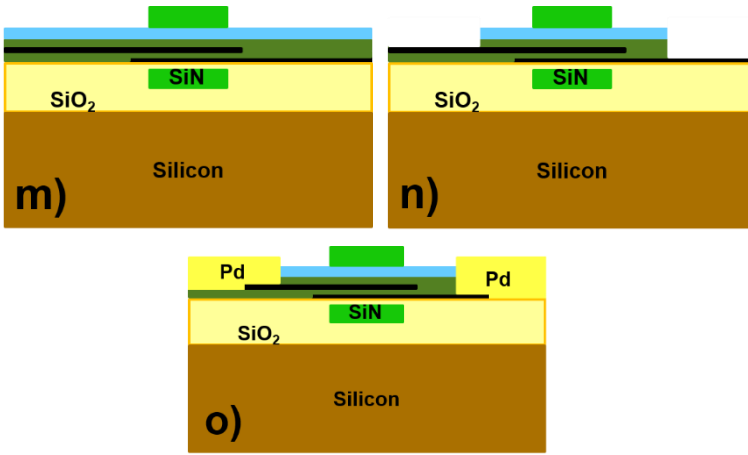
Figure 6.2: The process flow for fabrication of DLG-E-SiN. a) Sample received from imec with a 1 µm SiO$_2$ layer on top. b) Back etching SiO$_2$ and planarization of sample. c) Transferring the first graphene layer. d) Patterning the transferred graphene. e) Deposition of a 10 nm SiN film. f) Transferring the second graphene layer. g) Patterning the second graphene layer. h) Deposition of a 10 nm SiN film. k) Deposition of a 30 nm Al$_2$O$_3$ layer. l) Deposition of the top SiN. m) Patterning the top SiN waveguide. n) Opening vias on both graphene layers. o) Metallization and lift-off. Black color indicates the graphene layer, light green shows 300 nm SiN, dark green is 10 nm SiN gate and blue is Al$_2$O$_3$.

6.2.1 SiN waveguide planarization

In the MPW runs from IMEC the thickness of the top silicon oxide layer is fixed to 1 µm above the waveguide level, which is obviously too much for efficient coupling with a graphene layer. Therefore, the top silicon oxide layer should be etched back until the thickness of the silicon oxide layer is reduced to the desired thickness. First of all, an O$_2$ plasma cleaning process is performed on the SiN chips to remove particles and organic contaminants before the etch-back step. This is an important step as particles on the sample surface will work as an etch mask resulting in a non-uniform surface after etching.

For the SiO$_2$ etch back step there are two types of etching, wet and dry etching. **Figure 6.3** shows the SEM image of three samples after different etch-back processing techniques. In the wet etching, a 1:7 BOE solution and in the dry etching a combination of SF$_6$ and O$_2$ gasses were used.

The etch back with BOE seems to have teethed SiO$_2$ at the sides of waveguide [**Figure 6.3**(a) side view, (b) top view]. Similarly, the combination of the dry

and the wet etchings (etching 500 nm of SiO_2 with dry and 500 nm with the wet etching) shows an uncontrollable etching at the waveguide trenches and a full removal of the oxide film at the waveguide sides [**Figure 6.3**(c)]. On the contrary, dry etching with the RIE process appears to result in a more uniform surface and a controllable SiO_2 etching process [**Figure 6.3**(d)]. Hence, the etch-back with the dry etch is chosen to be used in the next processes in this thesis.

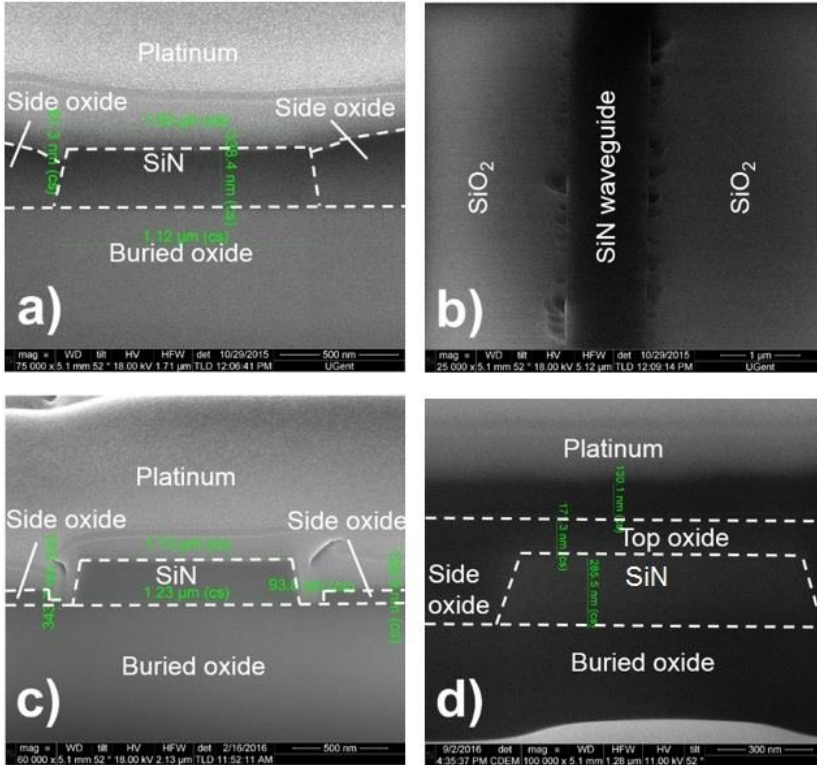**Figure 6.3:** Fib cross section of three samples a) Wet process side view. b) Wet process top view. c) Wet in combination with dry process. d) Dry process.

6.2.2 First graphene layer transfer and patterning

The second step of the DLG-E-SiN fabrication is to transfer the first graphene layer on the SiN waveguide using the transfer printing method discussed in chapter 4. After a lithography step, the transferred graphene coupon is

patterned with an O_2 plasma to obtain the desired width and length. Finally, the unexposed resist is removed with acetone.

6.2.3 SiN deposition-optimization

Our device is basically a capacitor that operates by applying a voltage between two electrodes. A dielectric film is required between both graphene layers to form this capacitor. According to previous works [1]-[6], a thin layer of Al_2O_3 deposited by ALD is a proper gate dielectric for graphene-based devices. In this work, we have used a nitride layer deposited through PECVD (a Vision 310 PECVD system from advanced vacuum) however, partly because it was the most readily available approach in the lab, partly because it fits well in the whole process flow, which is already relying on PECVD based SiN deposition for forming the top part of the waveguide.

The PECVD process is carried out with SiH_4 and NH_3 as the active precursors and Ar and/or N_2 as dilution gases. To minimize any possible damage to the graphene layer, the PECVD silicon nitride process should be optimized to obtain a low energy plasma. A high pressure and a large N_2 or Ar flow can be utilized to maximize collisions within the plasma and minimize the impact with the graphene surface [7]. The resultant plasma is relatively cold and mild. Under an optimized plasma density, the surface damage to graphene is minimized and a continuous growth of silicon nitride over graphene is ensured [7].

To find an optimized recipe for the nitride film deposition in PECVD, we investigated the impact of the plasma pressure, the deposition temperature and the flow of the diluting gasses. The N_2 flow was fixed to 1960 sccm in all experiments, the maximum that can be reached in our PECVD reactor. After deposition of SiN on the graphene/SiO_2/Si sample, the graphene quality was evaluated through Raman spectroscopy. The results are presented in **Figure 6.4**. In the first part of the experiment, the impact of the dilution gas was investigated. We used Ar and N_2 as a dilution gas with a pressure of 1000 mTorr and a temperature of 350 ºC. **Figure 6.4**(a) shows that the deposition process whereby we used a combination of Ar and N_2 results in the largest D band while the process with only Ar or only N_2 seems to be acceptable but requires further optimization. In the next part of the experiment, the SiN film was deposited using N_2 as the dilution gas. We used the recipe of N_2 1960 sccm, SiH_4 sccm 40, NH_3 40 sccm, power 20 W, temperature 350 ºC with the pressure of 500, 700 and 1000 mTorr. The interest in studying lower pressures is that 1000 mTorr is the maximum achievable pressure in our PECVD tool and it is preferred to avoid working at the limits. However, at lower pressures, next to a large D band, a large D' band is also observed. As seen in

Figure 6.4(b) the D and D' band become considerably smaller with increasing the pressure and I_{2D}/I_G notably improves. Therefore, 1000 mTorr was chosen as the best pressure value. Although the deposition at the temperature of 350 ℃ seems to result in a decent quality, we deposited a SiN film on another sample at a lower temperature for technical reasons (the PECVD tool cannot tolerate higher than 330 ℃). According to **Figure 6.4**(c) the deposition at 300 ℃ results in almost the same Raman spectrum as the one at 350 ℃. Therefore, 300 ℃ was chosen as the working temperature. The process has room for optimization to completely remove the small D and D' bands in **Figure 6.4**(c), but we were restricted by the limits of our tool.
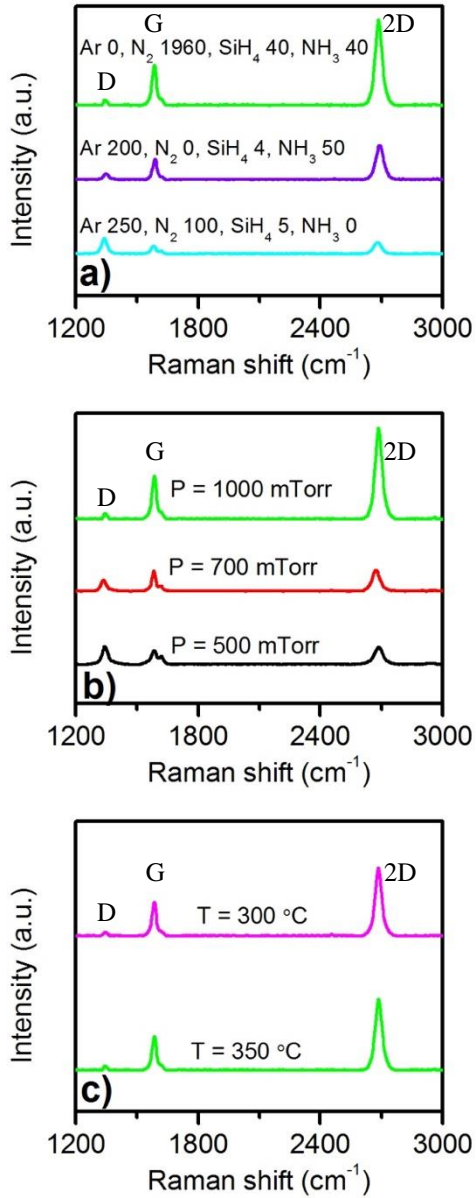
Figure 6.4: Raman spectra of the SiN-capped graphene. a) The dilution gas impact at 350 °C and pressure of 1000 mTorr. b) The pressure effect during PECVD deposition, with other parameters kept fixed, T = 350 °C. c) The temperature impact at optimized pressure of 1000 mTorr.

To assess the quality of the deposited SiN, an ellipsometry measurement was carried out on a SiN/SiO$_2$/Si stack (10nm/300nm/Si substrate) whereby the SiN layer was deposited with the optimized process as determined through Raman spectroscopy. From this measurement, the refractive index and the extinction coefficient of the deposited SiN at 350 °C were found to be 2.03 and 0.001 while at 300 °C they are 1.98, 0.0007 at 1550 nm. This measurement shows a reduced refractive index and therefore lower material density at the lower temperature. A decrease in the extinction coefficient is another observation in this experiment. Hence, a high temperature deposition is a desire to achieve a high density SiN. In this process, on the one hand the SiN layer needs to have a high density. On the other hand, a low loss SiN layer is needed to avoid excess insertion loss. We observed that these two parameters cannot be obtained with the same deposition temperature. Therefore, we opt to work at higher temperature to deposit a high density SiN layer. However, in our process, the deposition temperature was limited to 300 °C because of technical difficulties in the PECVD tool.

In summary, the best recipe for deposition of the PECVD SiN film on graphene in order to ensure a high density SiN layer and at the same time preserve the graphene quality is as follows: N$_2$ 1960 sccm, SiH$_4$ 40 sccm, NH$_3$ 40 sccm, power 20 W, pressure 1000 mTorr, temperature 300 °C, frequency 13.56 MHz.

6.2.4 Second graphene layer transfer and patterning

The second graphene layer is required to act as the second electrode of the capacitor and also to enhance the absorption in the device. This layer was transferred from the same source sample as prepared for the first graphene transfer. After the second transfer print process, the graphene layer is patterned and the resist is removed. **Figure 6.5** shows the image of the device after the second graphene patterning.
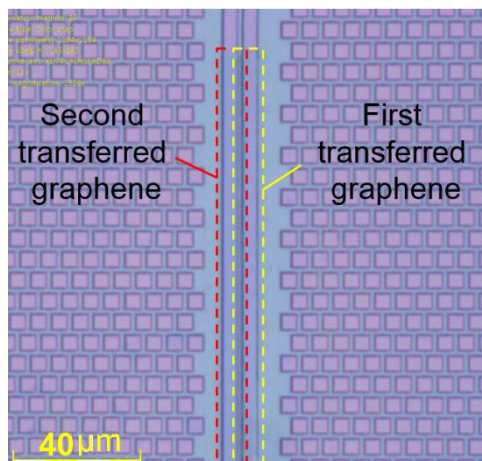
Figure 6.5: The SiN waveguide covered by two graphene layers with a 10 nm SiN dielectric spacer layer in between.

6.2.5 SiN and Al_2O_3 deposition on the second graphene layer

To etch the top SiN layer, a thin film of Al_2O_3 is deposited as an etch-stop layer to protect the graphene. The Al_2O_3 layer is deposited by E-beam evaporation. To avoid any damage to the graphene by the Al_2O_3 deposition, first we deposited a 10 nm SiN film with the optimized process derived in the previous sections. Next, a 30 nm Al_2O_3 film was deposited on the 10 nm SiN layer.

6.2.6 Top SiN deposition on Al_2O_3

After deposition of the etch-stop layer, the next step is to deposit the top 300 nm SiN layer. By deposition of this layer, the double graphene capacitor is sandwiched between two 300 nm thick SiN films.

6.2.7 Top SiN etching

To realize the desired waveguide structure, the final deposited SiN layer should be patterned aligned with the waveguide circuit underneath. In this stage, a standard positive lithography process was carried out to protect the part of the SiN layer where graphene layers have been transferred. The top SiN layer is then etched by RIE (SF_6, CF_4 and H_2). This step needs to be optimized to obtain smooth and low loss side walls. After etching, the photoresist is removed with acetone.

6.2.8 Via opening and metallization

The final step of the fabrication is the metallization. An image reversal lithography using AZ-5214 photoresist was carried out to open vias for both contacts. Now both the Al_2O_3 and SiN layers should be etched to have access to the graphene layer. Both are removed with a BOE solution. Subsequently, Pd was evaporated on the graphene layers. **Figure 6.6** is the microscope image of the fabricated devices after successful lift-off.
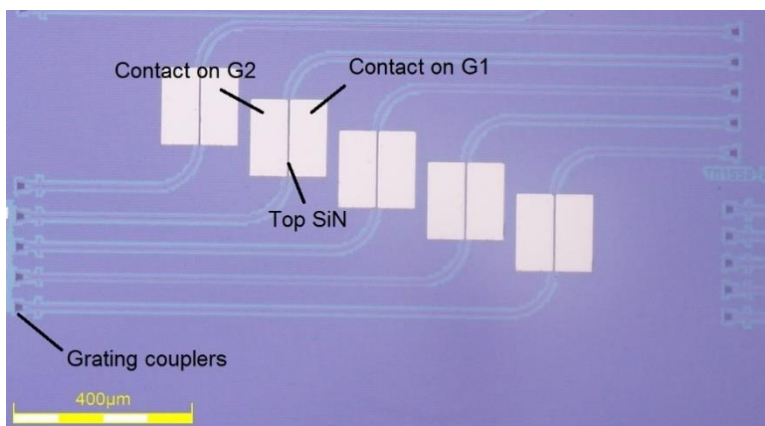

Figure 6.6: The microscope image of the fabricated graphene device. G1 and G2 indicate the first and second graphene layers, respectively.

6.3 Characterization of the fabricated DLG-E-SiN

During the device fabrication, the length dependent waveguide absorption of the device was measured step by step and summarized in **Figure 6.7**(a). The absorption is doubled after transferring the second graphene layer as expected, but it is lower than simulated data (see chapter 2) for both graphene layers. One reason for the lower absorption could be the thickness of the remaining oxide on the SiN waveguide. A thick SiO_2 on the waveguide, results into a reduced interaction of light with the graphene and thus a lower absorption. Another observation in **Figure 6.7**(a) is the extra loss (about 10%) caused by the 10 nm SiN layer between two graphene layers as it can be predicted from the ellipsometry data. In addition, we measured the absorption after fabrication of the full device including etching of the top SiN. As shown in **Figure 6.7**(b) the fabrication of top SiN induces a high loss. This loss is at least partly related to the low coupling efficiency between the 300 nm and 600

nm thick SiN waveguides. An improved device would have a tapered top SiN layer but its fabrication would require E-beam lithography.
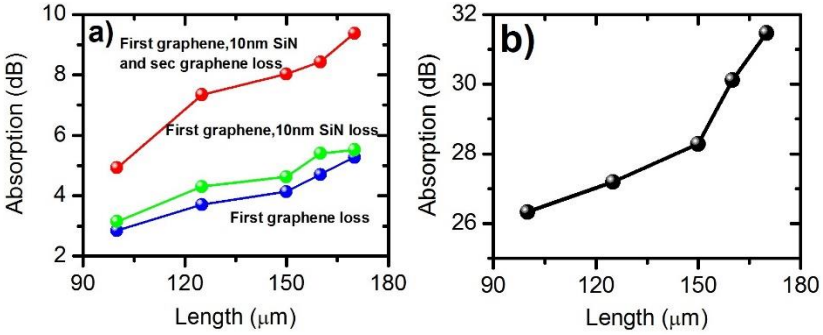

Figure 6.7: a) Absorption of a single layer graphene, SiN dielectric layer and double layer of graphene on the SiN waveguide b) Absorption after full device fabrication. The waveguide width is 800 nm.

Figure 6.8 plots the measured transmission versus the applied voltage between both graphene layers for devices with lengths of 100, 125, 150, 160, 170 µm at 1580nm (best coupling efficiency for the TE-grating coupler). The maximum extinction ratio observed in these devices is 3.5 dB for the device with the length of 150 µm at a gate voltage of 10 V. The neutrality point (maximum absorption) in these devices varies between V=0 and V=5 V.
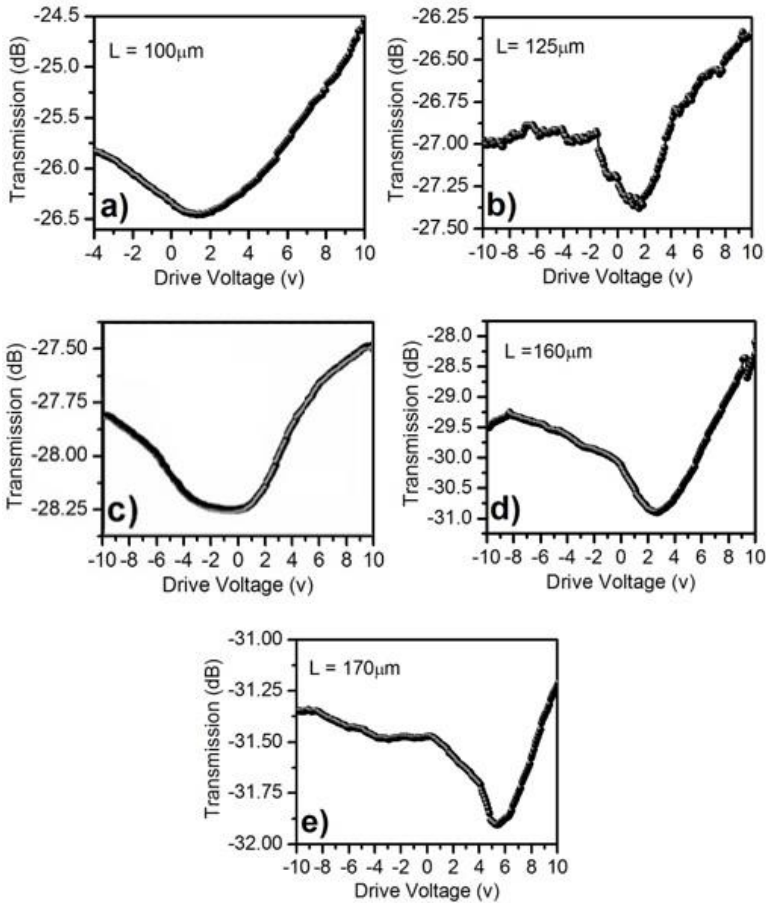
Figure 6.8: Transmission versus applied voltage for the devices with length of a) 100 µm. b) 125 µm. c) 150 µm. d) 160 µm. e) 170 µm.

The measured extinction ratio in these devices is lower than the values predicted from simulation (See chapter 2). The main reason might be a high leakage of the gate dielectric layer. **Figure 6.9** shows the leakage current versus applied voltage for the same devices. It is obvious that after applying only a few volts, the SiN-gate starts to pass a high current and in some cases breakdown occurs. Therefore, improvement of the device will require a higher quality gate dielectric deposited by ALD.
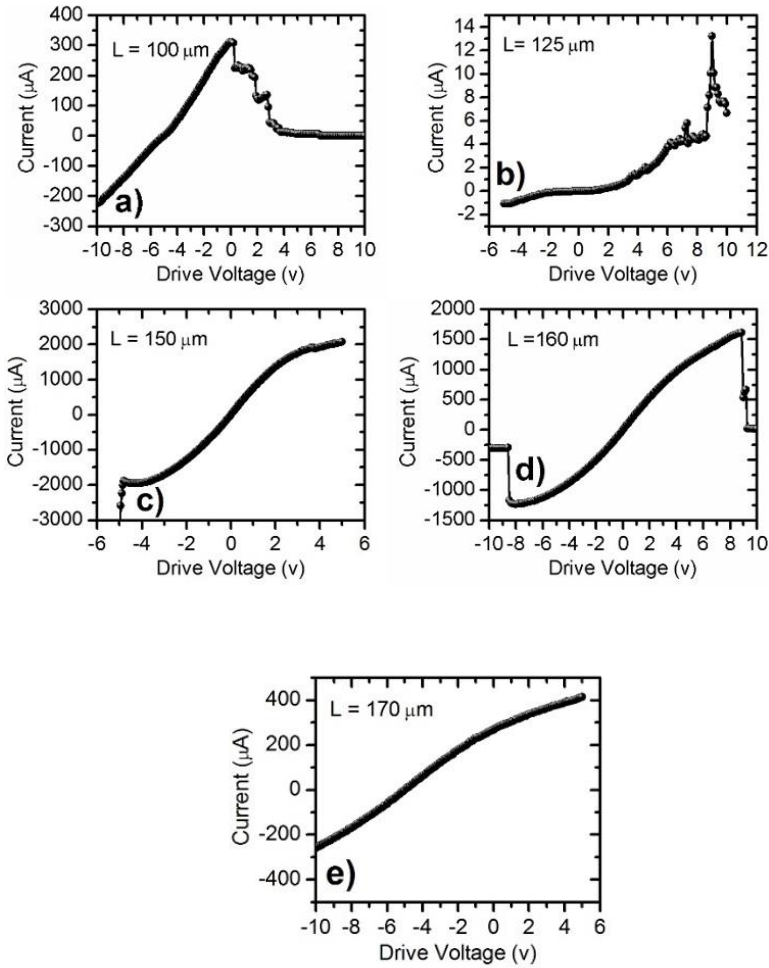
Figure 6.9: Current versus applied voltage for the device lengths of a) 100 µm. b) 125 µm. c) 150 µm. d) 160 µm. e) 170 µm.

6.4 Conclusion

In this chapter, we demonstrated a double-layer graphene-based switch embedded in a SiN waveguide fabricated using the novel transfer printing method developed in chapter 4. Since, a gate dielectric is required to form the capacitive stack from both graphene layers, we first optimized the deposition of SiN on graphene. This optimization minimizes the damage to the graphene layer, as evaluated through Raman spectroscopy. For the fabrication of the

device, graphene layers were transferred on the SiN waveguide using the transfer printing process developed in chapter 4. Further, the voltage dependent transmission was measured after full fabrication of the device. The maximum extinction ratio achieved in these devices (3.5 dB) is obtained for a device with 150 µm length at 1580 nm wavelength. Though Raman spectroscopy and loss measurement confirmed the deposited SiN has limited impact on the quality of the graphene layer, the device showed a high leakage current and low breakdown voltage. Hence, a high quality ALD layer such as Al_2O_3 or HfO_2 is suggested to be used in future devices. We propose to deposit these layers before transfer printing the graphene coupons, thereby reducing the processing complexity and protecting the graphene from environmental influences [8].

References

[1]   M. Liu, X. Yin, and X. Zhang, "Double-layer graphene optical modulator," Nano lett, vol. 12, no.3, pp. 1482-1485, 2012.

[2]   H. Dalir, Y. Xia, Y. Wang, and X. Zhang, "Athermal Broadband Graphene Optical Modulator with 35 GHz Speed," ACS Photonics,. vol. 3, no. 9, pp. 1564–1568 2016.

[3]   C. T. Phare, Y. Daniel Lee, J. Cardenas and Michal Lipson, "Graphene electro-optic modulator with 30 GHz bandwidth", Nature photonics, 9, 511-514, 2015.

[4]   S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric", Appl. Phys. Lett, 94, 062107, 2009.

[5]   L. Liao, J. Bai, Y. Qu, Y. Huang and X. Duan, "Top-Gated Graphene Nanoribbon Transistors with Ultra-Thin High-*k* Dielectrics" Nanotechnology, 21, 15705, 2010.

[6]   C. C. Lu, Y. C. Lin, C. H. Yeh, J. C. Huang and P. W. Chiu, "High Mobility Flexible Graphene Field-Effect Transistors with Self-Healing Gate Dielectrics", ACS Nano, 6, 4469–4474, 2012.

[7]   W. Zhu, D. Neumayer, V. Perebeinos, P.A. Zhu, "Silicon Nitride Gate Dielectrics and Band Gap Engineering in Graphene Layers," Nano Lett, Vol. 10, 3572-3576, 2010.

[8]   A. A. Sagade, D. Neumaier, D. Schall, M. Otto, A. Pesquera, A. Centeno, A. Elorzab and H. Kurz, "Highly air stable passivation of graphene based field effect devices", Nanoscale, 2014.

7

Conclusions and perspectives

Contents

7.1 Conclusions

This work aimed to develop the methods to design, fabricate and characterize graphene-based optical devices. To address this goal, in chapter 2 optimized designs for graphene-based modulators and switches were derived from simulation. These devices relied either on Si or on SiN waveguide platforms operating in the communication bands (wavelength regions 1310 nm and 1550 nm). In chapter 3, the basic processing steps for the fabrication of graphene-based devices such as graphene patterning and metallization on graphene were discussed. Moreover, several TLM configurations were presented and used to investigate how contact resistance and graphene sheet resistance depend on the contacting approach. In chapter 4, micron-size graphene transfer printing with a commercial automated transfer printer was presented. The loss characterization, resistivity measurement and Raman spectroscopy confirmed the quality of the transferred graphene. In chapter 5, a graphene-based optical switch was fabricated by the integration of a graphene layer on Si PhC cavities using the developed transfer technique. A high extinction ratio of 17 dB and 4.7 dB were measured with a front-coupled and side-coupled PhC cavity, respectively. Further design improvement was investigated by fitting the experimental results to a theoretical model. Another device demonstrated

using the developed transfer technique is a double-layer graphene embedded in the SiN waveguide. The processing steps and characterization of this device were provided in chapter 6. We observed 3.5 dB extinction ratio by applying 10 V DC voltage between both graphene layers. Several suggestions to enhance the device performance were presented.

7.2 Perspectives

To exploit the full potential of the graphene technology for optical interconnects, other aspects including optimization and exploring new techniques can be studied.

While the transfer printing technique developed in this thesis was limited to the transfer of un-capped graphene, the extension of this method to transfer of encapsulated graphene on a target substrate is to be developed. The importance of this work relies in the need for a clean graphene surface to enhance the device performance including the contact resistance, extinction ratio and insertion loss. The main challenge of this idea is to be able to deposit a high quality ALD dielectric on graphene, so that during the under-etching step with the BOE solution, the ALD layer is not etched away.

Another aspect to be investigated is the transfer of encapsulated graphene layers from the original growth substrate such as copper foil. The encapsulated graphene can be then used for the device fabrication. For example, in the double-layer graphene embedded in the SiN waveguide the encapsulation layer (ALD Al_2O_3 or HfO_2) can act as a dielectric between two graphene layers and facilitate the fabrication process of these devices and enhance the device performance.

Following the graphene process optimization, the next step can be integration of the hybrid graphene waveguide devices with III-V-on-Si heterogeneous lasers. Since graphene is not a gain material it cannot generate light and it requires to be integrated with other materials. Here we present our initial results for a DFB laser integrated with a graphene-based switch on the laser's taper section. In this device graphene has been transferred before coating the BCB bonding layer. After fabrication of the laser, vias are opened on graphene and the n-contact layer of the laser for metallization. Microscope images of the device from the different processing steps are shown in **Figure 7.1** and **Figure 7.2**. A SEM image of the taper cross section is also shown in **Figure 7.3**. The measurements were carried out on a temperature-controlled stage at 20℃. The laser optical spectrum and the L-I-V curve are shown in **Figure 7.4**. The SMSR is 32 dB. The laser threshold current I_{th} is 35 mA and a waveguide coupled optical output power of 4 mW is obtained at a drive current of 90 mA. The series resistance of the device is 6 Ω. In addition,

graphene device with the length of 150 µm on the taper shows 1 dB extinction ratio. Unfortunately, we observed a high leakage current through the BCB layer which serves as the gate dielectric between graphene and n-InP (**Figure 7.5**). Hence, considerable device improvement is predicted through deposition of a thin layer of a high quality dielectric, e.g. through ALD, in the gate stack. This idea can be further extended and form the basis for realizing semiconductor mode-lock lasers, whereby graphene is exploited as a saturable absorber.
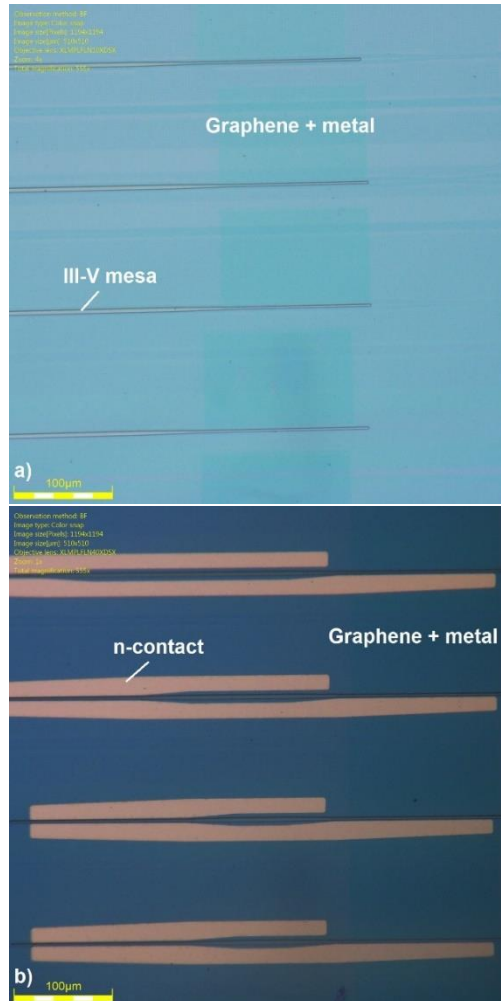

Figure 7.1: Microscope images of the device a) Definition of the III-V mesa showing the sample after QW etching with piranha. b) n-contact definition. In both images the trace of graphene and its protection metal is visible.
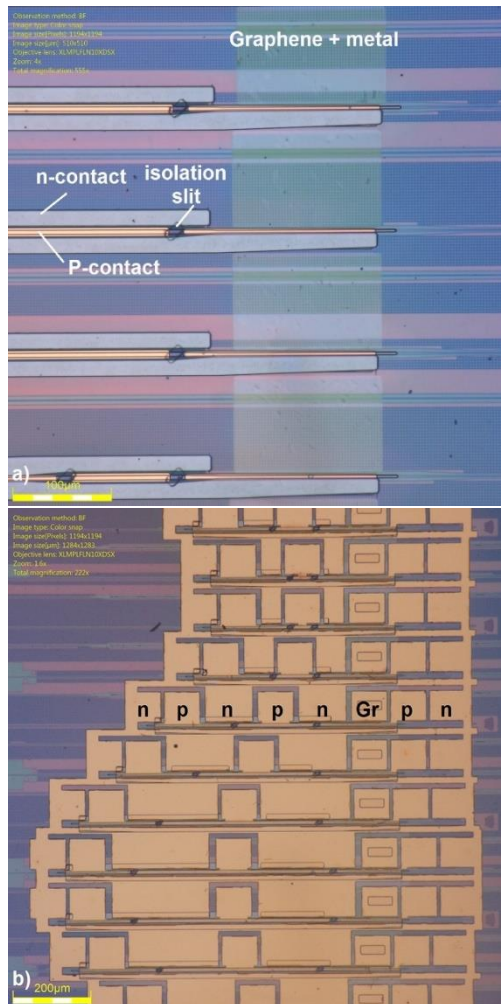
Figure 7.2: Microscope images of the device a) Definition of p-contact. b) Image of the sample after the final pads metallization and lift-off.
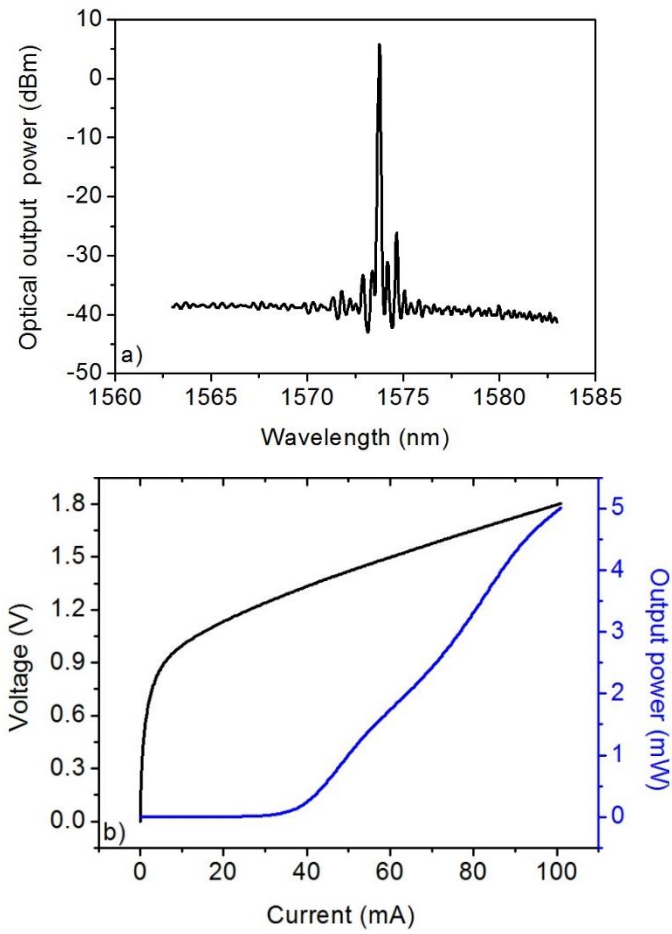
Figure 7.3: SEM image of the taper cross section. Black dashed line indicates the graphene layer.

Figure 7.4: a) DFB spectrum. b) LIV curve of the device (waveguide-coupled single facet output power).
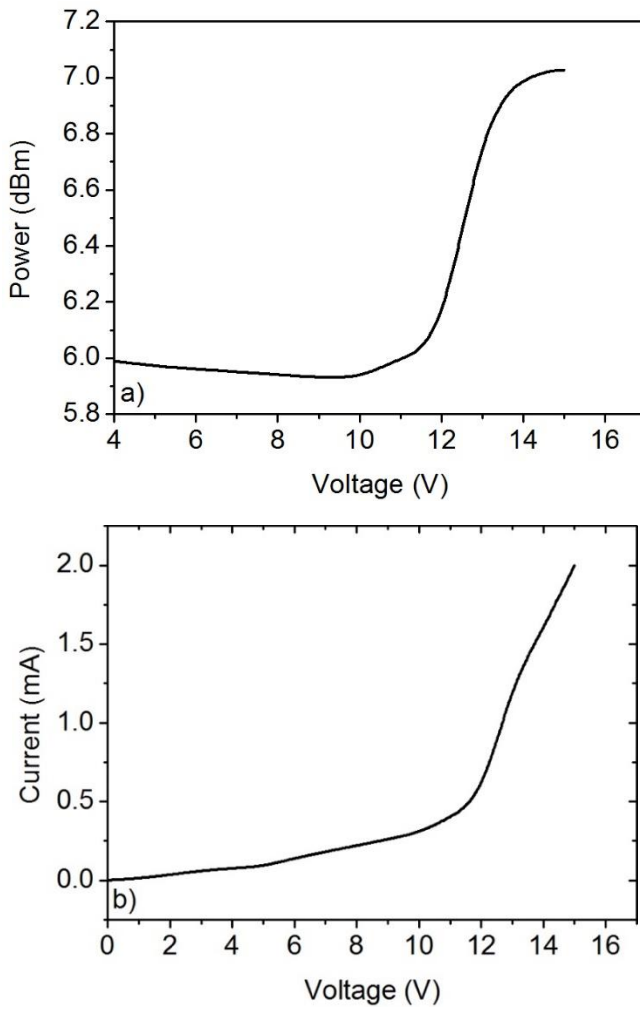
Figure 7.5: a) Voltage dependent output power of laser. b) I-V curve of graphene-based modulator.