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Adhesive Bonding of InP/InGaAsP Dies to Processed Silicon-On-Insulator Wafers using DVS-bis-Benzocyclobutene

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The process of bonding InP/InGaAsP dies to a processed silicon-on-insulator wafer using sub-300 nm layers of DVS-bis-benzocyclobutene (BCB) was developed. The planarization properties of these DVS-bis-BCB layers were measured and an optimal prebonding die preparation and polymer precure are presented. Bonding quality and bonding strength are assessed, showing high-quality bonding with sufficient bonding strength to survive postbonding processing.
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Silicon-on-insulator (SOI) is a material system that is gaining importance in semiconductor electronics industry for low power and high performance operation. Also in integrated optics it is an emerging technology platform. This is due to the fact that the refractive index contrast between the silicon waveguide core and the SiO_2 cladding is high ($\Delta n \cong 2$). This allows making very compact integrated optical functions leading to large-scale integration of optical functions. Moreover, these optical components can be fabricated using standard complementary metal oxide semiconductor (CMOS) technology, improving the yield, reliability, and economy of scale.[1] Although silicon is an interesting material for passive optical functions (optical filters, waveguiding, etc.) above 1.1 μm, where the material is transparent, it has an indirect bandgap and therefore is an inefficient light emitter. In order to integrate both active optical functions (laser emission, amplification, detection) and passive optical functions, III-V semiconductors with a direct bandgap need to be integrated on top of the passive SOI waveguide circuits. We focus in this paper on the integration of InP/InGaAsP heterostructures emitting at 1.55 μm on top of silicon-on-insulator waveguide circuits by means of a die to wafer bonding process, as shown in Fig. 1. Unprocessed InP/InGaAsP dies are bonded with its epitaxial layers down onto a processed SOI waveguide wafer, after which the InP substrate is removed. After substrate removal, the optoelectronic components can be fabricated in the bonded epitaxial layer.

Integration of two different material systems by means of a wafer bonding process can be done either using direct molecular bonding or adhesive bonding. Direct molecular bonding[2] relies on the van der Waals interaction between both surfaces. As this is a short-range force, sub-nm rms roughness of the surfaces is required.[3] Although this is obtainable on unprocessed SOI wafers using chemical-mechanical polishing (CMP)—and is the preferred way to fabricate SOI layer stacks—it is more difficult to obtain on the processed SOI waveguide circuits and on epitaxially grown InP/InGaAsP substrates. Therefore, in this work adhesive bonding was chosen to bond the III-V epi-structures on top of SOI waveguide circuits. One of the main advantages of adhesive bonding is that the surface quality that is required for bonding is less stringent as the polymer wets the surface and fills the troughs of the surface. It is also tolerant to particle contamination to some extent, and the topography of the surfaces to be bonded can be planarized by spin coating. Moreover, adhesive bonding processes are typically low-temperature processes, thereby reducing the stress due to the difference in thermal expansion of both materials. However, for the moment, little is known on the temperature stability and long-term stability of the bonding interface. It is also recognized that adhesive bonds are not hermetic seals.[4]

In literature, both thermosetting (spin-on glass,[5] polyimide,[6] benzocyclobutene,[6] etc.) and thermoplastic (PMMA,[7] SU-8,[8] etc.) polymers for adhesive bonding are described. For bonding using thermoplastic polymers, the post-bonding thermal budget is limited, which is a problem for the fabrication of the III-V devices after bonding. For our application, 1,3-divinyl-1,1,3,3-tetramethyldisiloxane-bisbenzocyclobutene (DVS-bis-BCB) was chosen as a bonding agent. It has a low curing temperature (250°C) and a high glass transition temperature (350°C). The curing reaction starts by thermal opening of the benzocyclobutene, which undergoes a Diels-Alder reaction with other available DVS-bis-BCB molecules to form a three-dimensional network. No byproducts are created during curing, and shrinkage upon cure is small (<5%), which is advantageous for adhesive bonding.[6]

Depending on the application, different bonding layer thicknesses are desired. In this application, where optical coupling needs to occur between the III-V active device and an SOI waveguide, ultrathin bonding layers below 300 nm are needed.[9] These thin bonding layers are also advantageous to reduce the thermal resistance of the active III-V devices as adhesives typically have a low thermal conductivity (k_{BCB} = 0.3 W/mK).[10]

DVS-bis-BCB Adhesive Die to Wafer Bonding Process

Commercially available B-staged DVS-bis-benzocyclobutene (Cyclotene 3022-35 from Dow Chemicals) was diluted using mesitylene (1,3,5-trimethylbenzene) to spin-coat ultrathin BCB layers. The thickness of Cyclotene 3022-35 diluted with 150% of mesitylene is shown in Fig. 2.[11] It was shown that defect-free films down to a few tens of nanometers in thickness can be obtained by simple solution casting.[12]

We evaluated the planarization properties of the ultrathin DVS-bis-BCB layers on the SOI waveguide topography. The height of the topography is 220 nm while the density of the features varies over the wafer surface. Three different types of topography were investigated: 10 μm wide trenches on a pitch of 30 μm (topography A), 10 μm wide trenches on a pitch of 120 μm (topography B), and an isolated step in the topography. Preliminary measurements showed that spin coating of multiple layers with the same aggregate thickness of a single layer showed significantly better planarization properties than single-step spin coating. Therefore, we assessed the degree of planarization by using a double coating obtaining a total layer thickness of about 300 nm. Different combinations of spin coating and curing were tried and the degree of planarization was measured as shown in Table I.

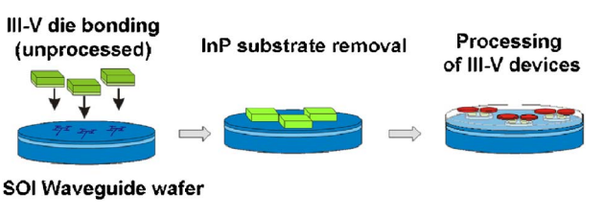

Figure 1. (Color online) Heterogeneous integration of InP/InGaAsP on top of an SOI waveguide wafer by a die to wafer bonding process.

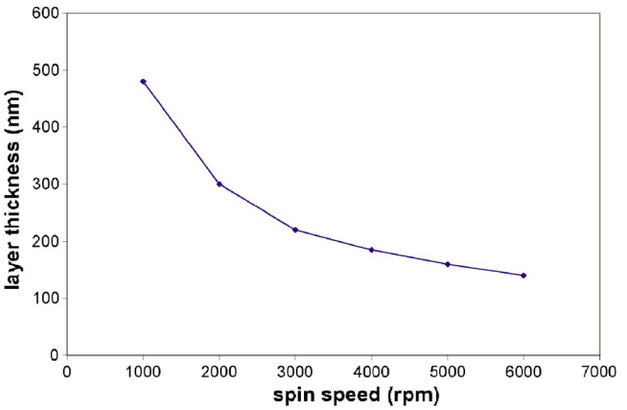

Figure 2. (Color online) Thickness of 2DVS-bis-BCB:3Mesitylene as a function of spin speed.

From these measurements, several conclusions can be drawn. First, it is clear that the planarization of the 30 μm pitch features is better than that of the 120 μm features. Second, the superior planarization properties of double spin-coated layers is clear: in the case of a 30 μm pitch, even a higher degree of planarization can be obtained using an aggregate 300 nm BCB layer than with a single 760 nm thick BCB layer. The type of curing of the first spin-coated layer also plays a role. Soft-curing the BCB by slowly (1.6°C/min) ramping to 210°C (indicated by "ramped" in Table I) gives a higher degree of planarization than a rapid thermal anneal (2 min at 250°C) due to the reflow of the BCB in the case of slow ramping.

The planarizing properties of the spin-coating process can be better understood by treating the resulting topography after spin coating as the output of a low pass filter with the original topography function as an input. Measuring the topography on an isolated step after spin coating gives the step response of the filter and thereby its filter characteristic in the spatial frequency domain. This filter function is plotted in Fig. 3 for the case in which the first layer (150 nm) is slowly cured and the second layer (150 nm) is cured using rapid thermal annealing, together with an overlay of the original topography function and the planarization result of a topography containing 10 μm trenches both on a 30 and 120 μm pitch. A local degree of planarization of 90 and 70%, respectively, is obtained, which is consistent with the measured degree of planarization in Table I.

From these results, we designed the SOI topography to obtain a degree of planarization higher than 90% (meaning a residual nonplanarity below 20 nm). This residual nonplanarity can than be compensated for by the elastic deformation of the InP wafer and the partially cured DVS-bis-BCB. This can be achieved by adding dummy structures to the functional components in order to get a sufficient high-frequency content of the topography according to Fig. 3.

The optimum degree of polymerization of the DVS-bis-BCB layer prior to bonding was evaluated by bonding unprocessed flat wafer surfaces. A layer of 300 nm BCB was spin-coated on a Pyrex

Table I. Degree of planarization of thin DVS-bis-BCB layers on different types of topography.

	Top. A	Top. B
150 nm BCB (ramped)	0.84	0.66
150 nm BCB (ramped) + 150 nm BCB (ramped)	0.95	0.8
150 nm BCB (ramped) + 150 nm BCB (RTA)	0.91	0.75
Thick BCB layer	0.925 (760 nm)	0.945 (1 μm)

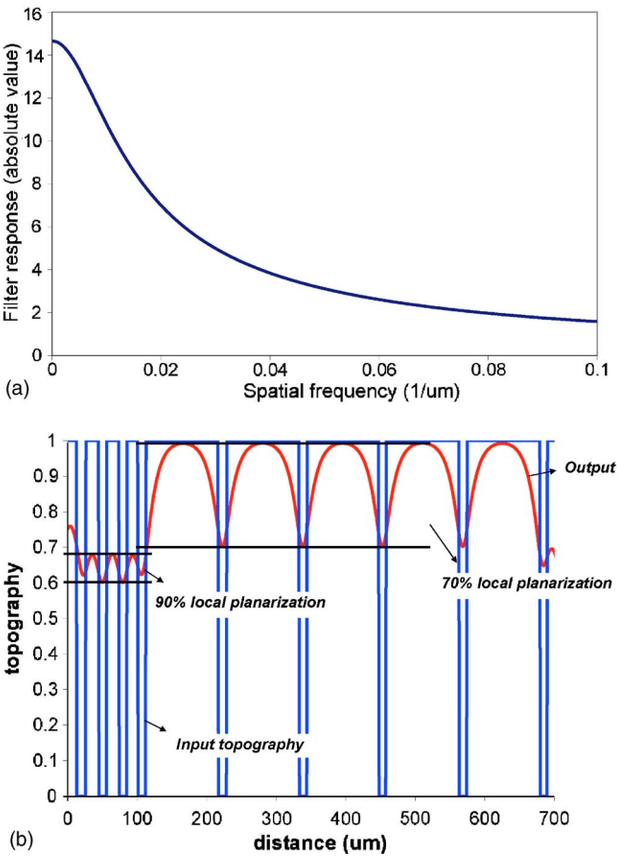

Figure 3. (Color online) Transfer function of the spin coating process (a) and resulting planarization simulation (b).

host wafer and placed on a hot plate in a nitrogen environment at 250°C to evaporate the mesitylene solvent and partially cure the BCB. The degree of polymerization vs time is depicted in Fig. 4.[13] Subsequently InP dies were bonded (using a process that is described later) and the wafer stack was cured at 250°C for 1 h. The bonding quality was assessed by optical inspection through the Pyrex substrate. When the degree of polymerization of the DVS-bis-BCB is too high, it is not tacky any more and the bonding fails. When the BCB is still liquid, attaching the InP dies can puncture the

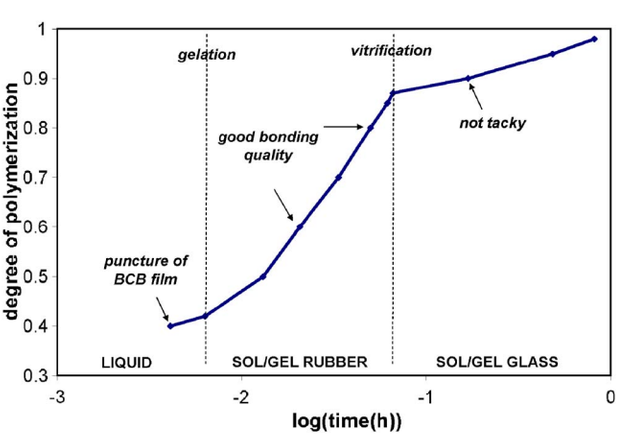

Figure 4. (Color online) Degree of polymerization vs time at 250°C (Ref. 13) and the relation with the quality of the bond.

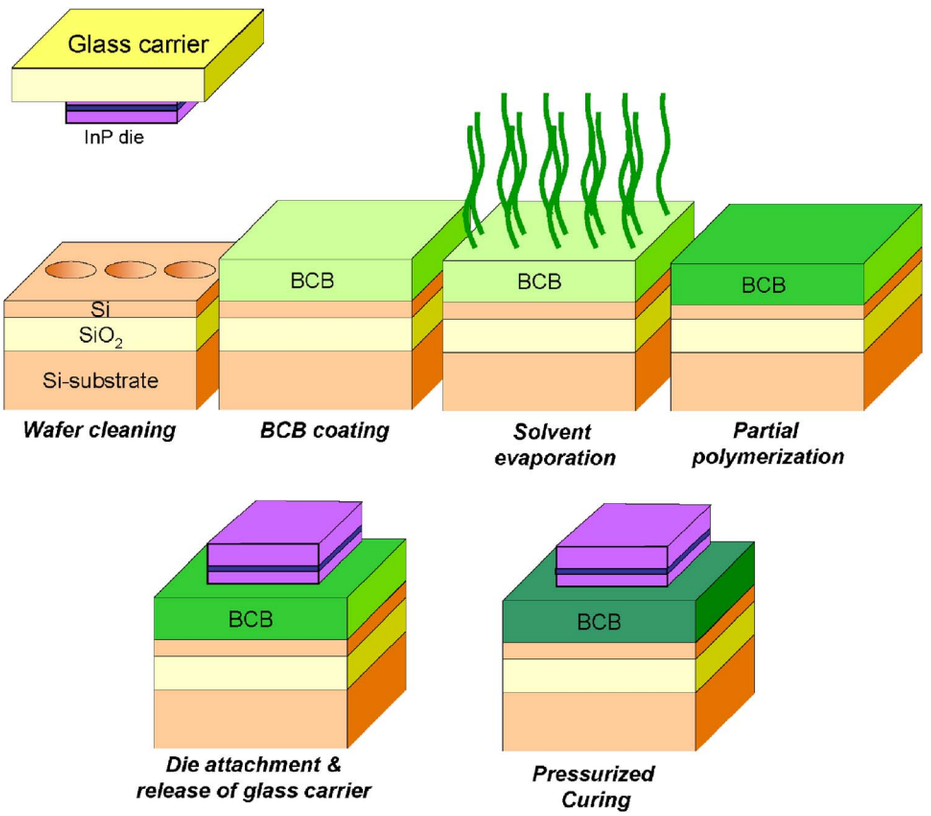

Figure 5. (Color online) Overview of the InP/InGaAsP die to wafer bonding process.

very thin DVS-bis-BCB layer, thereby reducing the bonded area, and this results in a lift-off of the bonded film during InP substrate removal. Best results were obtained when the BCB was in the sol/gel rubber phase. Nearly perfect bonding was obtained as the film can deform elastically and is still tacky.

As described below, from these experiments we developed a process to bond InP/InGaAsP heterostructure dies to a processed SOI substrate. Before bonding, the SOI waveguide substrate, with a topography designed for good planarization, is cleaned using an SC-1 solution ($1NH_3$:$4H_2O_2$:$20H_2O$) at 70°C. This surface treatment lifts off particles from the surface and renders the surface hydrophilic. After surface cleaning, adhesion promoter AP-3000 from Dow Chemicals is applied. Mesitylene diluted Cyclotene 3022-35 is spin-coated at 5000 rpm on the SOI and is soft-cured (210°C for 40 min, ramped at 1.6°C/min). Subsequently, a second layer is spin-coated at 5000 rpm and undergoes a rapid thermal annealing for 2 min at 250°C, thereby increasing the degree of polymerization into the optimal region for bonding. Both curing steps are performed in a nitrogen environment to prevent the oxidation of the DVS-bis-BCB.

The cleaved InP/InGaAsP dies (with a size ranging from a few mm^2 to 1 cm^2) are temporarily attached to a Pyrex carrier using a thermoplastic photoresist. The surfaces are cleaned by removing a sacrifial InP and InGaAs layer using $3HCl$:H_2O and $1H_2SO_4$:$3H_2O_2$:$1H_2O$, respectively. This cleaning step removes the hydrocarbon contamination and lifts off the particles on the dies (mainly from the cleaving operation). The InP surface is conditioned for an optimal bonding strength by dipping in $1HF$:$10H_2O$ (as will be shown in the subsection on characterization of the bonded layer stack). This surface treatment renders the InP surface hydrophilic.[14]

The InP dies are bonded in a vacuum environment to avoid the inclusion of air at the bonding interface. The bonding is performed at 150°C in order to detach the InP dies from the Pyrex carrier as the thermoplastic photoresist starts to flow at 150°C and the stack is cured for 1 h at 250°C under a uniform pressure of 300 kPa in a nitrogen environment. The bonding sequence is graphically depicted in Fig. 5.

After bonding, the InP substrate of the bonded die is removed by mechanical grinding until about 80 μm of the substrate remains, which is then chemically removed using $3HCl$:H_2O until an InGaAs etch stop layer is reached. Due to the anisotropic etching of the InP substrate using HCl, the (112) plane is exposed in the [011] direction, forming an angle of about 35 degrees with the surface, as is shown in Fig. 6. This is due to the fact that HCl does not etch an exposed (01-1) plane.[15] This can be circumvented by using a HCl:HNO_3 etching mixture that etches isotropically but is nonselective. Therefore, the final etching step always has to be a selective (and anisotropic) etch to the InGaAs etch stop layer. Another option is to saw the InP dies instead of cleaving them, thereby not exposing a single crystallographic plane. This might, however, introduce blisters at the epitaxial layer side, which can inhibit good bonding. On the other two faces of the die, the epitaxial layer can be slightly undercut by the HCl etching.

Characterization of Bonded Layer Structures

The die-to-wafer bonded structures were characterized on bonding quality and bonding strength. The bonding quality was assessed by scanning acoustic microscopy (SAM) revealing no delamination at the bonding interface. The resolution of this method is, however, limited to about 10 μm. Infrared transmission inspection, optical inspection by bonding on a Pyrex host substrate, and SEM cross-section imaging were also performed, not revealing any bonding defects. A cross section and SAM top view image of a bonded layer structure after InP substrate removal is shown in Fig. 7.

The bonding strength was assessed by performing die shear tests on the bonded samples. 25 mm^2 InP dies with different surface conditioning were bonded to a silicon host substrate and the shear force

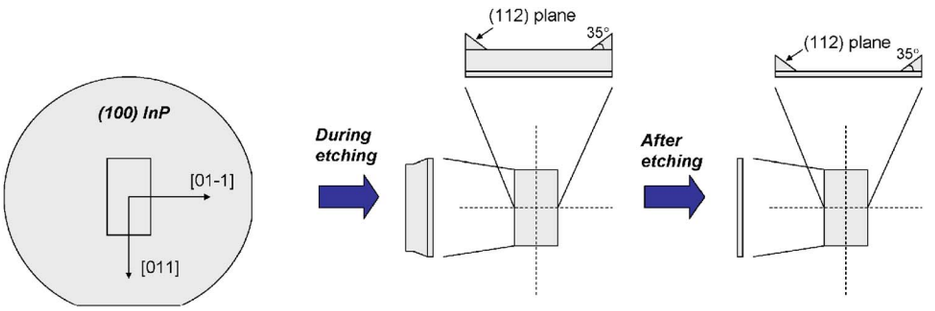

Figure 6. (Color online) InP substrate removal and the revealing of the (112) plane by anisotropic HCl etching.

needed to detach the InP dies was measured. The results are depicted in Fig. 8, in which the die shear strength of 25 mm^2 InP dies that were bonded using a 300 nm DVS-bis-BCB layer is compared for various treatments of the InP surface prior to bonding. From these results it is clear that the HF treatment before bonding gives the highest bonding strength and that this is due to a chemical change in the surface condition and not due to a particle removal effect. This can be seen by comparing the results for the HF, HF + SC − 1, and HF + SC − 1 + HF maximum shear stress. For comparison, the influence of an O_2-plasma (formation of oxides on the InP surface) and the influence of a $1H_2SO_4$:$3H_2O_2$:$1H_2O$ surface treatment (for etching the sacrificial InGaAs layer) are also shown. The critical adhesion energy of the bonded stack was measured using the Maszara razor blade method.[16] It increased from 0.2 J/m^2 before curing to 10 J/m^2 after curing for a bonding layer thickness of 300 nm. Typically, a 5 J/m^2 bonding energy is needed to survive the post-bonding processing steps (i.e., the mechanical grinding of the InP substrate).[17]

The stress induced in the bonded stack was measured by evaluating the wafer stack curvature as a function of temperature. The measurement results are plotted in Fig. 9. The temperature was ramped from 20 to 420°C at a rate of 5°C/min and then ramped back to room temperature. Little or no hysteresis can be seen and a linear relation is obtained as expected for elastic materials. The point of zero stress lies around 230°C. This is the point where the BCB fixes the InP die and the SOI substrate to form a rigid stack and lies close to the curing temperature of 250°C. The residual strain in the InP/InGaAsP epilayer at room temperature after substrate removal is therefore tensile. Strain levels are, however, below 0.05% in the

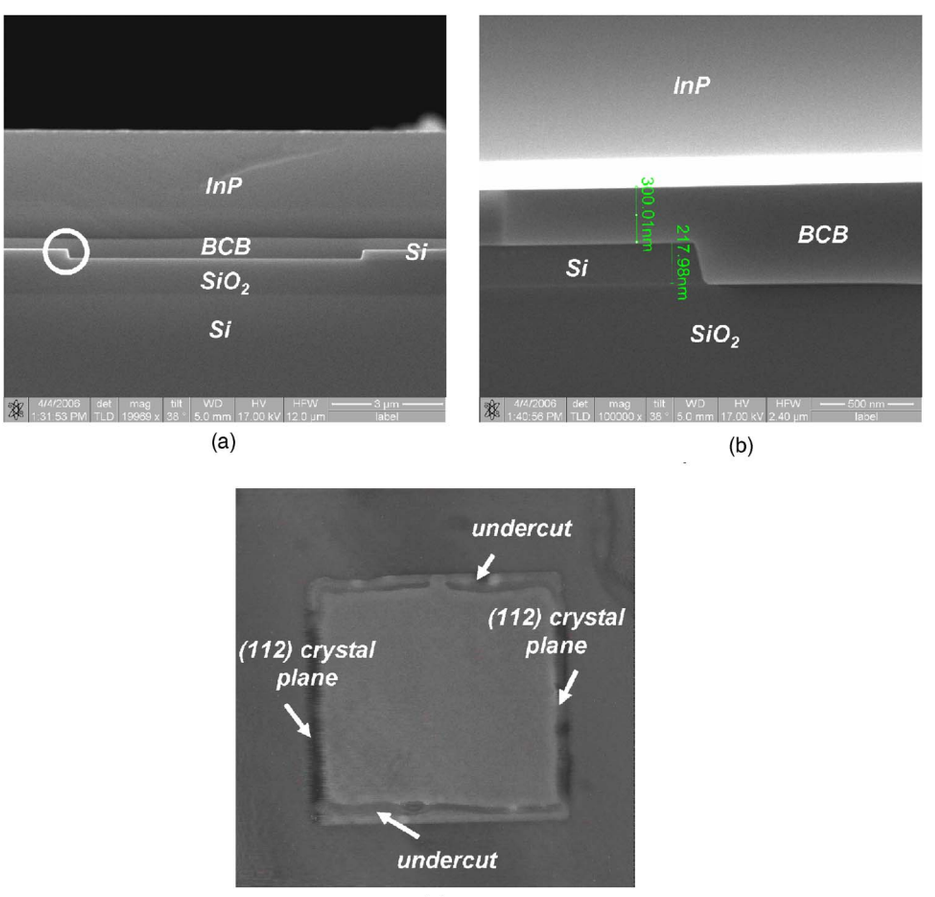

Figure 7. (Color online) Cross section (a,b) and SAM top view image (c) of a bonded layer structure. The SOI waveguide layer, BCB bonding layer, and InP/InGaAsP layer are clearly distinguishable.

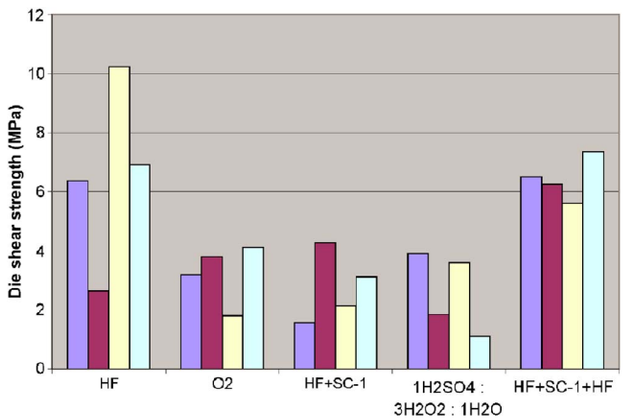

Figure 8. (Color online) Maximum shear force that can be applied to a bonded 25 mm^2 InP die bonded using 300 nm of DVS-bis-BCB.

InP/InGaAsP thin film after substrate removal, which is sufficiently low to prevent changes in the light emission properties of the InP/InGaAsP layer.

Applications

InP/InGaAsP die to SOI wafer bonding was demonstrated for the integration of III-V Fabry-Perot laser diodes, MSM photodetectors, and pin-photodetectors[18,19] on top of SOI waveguide circuits. While not yet demonstrated, this technology is equally attractive for the integration of III-V modulators, optical amplifiers, and microlasers on top of SOI waveguide circuits.

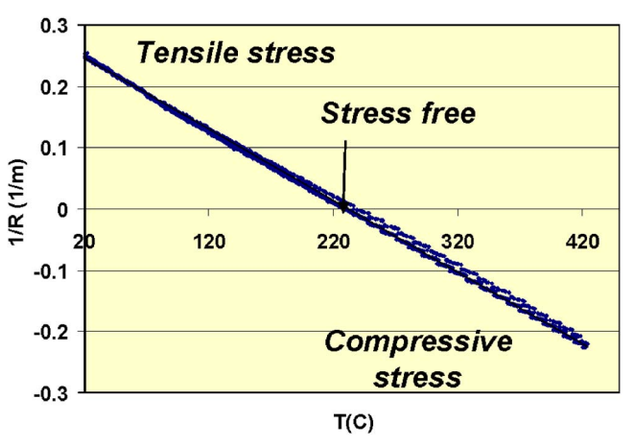

Figure 9. (Color online) Measurement of the wafer curvature as a function of temperature. The nature of the stress in the InP/InGaAsP layer is also added.

Conclusions

An integration process of InP/InGaAsP dies on top of silicon-on-insulator waveguide circuits by means of DVS-bis-benzocyclobutene adhesive bonding was developed. High-quality InP/InGaAsP epitaxial layer structures bonded to SOI were obtained and the bonding strength and quality were evaluated. First demonstrators of this technology for the fabrication of InP/InGaAsP active optical devices on top of SOI have been made, but the applicability of this generic technology reaches much further.

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