CMOS compatible silicon etched V-grooves integrated with a SOI fiber coupling technique for enhancing fiber-to-chip alignment

J. V. Galan, P. Sanchis, J. Martí

Nanophotonics Technology Center, Universidad Politecnica Valencia, Camino de Vera s/n, 46022 Valencia, Spain, jogaco@ntc.upv.es

S. Marx, H. Schröder Fraunhofer Institute for Reliability and Microintegration (IZM), Gustav-Meyer-Allee 25, 13355 Berlin, Germany

B. Mukhopadhyay, T. Tekin TU Berlin, Research Center for Microperipheric Technologies, TIB 4/2-1, Gustav-Meyer-Allee 25, 13355 Berlin, Germany

S. Selvaraja, W. Bogaerts, P. Dumon Ghent University – IMEC, Dept. of Information Technology, Photonics Research Group, Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium

L. Zimmermann Technische Universitaet Berlin, HFT 4, Einsteinufer 25, 10587 Berlin, Germany

Abstract Integration of a polarization insensitive inverted taper-based fiber coupling structure with silicon etched V-grooves is demonstrated in CMOS silicon photonics. Coupling loss of 7.5dB are measured at λ =1.55µm. A spectrum broader than 70nm is observed.

Introduction

Silicon on Insulator (SOI), has stirred up a huge interest, mainly due to the possibility to achieve low cost mass production of photonic components and circuits by adapting Complementary Metal Oxide Semiconductor (CMOS) microelectronic tools to photonic industry. One of the most challenging issues in SOI is to get an efficient coupling to optical fiber. Large mode mismatch between optical fiber and SOI waveguides forces the development of efficient fiber coupling techniques. Two kinds of efficient fiber coupling techniques have mainly been reported in literature: vertical grating couplers [1] and horizontal inverted tapers [2]. These coupling structures need stronger alignment requirements as, besides achieving acceptable coupling loss, there is always a need for an active alignment with high alignment tolerances, which, of course, is not suitable when having to produce thousand and thousand of chips. For vertical grating couplers, large alignment tolerances of about ±1µm can be achieved [3], as well as acceptable coupling loss has been reported for particular designs [4]. Also, an advantage of the so obtained vertical orientation is that it is suitable for testing purpose at wafer level. Although special novel package concepts for gratings have already been realized [5-7], such vertical orientation is not easy to adapt to standard layouts for optoelectronics devices where, quite often, we have horizontal (in-plane) orientation. For existing horizontal coupling structures in literature, low coupling loss have been achieved, but small alignment tolerances of about ±300nm are obtained [7], which is crucial for passive chip assembly, mostly in the case of multiple fiber attachment. One of the solutions to improve the alignment between optical fiber and SOI horizontal coupling techniques is the integration of V-groove structures in the silicon substrate [8] for aligning the fiber passively. Here we report experimental realization on the integration of silicon etched V-grooves with a SOI inverted taper based fiber coupling structure fabricated with CMOS fabrication tools, allowing an improvement in the alignment with the fiber for future packaging.



Figure 1: (a) Illustration of the V-groove integration with the SOI waveguide coupling structure. (b) Detailed 3D view of the coupling structure.(c) 3D graph of optical fiber placed in the V-groove.

Inverted taper based coupling structure for V-groove integration

Fig. 1a depicts an illustration on the integration of silicon V-groves with the fiber coupling structure. A detailed 3D view of the coupling structure is also depicted in Fig. 1b, as well as its main design parameters as also indicated. The 500nm wide SOI waveguide is tapered down till an inverted taper tip width of wt. The length of the inverted taper is Lt. At the same time the substrate etching is used for creating the Vgroove etch pattern, it can be useful for defining a fiber adapted wavequide with the SiO₂ layer which is hanging on air. The SiO₂ waveguide has a width W and a thickness H. As we will further use commercial SOI wafers from SOITEC with 220nm/2µm Si/SiO₂ thicknesses, here H=2µm. When optical mode in the SOI waveguide arrives on the inverted taper, it starts delocalizing itself from the SOI waveguide core and excites the optical mode in the SiO₂ waveguide adiabatically. Hence, optical mode in the SiO₂ waveguide matches much better with the fiber mode, thus resulting in an efficient coupling. Design procedure is the same as the previously published in [8]. However, wafers to be used have a different thickness than the considered in [8], so Table 1 summarizes optimized design parameters and obtained coupling loss for this particular case. It is obtained 6dB coupling loss to 10µm mode field diameter (MFD) standard optical fibers, and a polarization insensitive behaviour for optimized design. It is important to remark that just 75µm of the SiO₂ waveguide are hanging on air, as it was found it was enough from simulation results [8], thus increasing mechanical robustness of the structure.

Lt	Wt	W	Н	Coupling loss to 10µm MFD standard fibers (TE and TM)
400µm	200nm	8µm	2µm	6dB

Table 1: Optimum simulation parameters for λ =1.55 μ m.

Fabrication

The test circuits with inverted tapers were fabricated in SOI wafers with a 220nm silicon layer and 2um buried oxide (BOX). First, passive silicon structures containing the waveguides and inverted tapers were defined in a 193nm deep UV (DUV) lithography step. Second, waveguides and tapers were etched 220nm, and then covered with 750nm of SiO₂. A new hard-mask based process was then developed to fully open the 2.75um of SiO₂ as etch pattern for definition of the V-grooves. Fig. 2a depicts a scanning electron microscope (SEM) image of window in the oxide for definition of the V-grooves.



Figure 2: a) Edge of window in the oxide for definition of the V-grooves. b) Optical microscope and c) SEM images of fabricated samples.

The fabrication of small 3D silicon structures such as V-grooves requires very precise micromachining technologies like anisotropic etching of monocrystalline silicon, since passive alignment of fibres are addressed. Aqueous KOH is widely used in this technique. The controlling the involved physical and electrochemical processes are challenging. For device fabrication, these issues are of great economical importance. It should be ensured that the etching behaviour is stable and predictable. In particular the anisotropy ratio (etch depth divided by the lateral underetching of the mask) should be reproducible with high accuracy and the etched surfaces should be smooth. To understand mechanism involved in anisotropic KOH etching process a model was proposed to explain and to calculate the microscopic 3D shapes [9]. Based on the theoretical and experimental investigations [10] a controllable process for three dimensional structuring by means of anisotropic KOH etching was developed. Fig. 3b and Fig. 3c depict optical and scanning electron microscope (SEM) images of fabricated V-grooves, respectively. As known from former detailed experimental investigations [9,10] silicon dioxide etch masks are not the best etch mask material due to a not negligible etch rate as can be seen in Figure 3b and 3c. Such underetching caused by the etch mask material and some possible misalignments of the etch mask with respect to the {100} silicon crystal direction cause uncertainties of V-groove width. In order to avoid geometrically constrains regarding to the fiber diameter we only controlled the etch depth by etching time and used and oversized V-groove.

Measurements

Fig. 3a depicts experimental measurements for transmission spectrum and TE polarization of fabricated

samples. A top view image of optical fiber placed in the V-groove while measuring the samples is also shown in Fig. 3b. We obtained 7.5dB coupling loss at λ =1.55µm. Obtained experimental results slightly differ from those previously obtained theoretically mainly due to small differences in dimensions of the structures. Fig. 4 depicts two different SEM images showing actual section dimensions of SiO₂ waveguide after fabrication. We measured a waveguide width of 6.7µm as well as a waveguide thickness of 1.689µm, whilst design values were 8µm and 2µm, respectively. By changing polarization at the input of the structure, we also obtained a small variation of ±0.5dB on results depicted in Fig. 3a. So, we also can corroborate that our coupling structure is polarization insensitive, as expected from simulation results. Moreover, obtained spectral response is almost flat in a wavelength bandwidth higher than 70nm, as shown in Fig. 3a. It is important to notice that lower coupling loss (~1-2dB) may be achieved by adding a 6-7µm uppercladding layer on top of the SOI wafer, better mode matching to optical fiber mode.



Figure 3: a) Transmission spectrum of the fabricated samples. b) Top view image of optical fiber placed in the V-groove while measuring the samples.



Figure 4: SEM images about detailed view of actual section dimensions of the SiO₂ waveguide.

Conclusions

In conclusion, the demonstration of the integration of an inverted taper-based fiber coupling structure with silicon etched V-grooves is reported. Fabrication has been carried out using CMOS fabrication tools, thus allowing low cost mass production. Coupling losses of 7.5dB are measured for fabricated samples at λ =1.55µm. We also found a broadband spectrum higher than 70nm as well as insensitivity to polarization.

Acknowledgments

This work was supported by the FP6 ePIXnet Network of Excellence. The authors would like to thank ePIXfab (www.epixfab.eu) and ePIXpack (http://epixpack.eu) for fabrication. W. Bogaerts acknowledges the Flemish Fund for Scientific Research (FWO) for a postdoctoral grant. J. V. Galan, P. Sanchis and J. Martí acknowledge Spanish Ministerio de Ciencia e Innovacion (MICINN) under contracts TEC2008-06360 and TEC2008-06333. All authors also acknowledge the European Commission under project HELIOS (photonics electronics functional integration on CMOS), FP7-224312.

References

- [1] D. Taillaert et al., IEEE J. Quantum Electr., vol. 38 (2002), pp. 949-955.
- [2] V. R. Almeida et al., Opt. Lett., vol. 28 (2003), pp. 1302-1304.
- [3] D. Taillaert et al., Japanese J. of Appl. Physics, vol. 45 (2006), pp. 6071-6077.
- [4] F. Van Laere et al., IEEE J. of Ligthw. Technol., vol. 25 (2007), pp. 151-156.
- [5] T. Tekin et al., Proc. of European Conference on Optical Communications, vol. 5, (2008) pp. 93-94.
- [6] H. Schröder et al., SPIE Photonics West Conference OPTO2009 Proc. SPIE 7221, 72210D.
- [7] L. Zimmermann et al., IEEE LEOS Newsletter December 2008.
- [8] J. V. Galan et al., Opt. Express, vol. 15 (2007), pp. 7058-7065.
- [9] H Schröder et al., J. Micromech. Microeng. Vol.8 (1998) pp.99–103.
- [10] H. Schröder and E Obermeier, J. Micromech. Microeng. 10 (2000) 163–170.