High Efficiency Broadband Polarization Rotator on Silicon-On-Insulator

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Abstract: We demonstrate a polarization rotator fabricated using a 4 etch-step CMOS-compatible process including layer depositions on a silicon-on-insulator wafer by means of 193nm deep UV lithography. The measured polarization rotation efficiency is at least -0.5dB over a wavelength range of 80nm around 1550nm.

1. Introduction

In 2009 we demonstrated high efficiency grating couplers having only -1.6dB insertion loss with a 3-dB bandwidth of 80nm. This was done on Silicon-On-Insulator using an extra silicon overlay [1]. In this paper we will show that the same process can be used to achieve polarization rotation. This functionality is especially required in optical communication system circuits where polarization diversity [2] or polarization tracking is used. The most successful implementations of polarization rotators to date are based on waveguides with angled sidewalls [3]. However, this would introduce extra dedicated processes. In [4] a compact polarization rotator was proposed using a straight asymmetric shallow etch in a square strip waveguide configuration. In what follows we will report on the development and characterization of a polarization rotator based on this principle and thereby integrating polarization rotators and highly efficient grating couplers on the same optical chip.

2. Fabrication Process and Polarization Rotator Design

The complete fabrication process is done in the *imec* CMOS pilot line with 193nm DUV lithography and consists of around 30 process steps. First a very thin silicon oxide layer is deposited on top of a 200mm SOI wafer with a buried oxide layer thickness of 2μm and a crystalline silicon layer thickness of 220nm. In a second step an amorphous silicon layer of 160nm is deposited and a deep etch is performed through the amorphous silicon and oxide layer reaching 70nm into the crystalline silicon layer. This is used to define the slits of the high efficiency grating couplers. Next, the amorphous silicon is removed where necessary and the deposited oxide layer in the first step will now act as an etch stop layer in order to not affect the underlying crystalline silicon. Next a shallow etch of 70nm in the 220nm crystalline silicon layer is introduced to achieve low loss and robust spectral filter components. In the end the waveguide trenches are defined by a 220nm etch and the amorphous silicon is annealed after which it becomes polycrystalline silicon.

In Figure 1 an artist's impression is shown of a highly directional grating coupler [1] and a polarization rotator, both compatible with the aforementioned process flow. The polarization rotator design is based on symmetry breaking of a single-mode waveguide with an almost square waveguide profile. A vertical taper, defined in the silicon overlay, is used as an adiabatic transition between a 450nm wide Si waveguide with a height of 220nm and an equally wide waveguide with a silicon overlay. This double patterned strip waveguide has a combined thickness of 380nm and is formed by 220nm crystalline silicon, a thin layer of silicon oxide and 160nm of polycrystalline silicon. The actual polarization rotator is formed by an asymmetric shallow etch of 70nm in a 355nm wide waveguide with silicon overlay. Maximum conversion efficiency is only possible when a TE/TM polarized fundamental mode couples equally to both 50% TE/TM polarized fundamental modes of the asymmetrical waveguide at the symmetric-asymmetric waveguide interface. At the conversion length L_c of 8μm, both asymmetrical hybridly polarized waveguide modes will couple to the fundamental TM-mode in the output waveguide when a TE mode is launched (and vice versa when a TM mode is launched) at the asymmetric-symmetric waveguide interface and hereby obtaining polarization conversion. The short conversion length is a consequence of the large difference in propagation constants of the two beating modes in the asymmetric waveguide and results in a large optical polarization conversion efficiency bandwidth.

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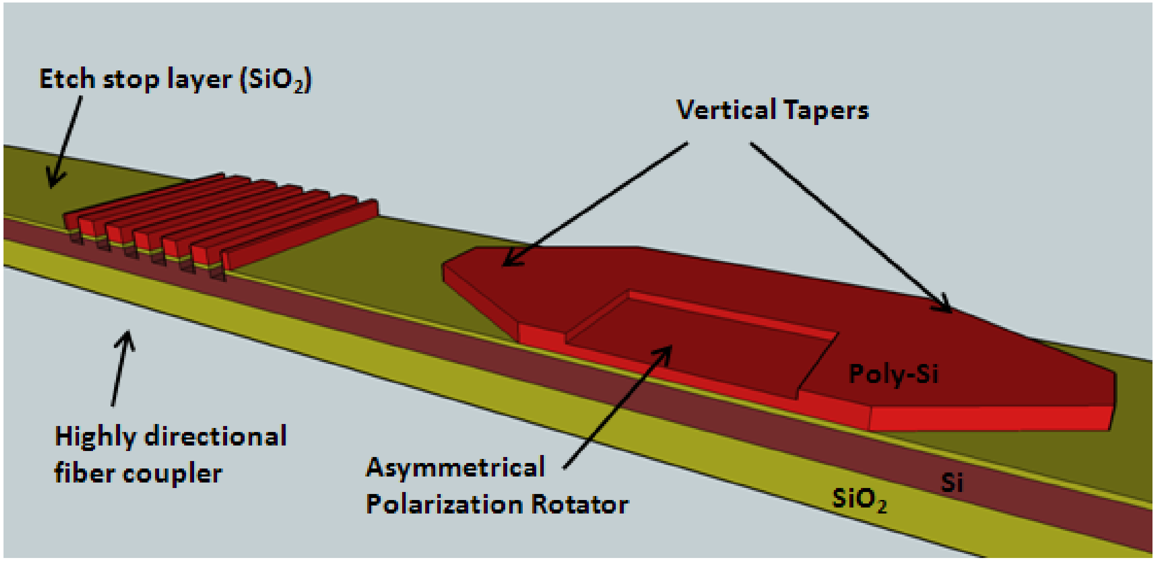

Fig. 1: Artist's impression of a highly directional fiber coupler and asymmetrical polarization rotator fabricated within the same process flow. (Dimensions are not to scale)

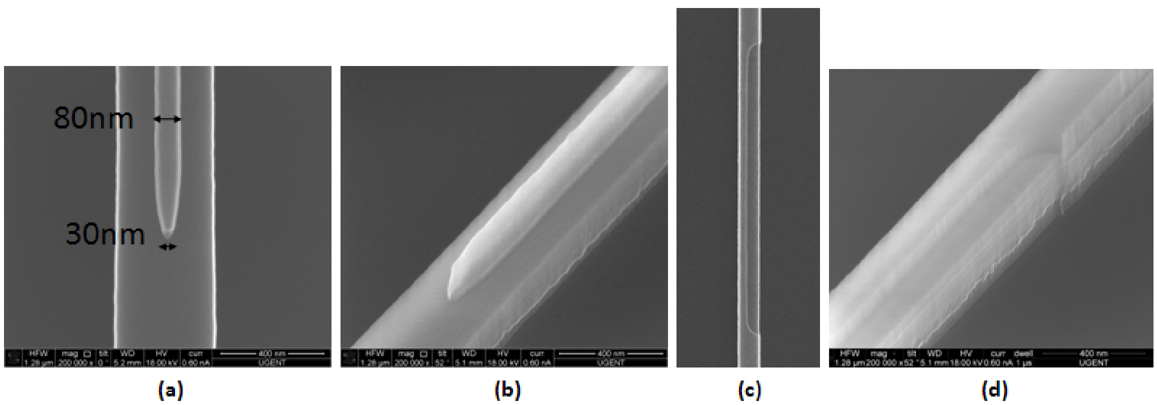

Fig. 2: SEM pictures: Vertical Taper tip (a,b) and Polarization Rotator (c,d).

3. Characterization

With this polarization rotation method, it is in theory possible to achieve 100% rotation efficiency. However, the finite width of the vertical taper tip, fixed at 100nm, introduces 5% loss for the TM polarized mode and is lossless for the TE polarization. Furthermore, a non-ideal symmetric-asymmetric waveguide interface could undermine the excitation ratio of the modes in the asymmetric waveguide. Another showstopper could be a misalignment or linewidth variation in the double patterning method of the waveguide with the silicon overlay. Nevertheless, these issues will turn out to be of minor influence for the polarization conversion in the experimental realization.

Figures 2 (a) and (b) show a SEM picture of the fabricated vertical taper tip. Due to a fixed high lithographic illumination dose for defining the overlay etch, the silicon overlay tip is only 80nm wide, leading to a negligible efficiency penalty for the vertical tapering for both TE and TM polarizations. SEM pictures 2 (c) and (d) of the polarization rotator itself reveal a rounded symmetric-asymmetric waveguide interface. The measured waveguide width is 310nm and the silicon overlay width is around 300nm wide, deviating from the theoretically optimal predicted waveguide widths of 355nm. This non-recurrent uncertainty in the fabrication process was circumvented by a relatively large parameter sweep of the waveguide width, conversion length L_c and fill factor of the shallow etch width with respect to the waveguide width.

The measurement results of the best performing polarization rotator are plotted in Figure 3. The efficiency is ex-

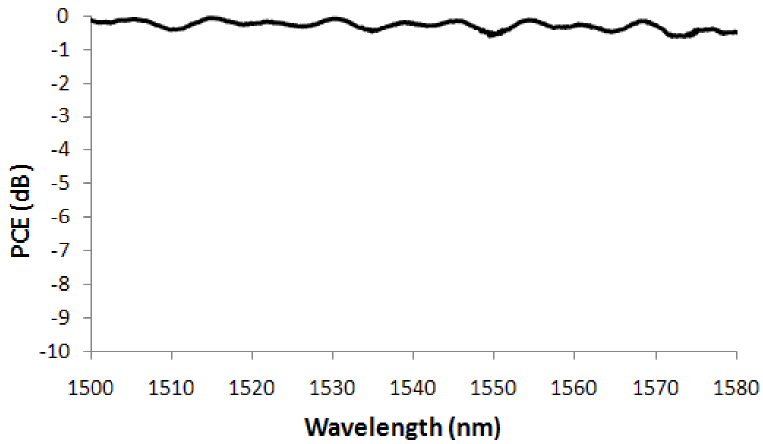

Fig. 3: Polarization Conversion Efficiency (PCE) measurement.

pressed in terms of polarization conversion efficiency (PCE), defined by $PCE = P_{TM}/(P_{TE}+P_{TM})$, where P_{TM} and P_{TE} are respectively the powers coupled into the TE/TM polarized output modes. A high polarization conversion efficiency of -0.5dB was measured over a broad wavelength range of 80nm, equal to the 3-dB bandwidth of the grating coupler. This high efficiency proves that our earlier fabrication remarks such as a non-ideal waveguide interface don't form any fundamental problem in achieving high performance polarization rotation. The actual dimensions of this polarization rotator are a waveguide width of 330nm, a conversion length of 9μm and a shallow etch fill factor of 44%.

4. Conclusion

We have experimentally realized a high efficiency and broadband integrated polarization rotator with a polarization conversion efficiency of -0.5dB over a bandwidth of 80nm. An advanced passive SOI 4 etch-step process flow was used for the fabrication. With this process, 4 different layer thicknesses can be resolved and high-efficiency grating couplers using a silicon overlay could be integrated on the same optical chip. Furthermore, the accompanied extra design freedom offers an excellent tool to optimize other optical integrated components such as splitters, filters and optical interconnects. Additionally, when using the polarization rotator in an optical circuit, one has to filter the unwanted polarization crosstalk with a polarization splitter by means of e.g. a directional coupler or MMI.

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