JNTE 10

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OPTICAL COUPLING OF SOI WAVEGUIDES AND III-V PHOTODETECTORS

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UNIVERSITEIT GENT

ESA/ESTEC
(ARTES 5)

SEVENTH FRAMEWORK PROGRAMME

Outline

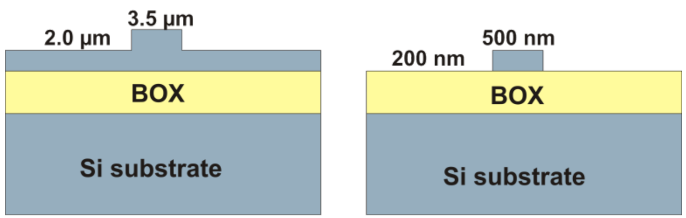
- Background and motivation
- Coupling light from fiber to silicon waveguides
  - Principle of grating couplers
- Photodiode design
  - Photodiode design for high speed
  - Prism coupling
  - Evanescent coupling
- Fabrication
  - Prism photodiode fabrication
  - Heterogeneous integration
- Performance
  - Prism photodiodes, discrete and integrated (OTUS)
  - Heterogeneously integrated photodiodes (BOOM)
- Conclusion

Background: Integrated optics

SOI platform

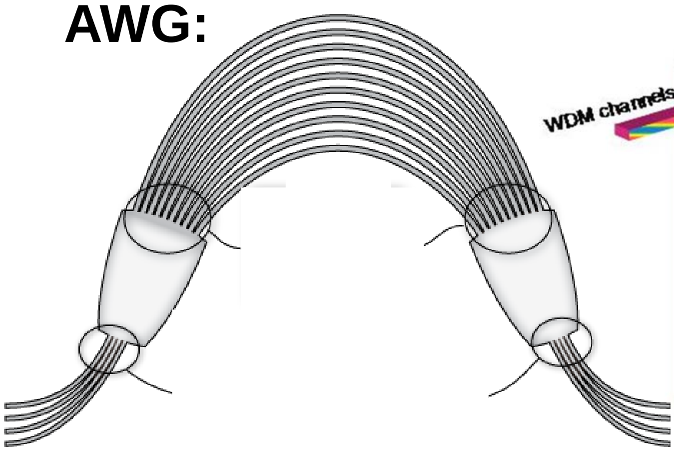
light wave guiding and processing
(optics - interference)
CMOS technology

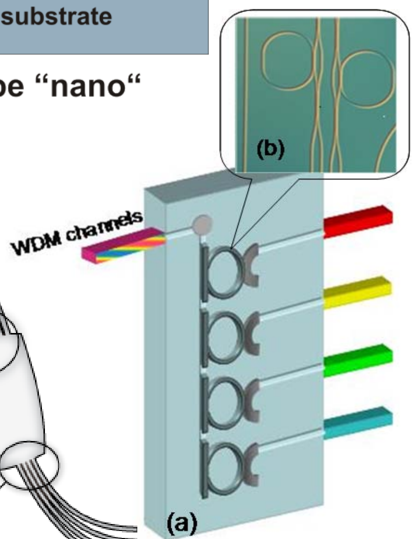
SOI waveguides:



type “micro“ type “nano“

AWG:

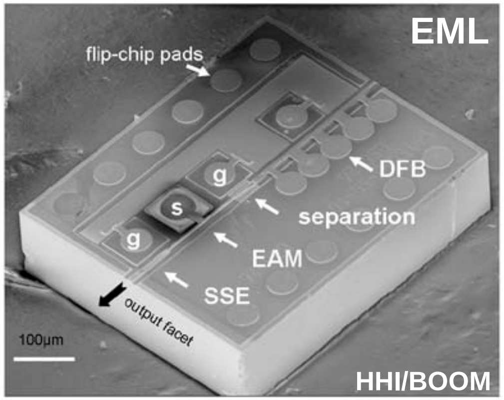




III/V oe-devices

light detection,
modulation
and generation
(applied
Quantum Theory)
wavelength range: 1.3 µm … 1.5 µm
(fibre based telecommunication)

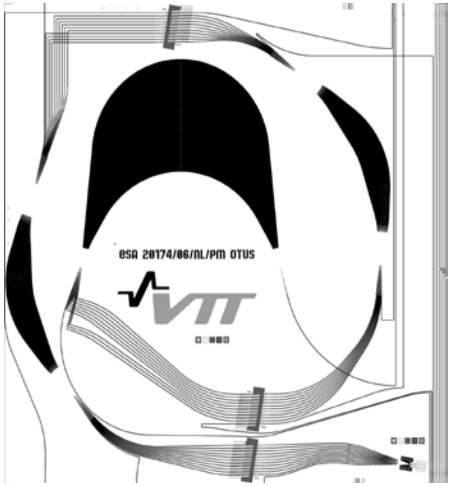
InP, InGaAsP,
InAlGaAs
InGaAs on InP



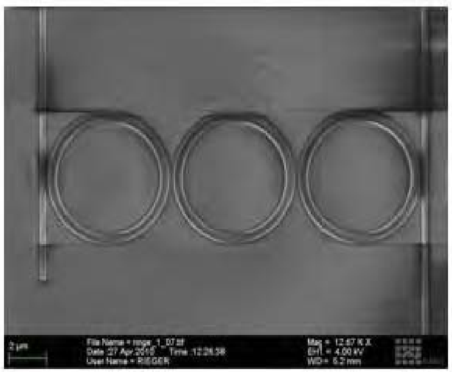
Waveguides,
photodiodes,
modulators: Mach-Zehnder (MZI),
electro-absorption (EAM),
semiconductor amplifiers (SOA)
lasers and integrated devices

Motivation

"micro"-waveguides:



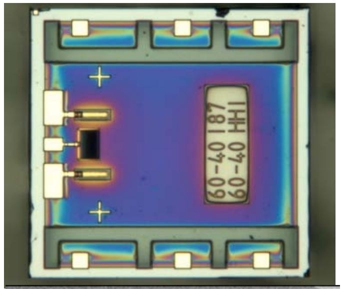
"nano"-waveguides:

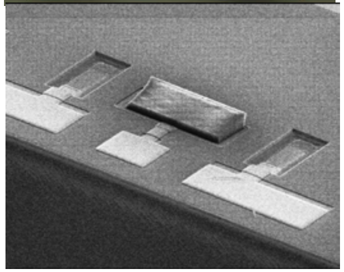


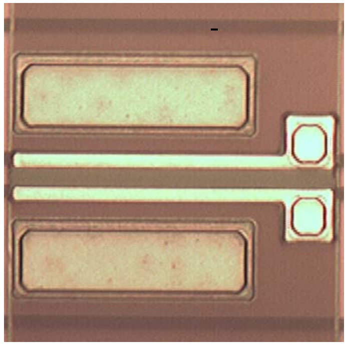
SOI platform

III/V oe-devices

hybrid integration







Integration, optical coupling → How?

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Heinrich Hertz Institute

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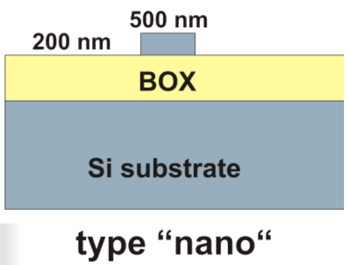
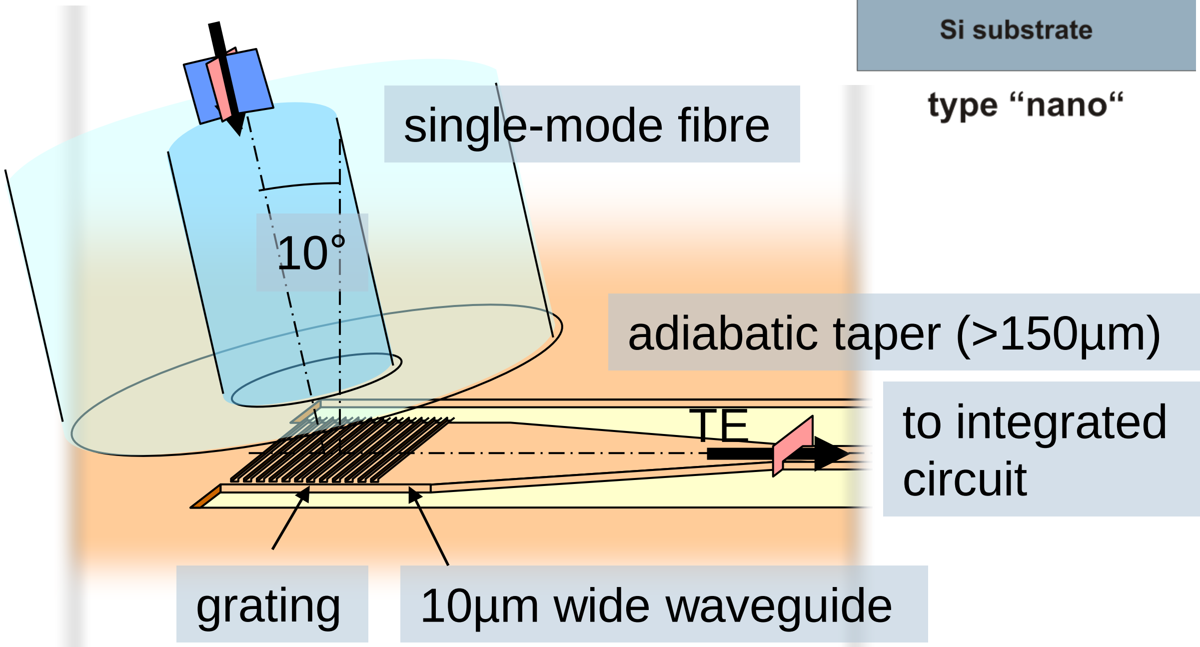
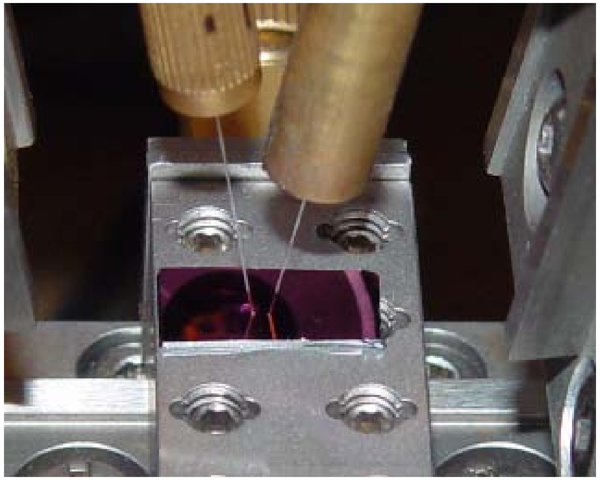
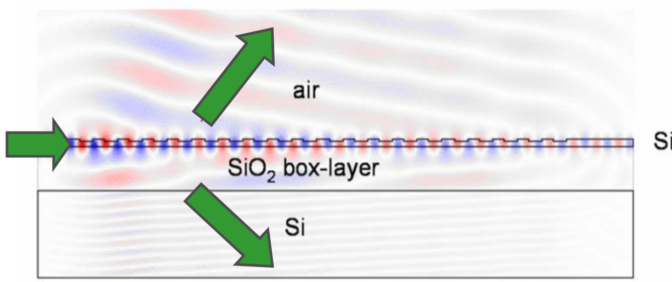
Coupling light into Si “nano” waveguides

Grating fiber couplers



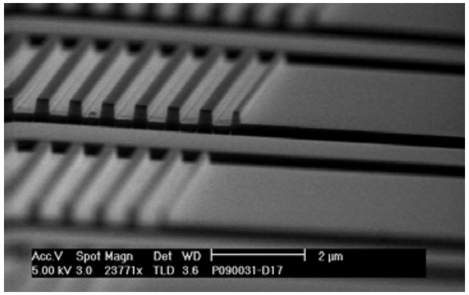






Efficiency

- **Standard: 31 %** — **D. Taillaert, JQE 7, p949 (2002)**
- **With poly-silicon overlay: 68 %** — **D. Vermeulen, GFP09, PD1**



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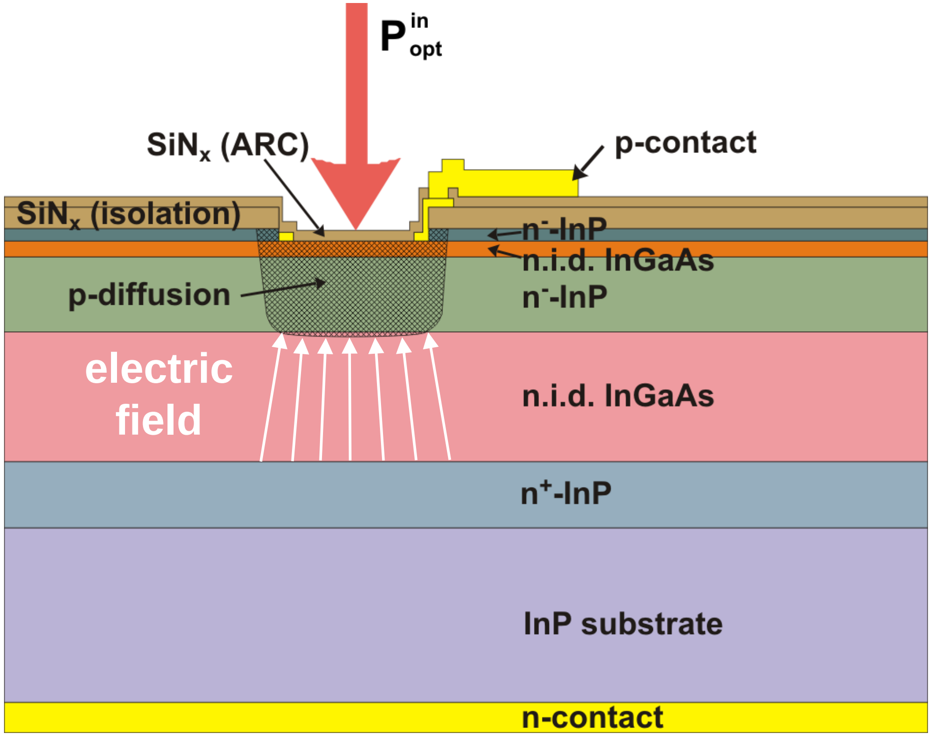
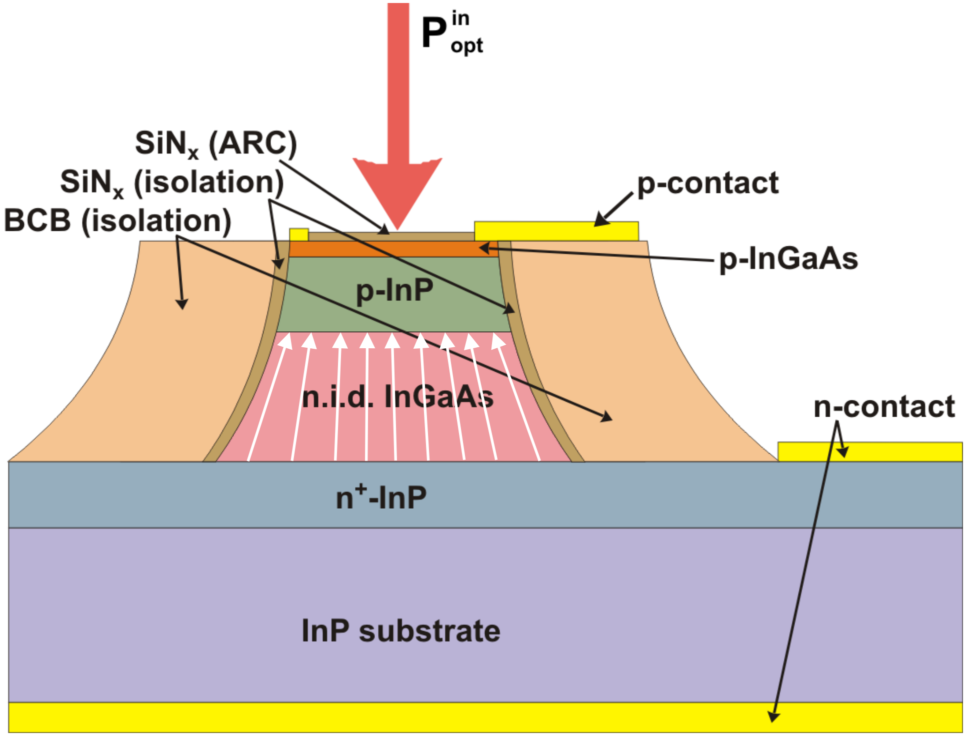
III-V Photodiodes



planar type



mesa type

How to make a high-speed PD

Bandwidth is depending on: (K. Kato,1993.)

- The time it takes a carrier to drift across the depletion region

$$f_t = \frac{3.5v}{\pi d}$$

v = average speed holes and electrons
d = thickness intrinsic layer

- The time it takes to charge and discharge the capacitance of the diode

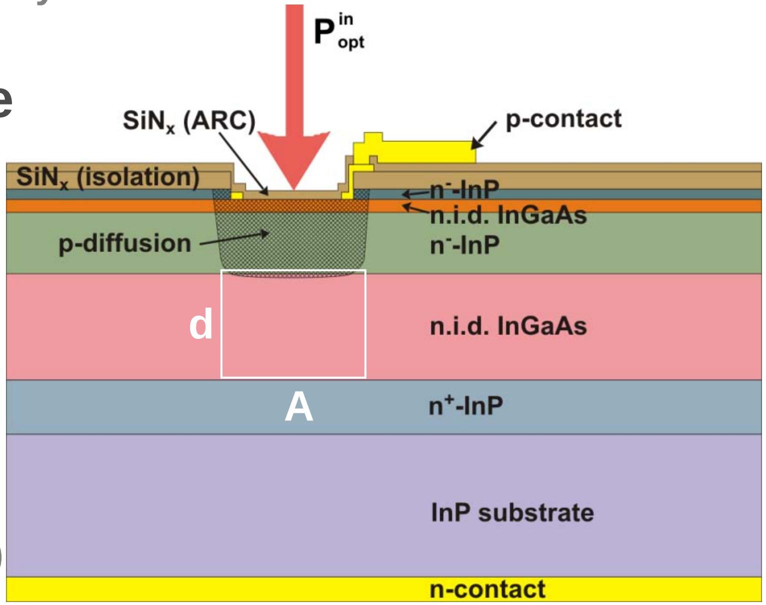
$$f_{RC} = \frac{1}{2\pi C(R_{load} + R_{contact})}$$

C = capacitance
R = resistance

$$C = \frac{\epsilon_0 \epsilon_r A}{d}$$

$$R = \frac{k}{A}$$

A = area
d = thickness intrinsic layer
ε_r = relative permittivity
k = contact resistance (Ohm.m^2)

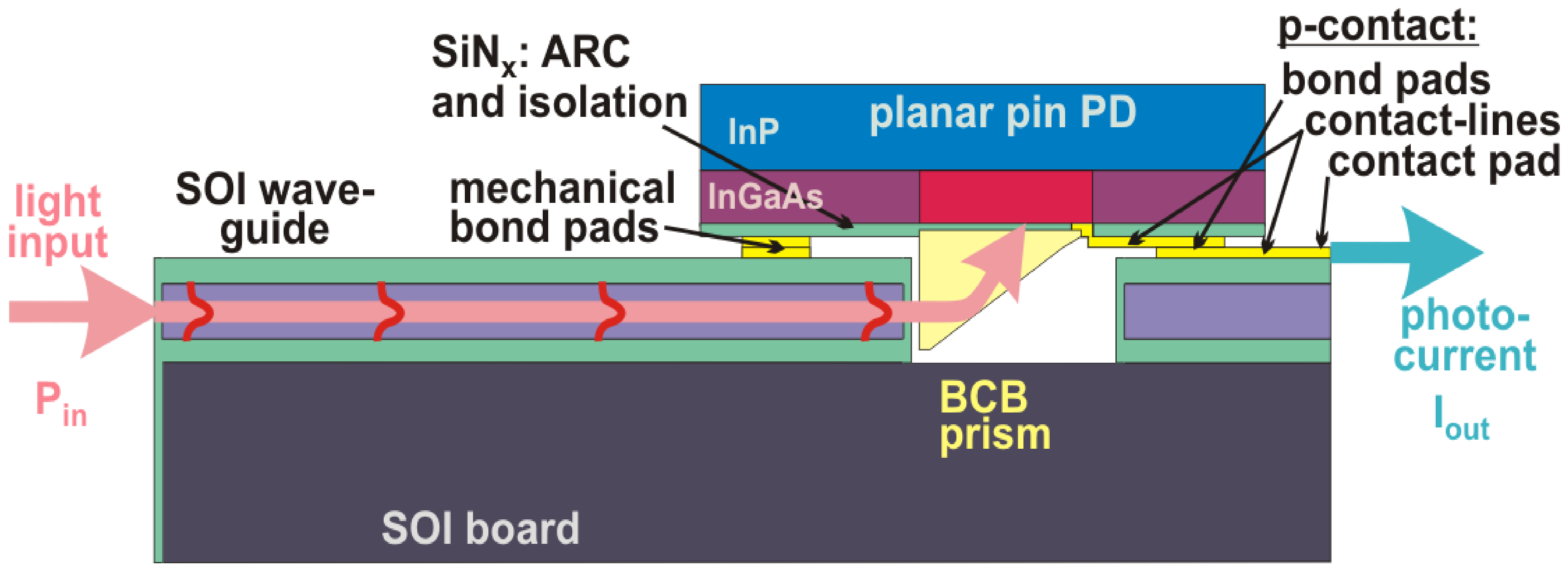


However: C is determined by active area *and* parasitics

Total 3-dB bandwidth:

$$\frac{1}{f_{3dB}^2} = \frac{1}{f_t^2} + \frac{1}{f_{RC}^2}$$

OTUS PD: Integration and optical coupling



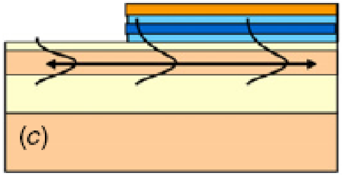
Requirements:

- **Compatible architectures (fabrication, integration)**
- **Effective optical coupling (high responsivity)**
- **Suitable for 10 Gb/s operation**
- **Independent of polarization and wavelength**

Light coupling Si "nano" waveguides/III-V PDs

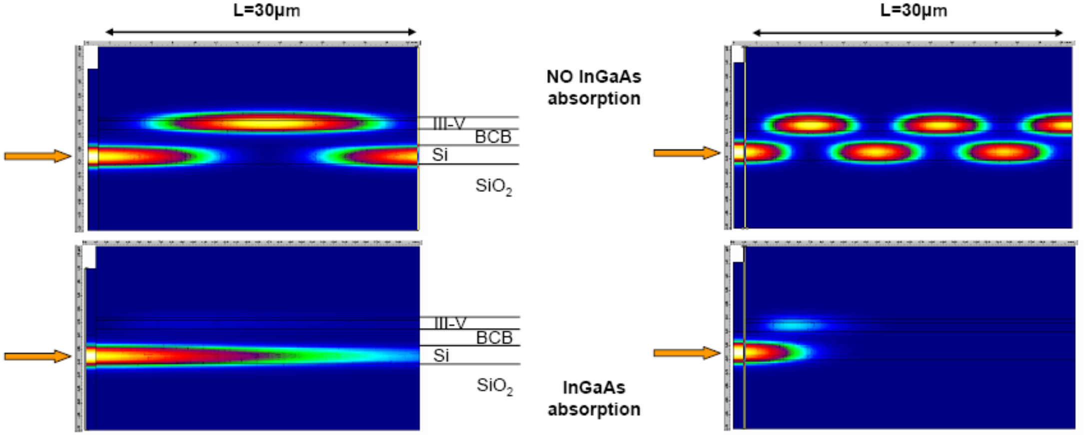
Principle of evanescent coupling

- **Coupled mode theory: power transfer from Si waveguide into III-V absorption layer**



- **For large & fast power transfer**
  - Similar phase velocity → small phase mismatch
  - Large mode overlap → thin bonding layer
- **Power transferred into the III-V layer is absorbed**

Example evanescently coupled PD:
Power transfer from silicon layer to III-V layer

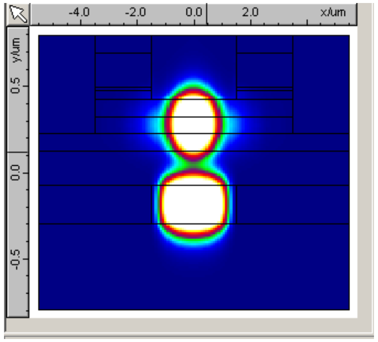


(a) 400nm BCB (b) 200nm BCB

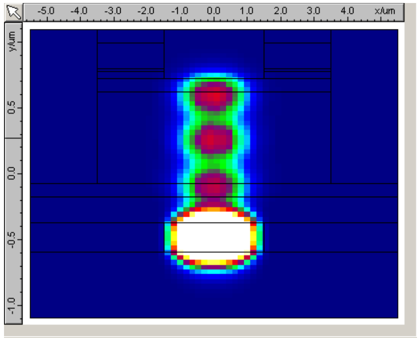
Increase high-speed performance

- **Optimize trade-off RC-limit and transit-limit**
  - **Find optimum absorption layer thickness d**

Thin InGaAs
- Coupling the 0th order

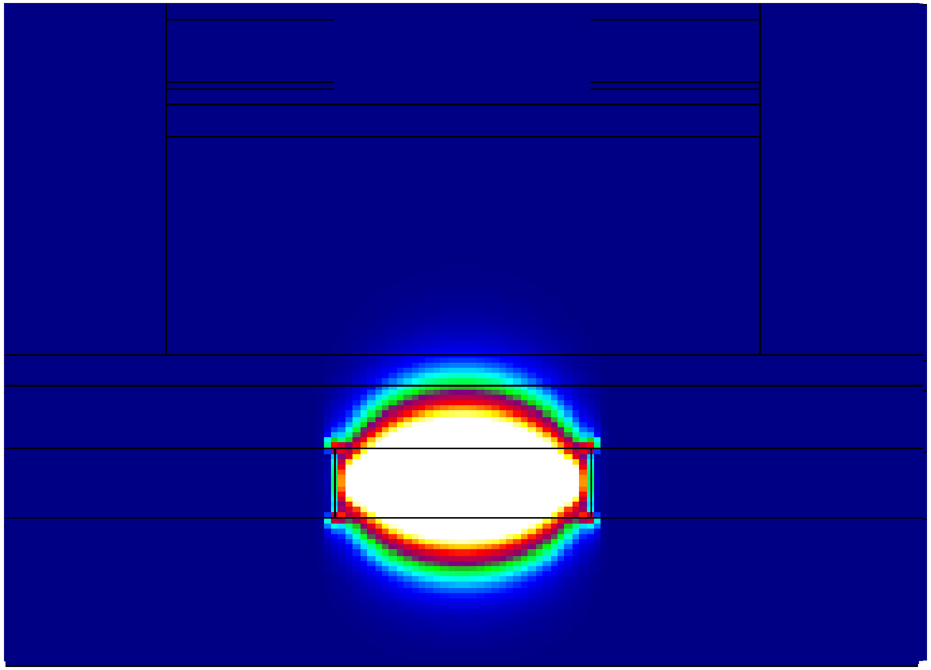


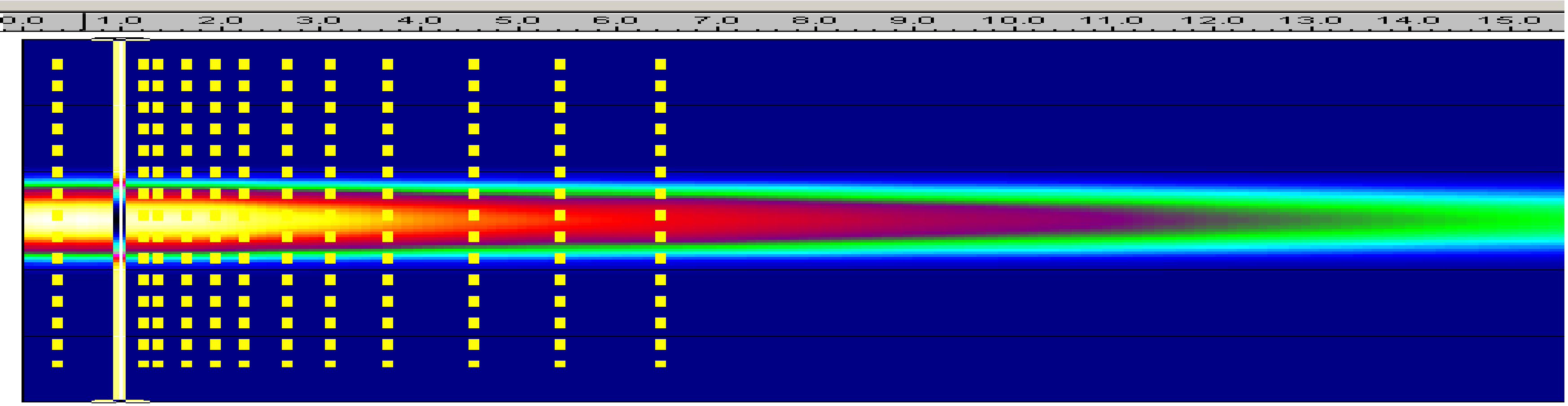
Thick InGaAs
- Coupling to 2nd order



- **Optimize silicon waveguide for phase matching**
  - **High responsivity:**
    - **minimized metal contact absorption**
  - **Fast absorption:**
    - **short detector length for lower capacitance**

Example: Simulating TM detector





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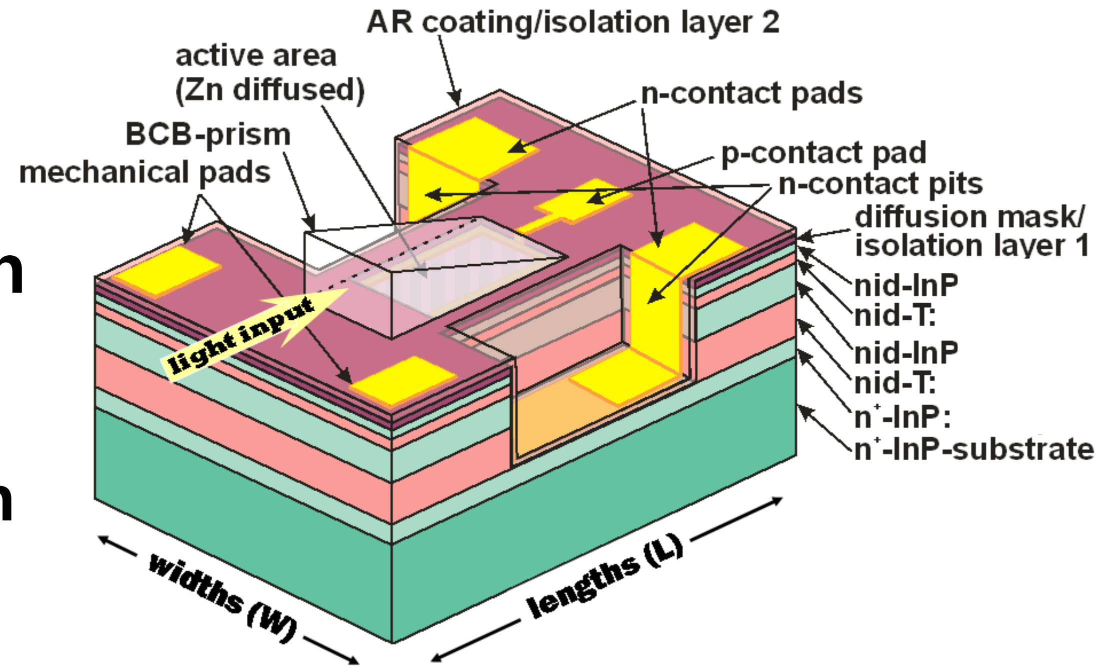
Fabrication – processing steps

Standard photodiode processing sequence

+ BCB prism fabrication as add-on:



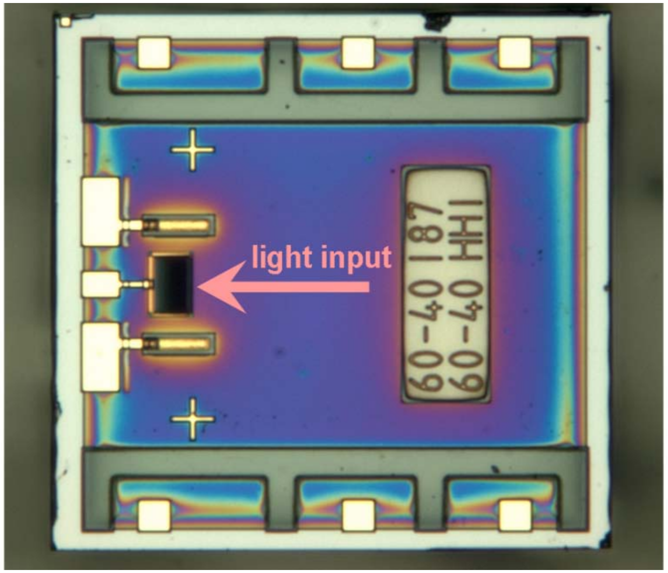
❶ **BCB layer deposition and curing**

❷ **Lithography to produce a tapered resist mask (providing sliding mask technique)**

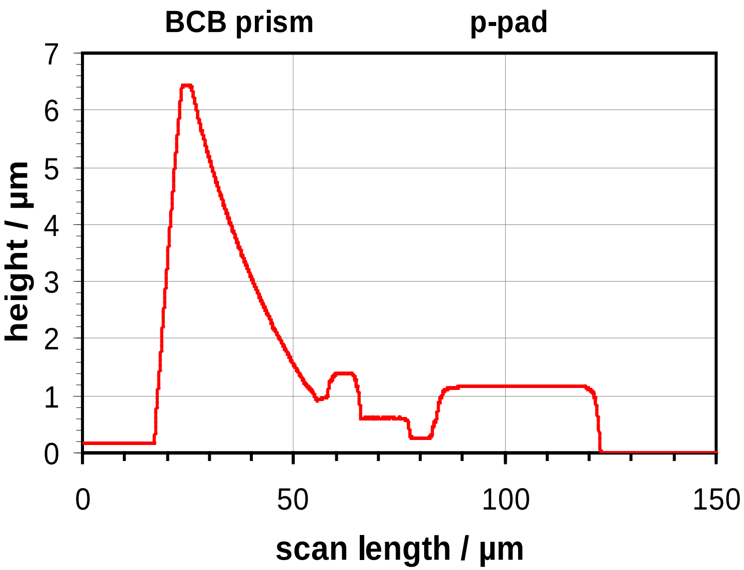
❸ **Relief transfer into BCB layer by RIE process (O_2 containing plasma)**

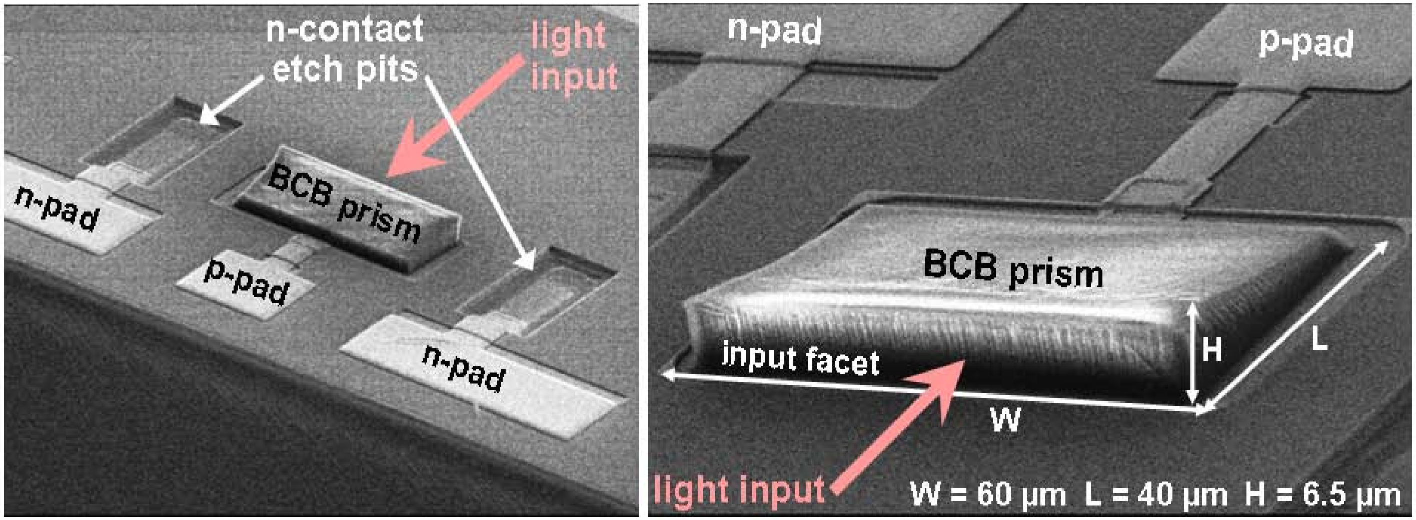
→ **Advantage: "custom-made" prism shapes available**

Fabrication of photodiode chips - results



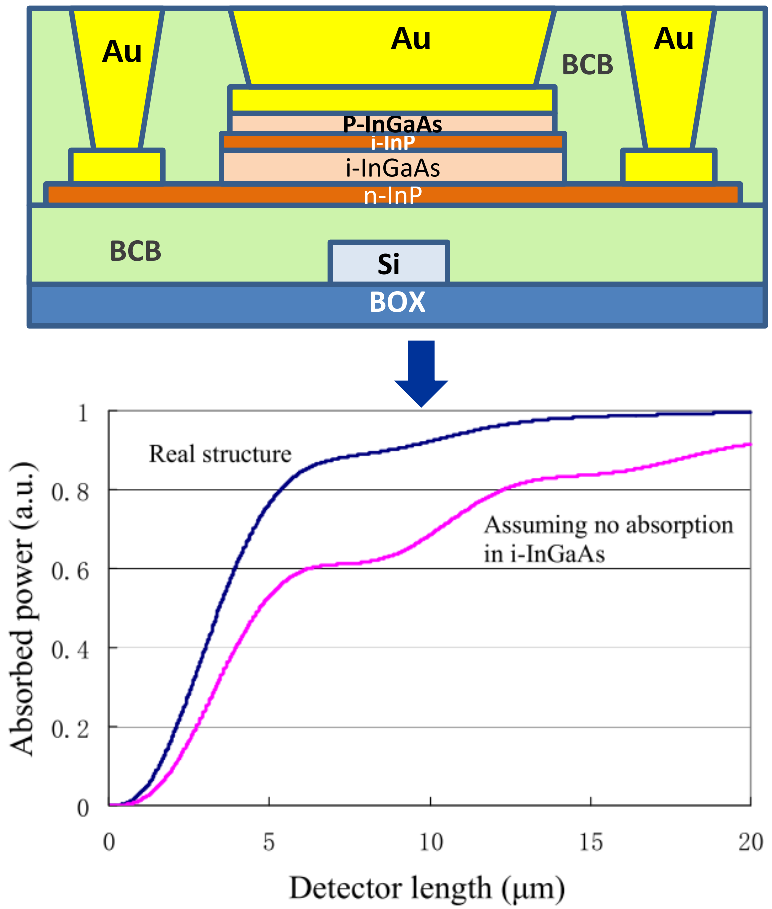
Chip footprint: 500 x 500 µm²



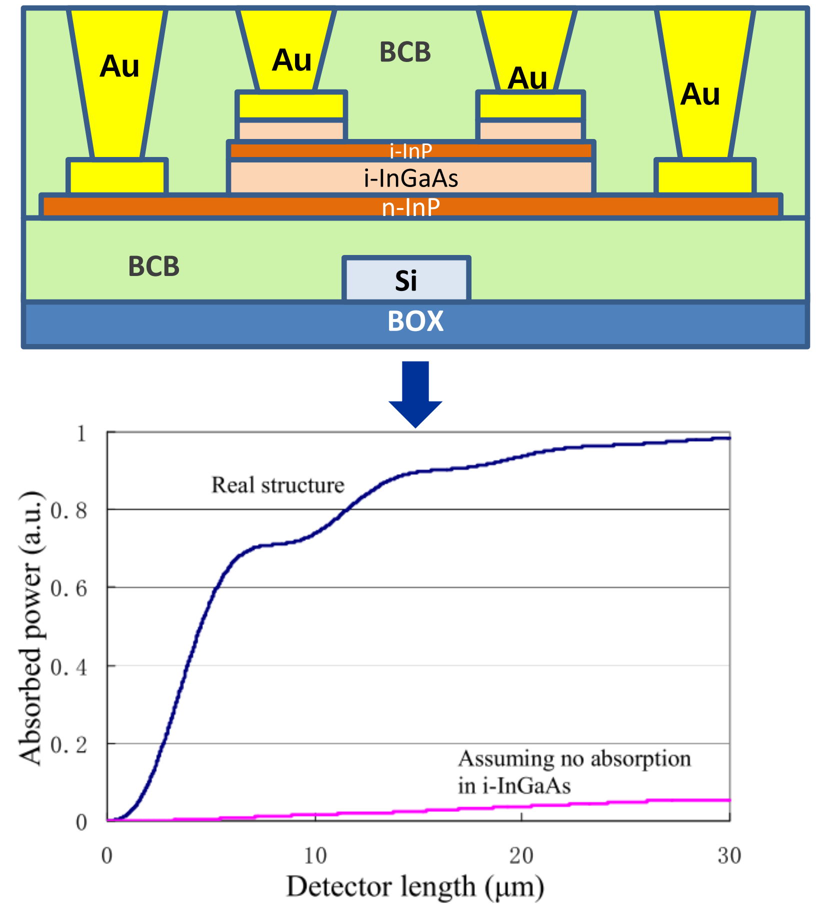


Photodiode design evanescent coupling

Old design



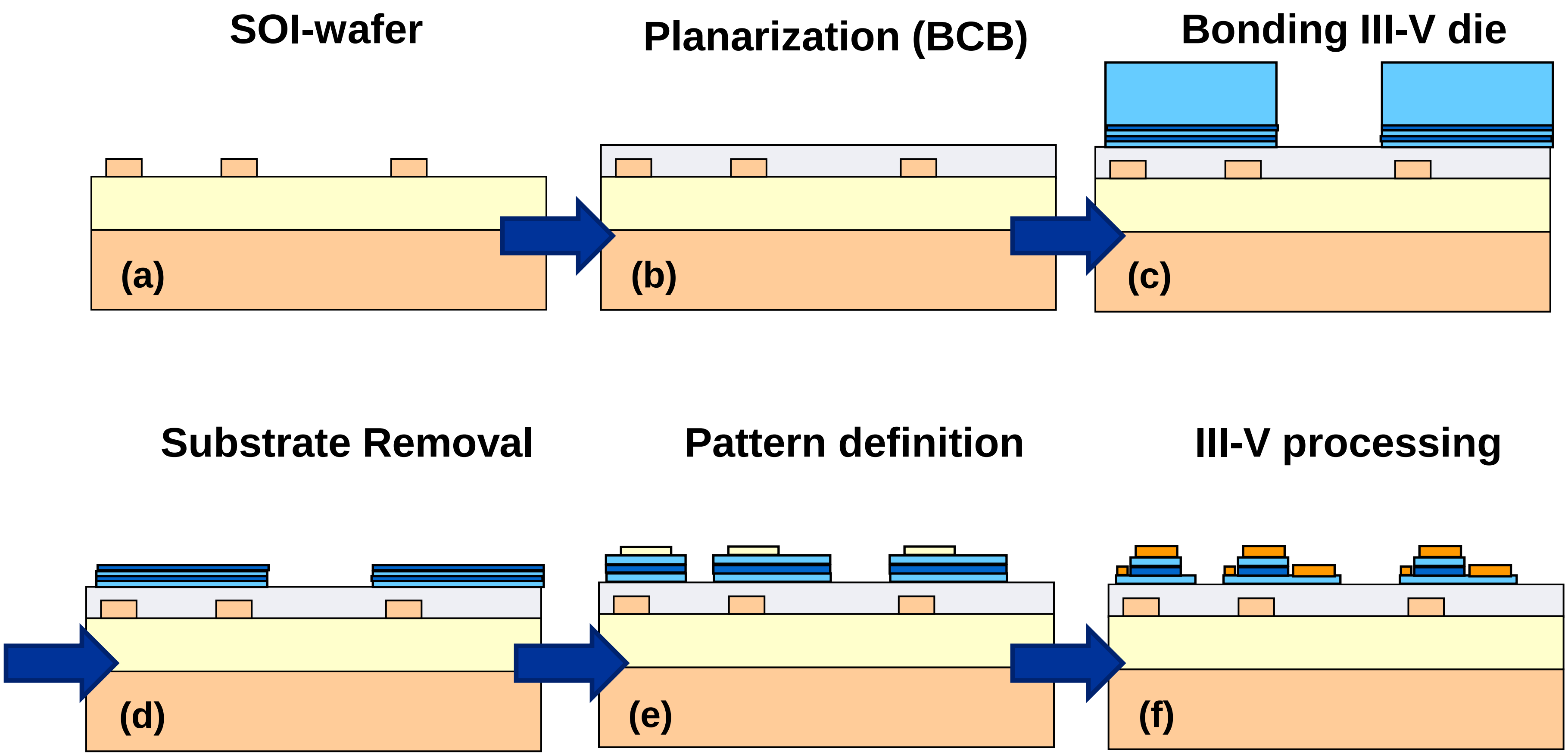
New design: the helmet



Improvement in responsivity by minimizing absorption in contact metal and p-doped InGaAs

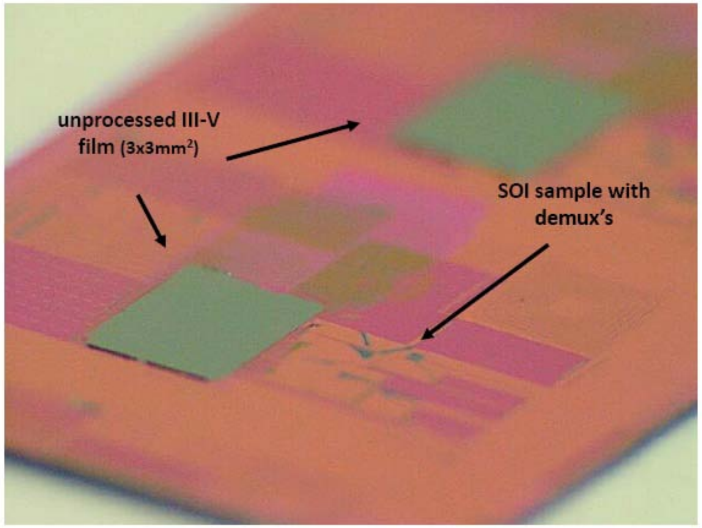
Z. Sheng, GFP, 2009

Heterogeneous integration

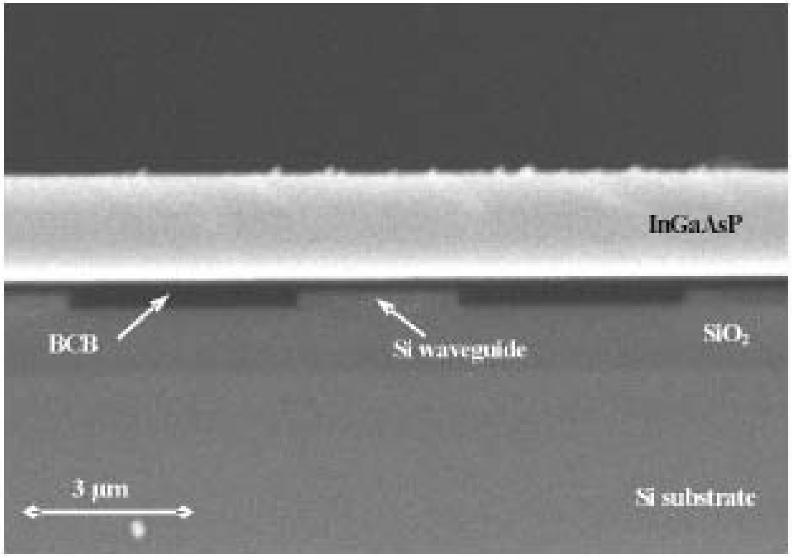


Heterogeneous integration examples

- **Two unprocessed BCB bonded InP-based epitaxial layers (3 x 3 mm²) on top of an SOI substrate**



- **Cross-section SEM picture of a III-V film (after substrate removal) bonded on SOI using a 100 nm BCB layer**



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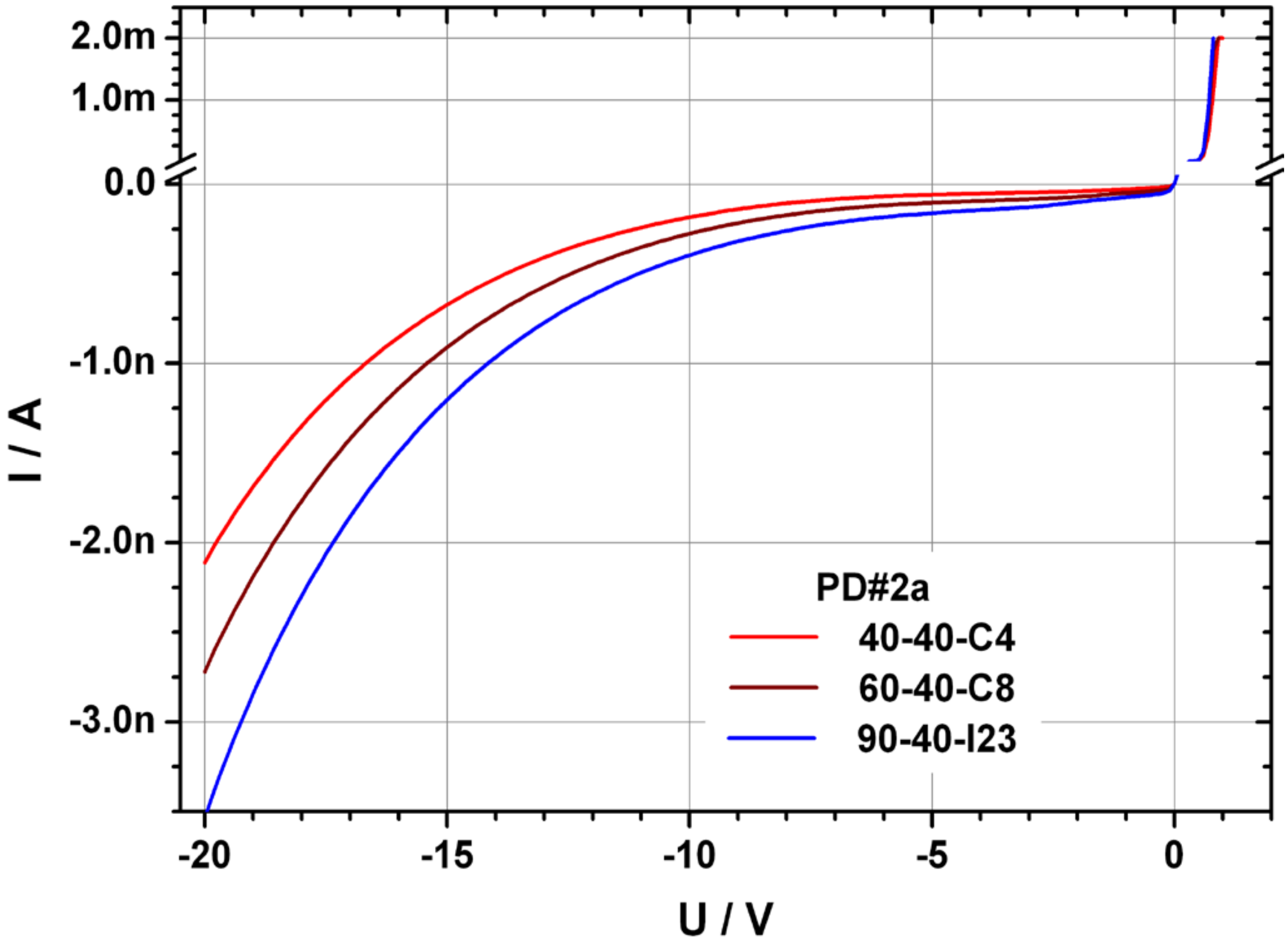
Photodiode performance – discrete chips (1)

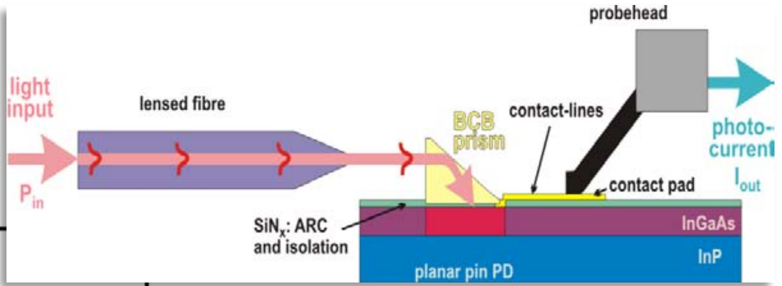


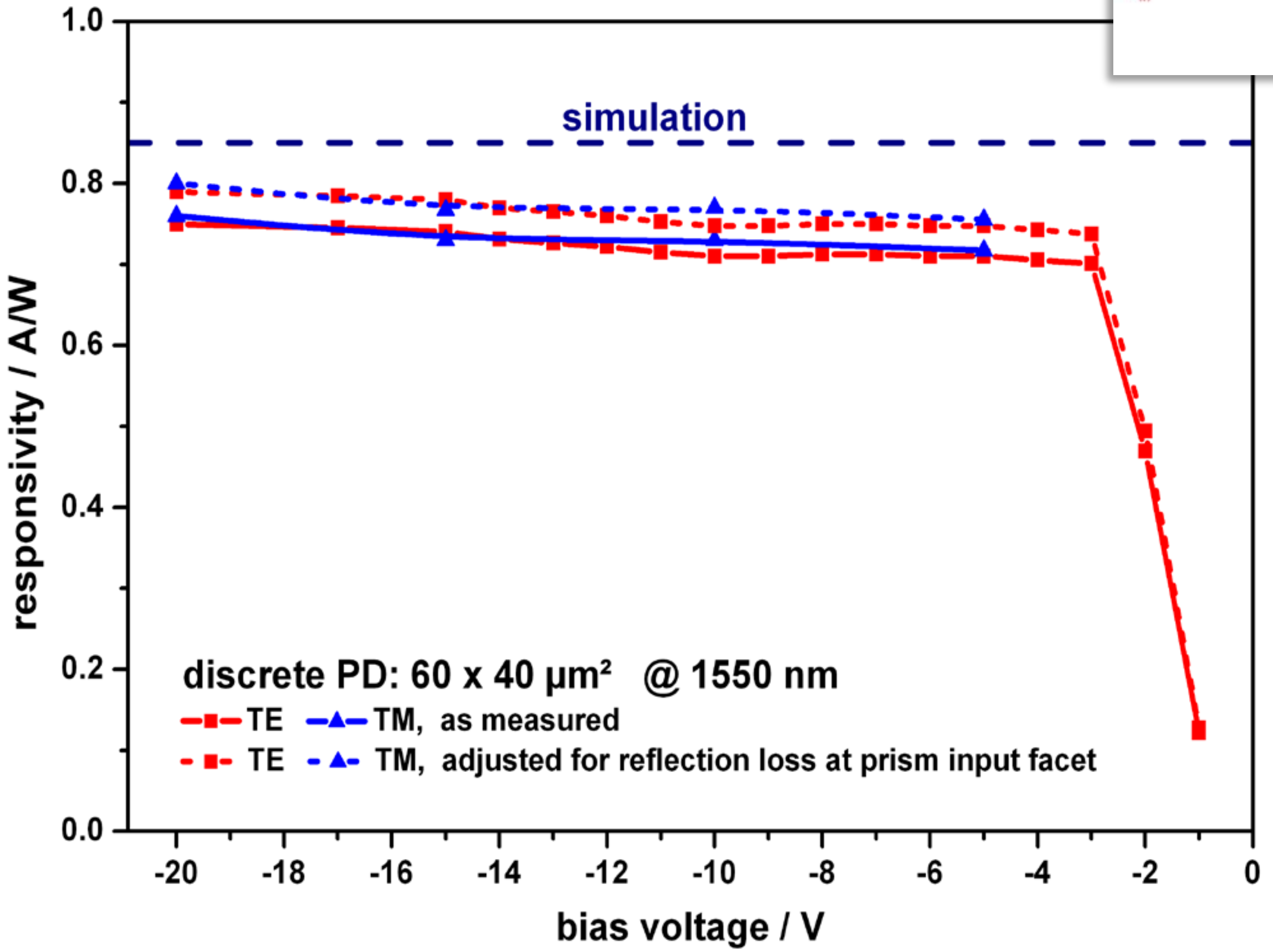
Low dark currents

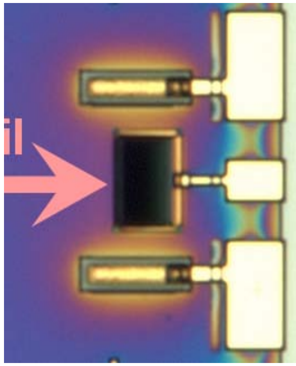
High breakdown voltages

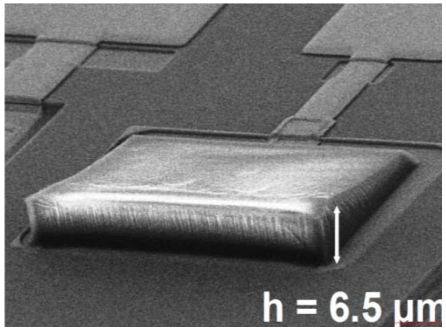
Photodiode performance – discrete chips (2)

High responsivity

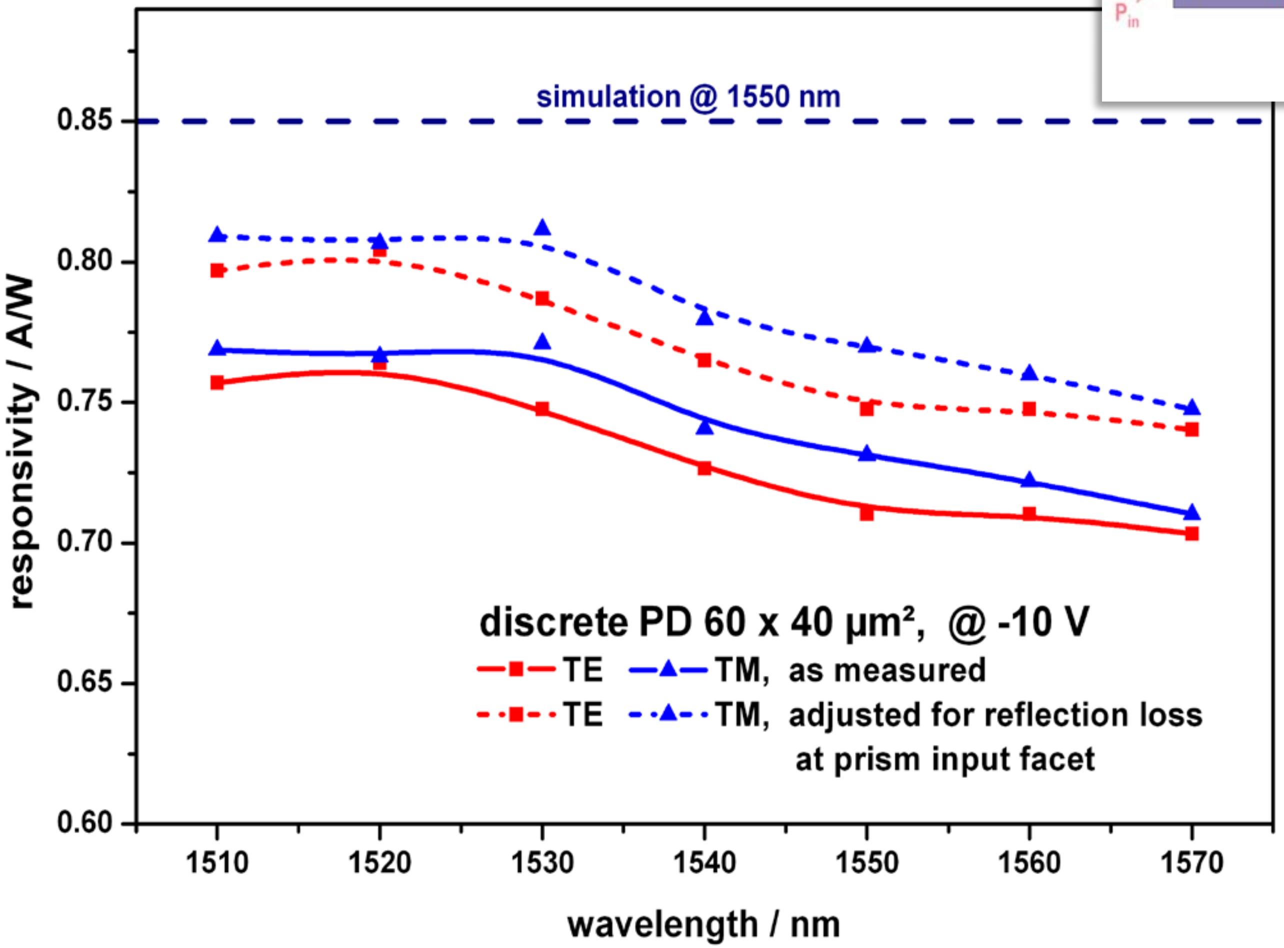


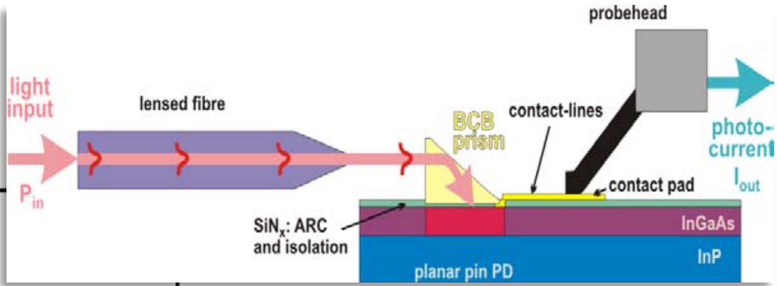


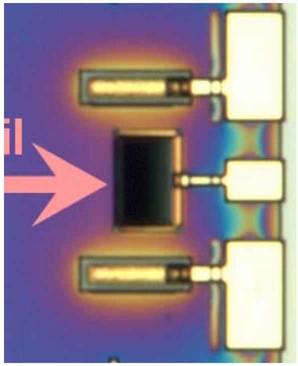




Photodiode performance – discrete chips (3)

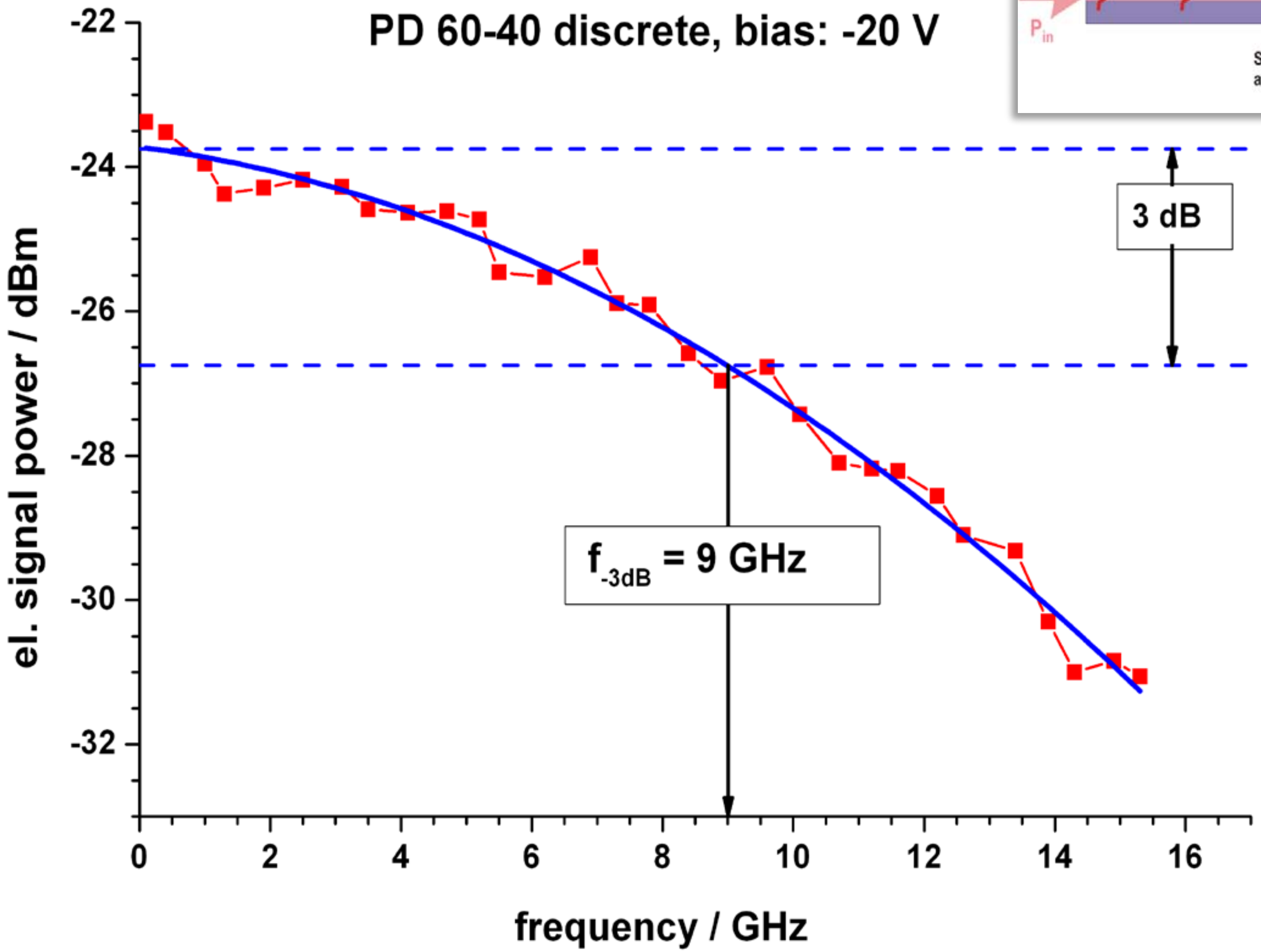


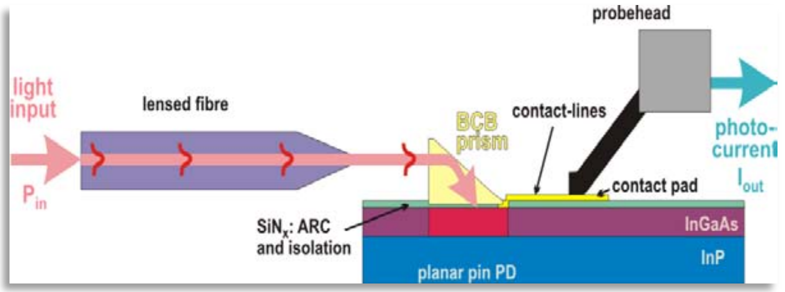


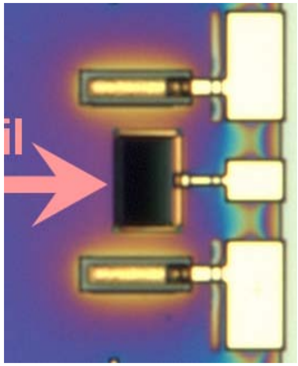


Weak dependence on wavelength and polarization

Photodiode performance – discrete chips (4)





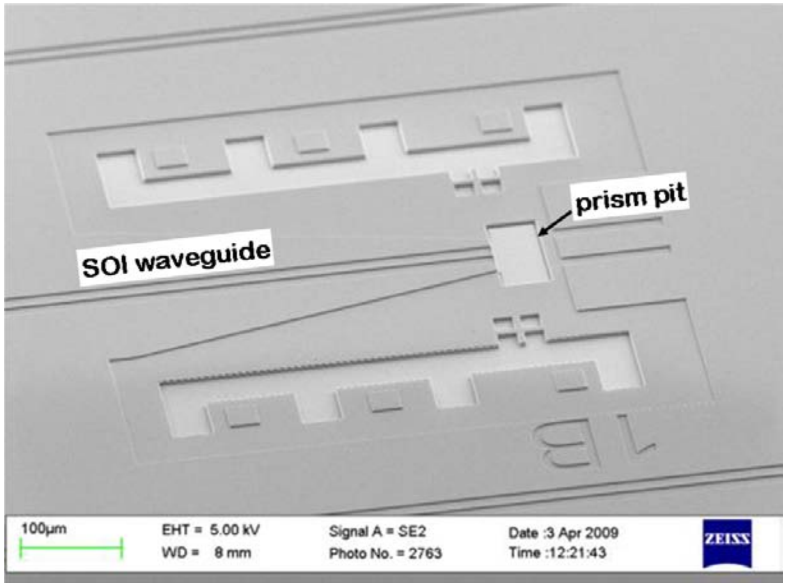


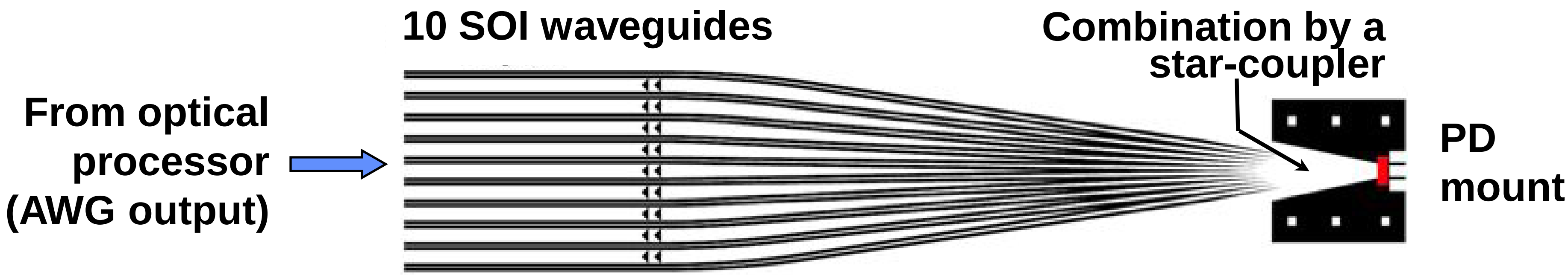
Bandwidth suitable for 10 Gb/s operation

Photodiode integration – PD mount on SOI

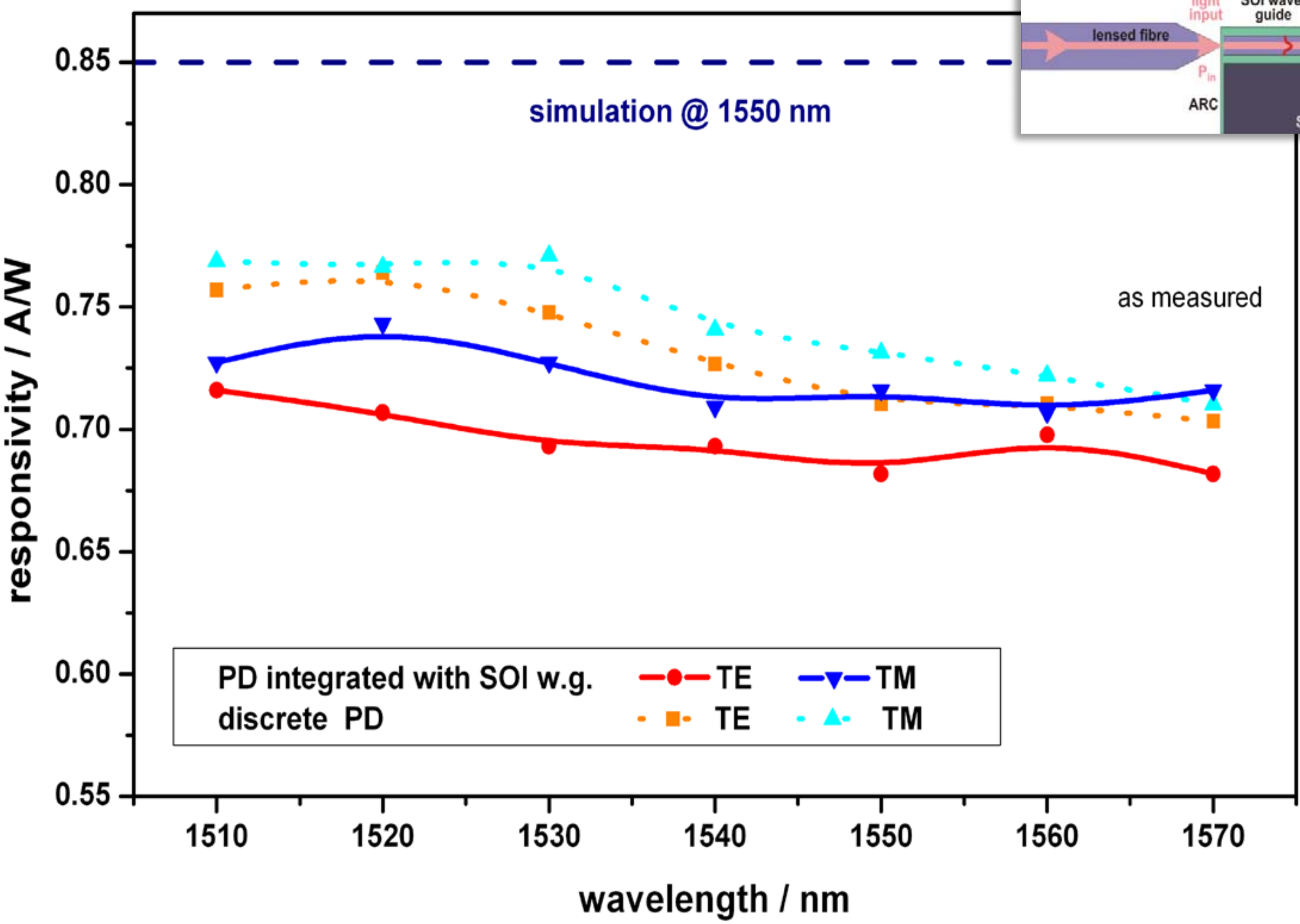
Demands on optical coupling:

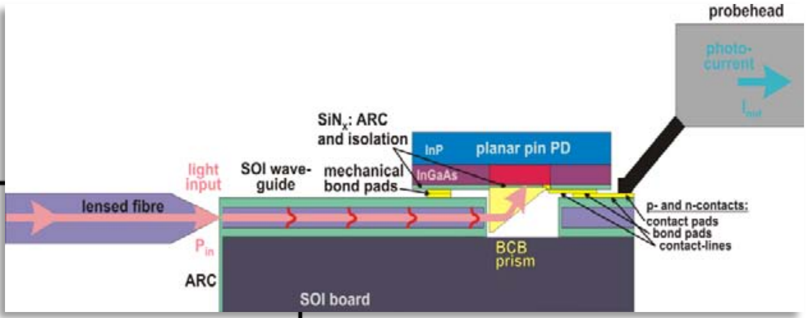
- **high responsivity**
  independent on
  - **wavelength**
  - **polarization**
  - **waveguide position**
- **high bandwidth for 10 Gb/s operation**





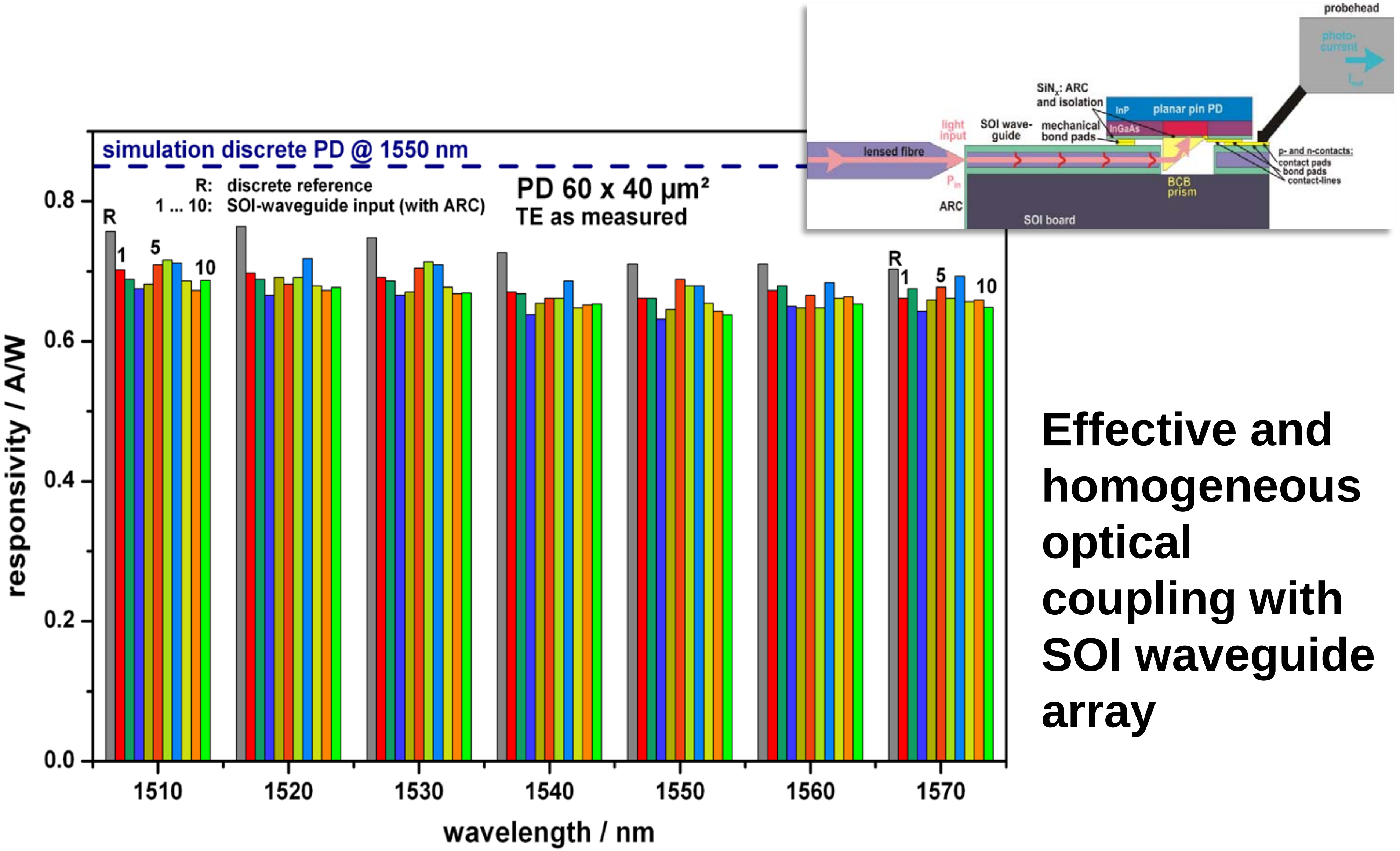
Photodiode performance – chips on SOI (1)





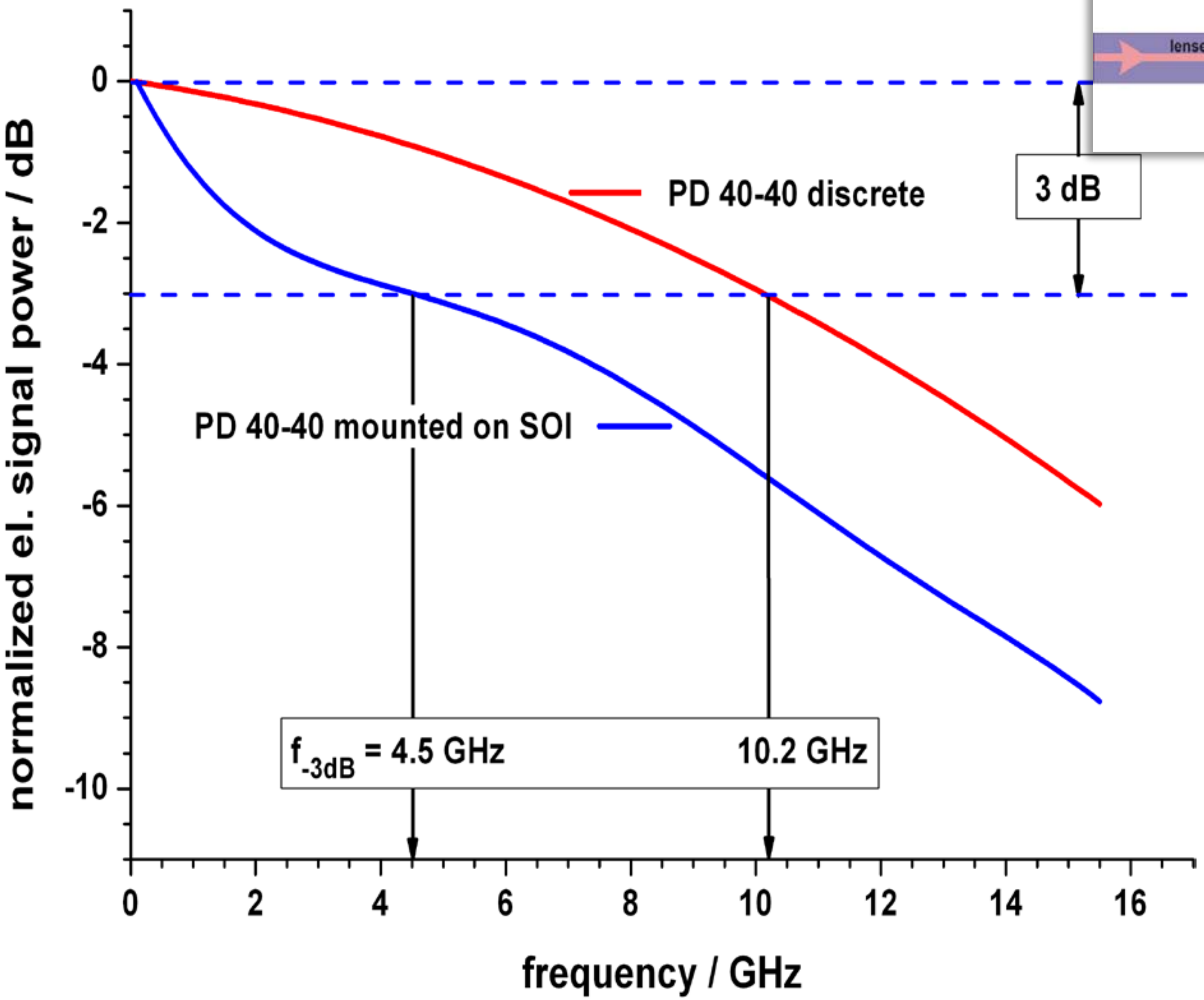
Weak dependence on wave-length and polarization

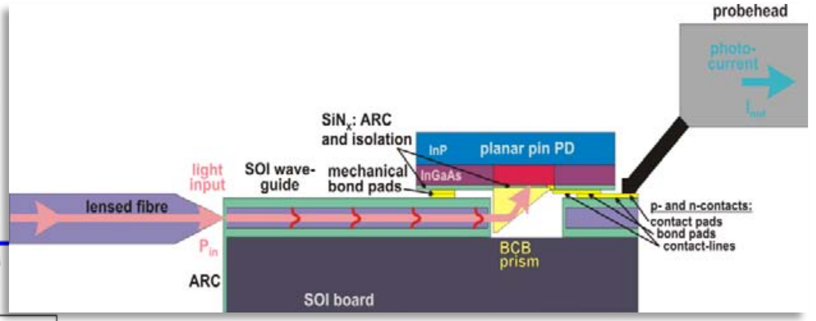
Photodiode performance – chips on SOI (2)



Effective and homogeneous optical coupling with SOI waveguide array

Photodiode performance – chips on SOI (3)

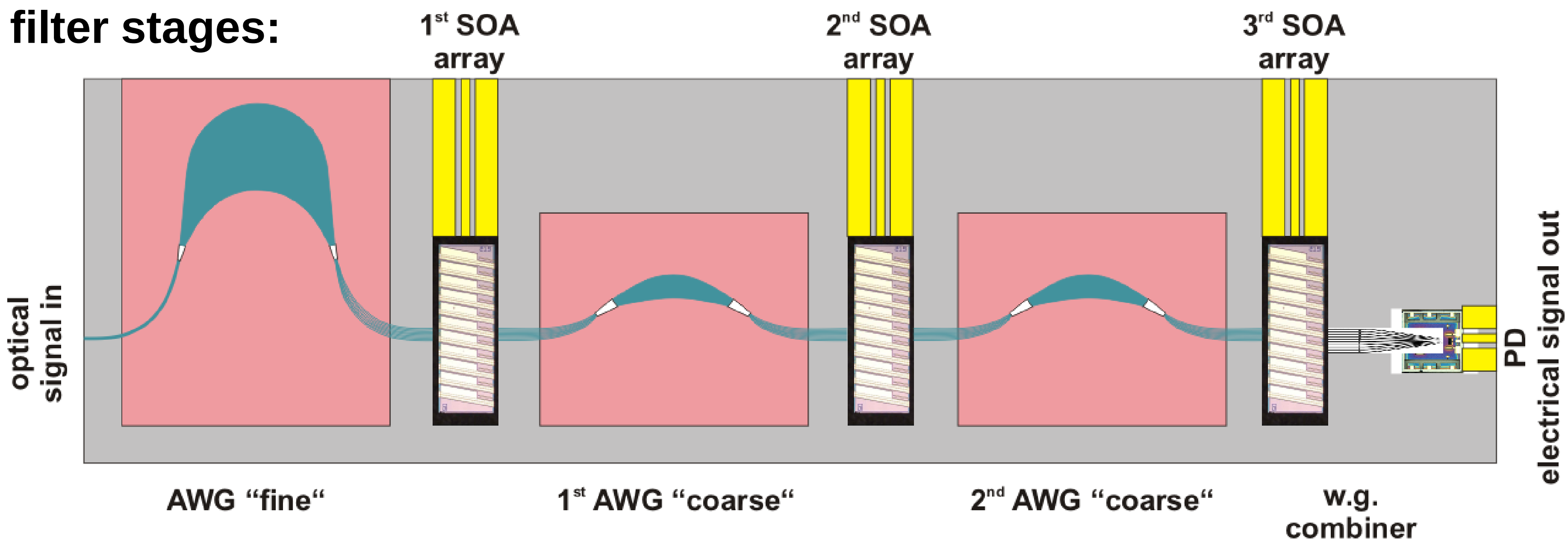




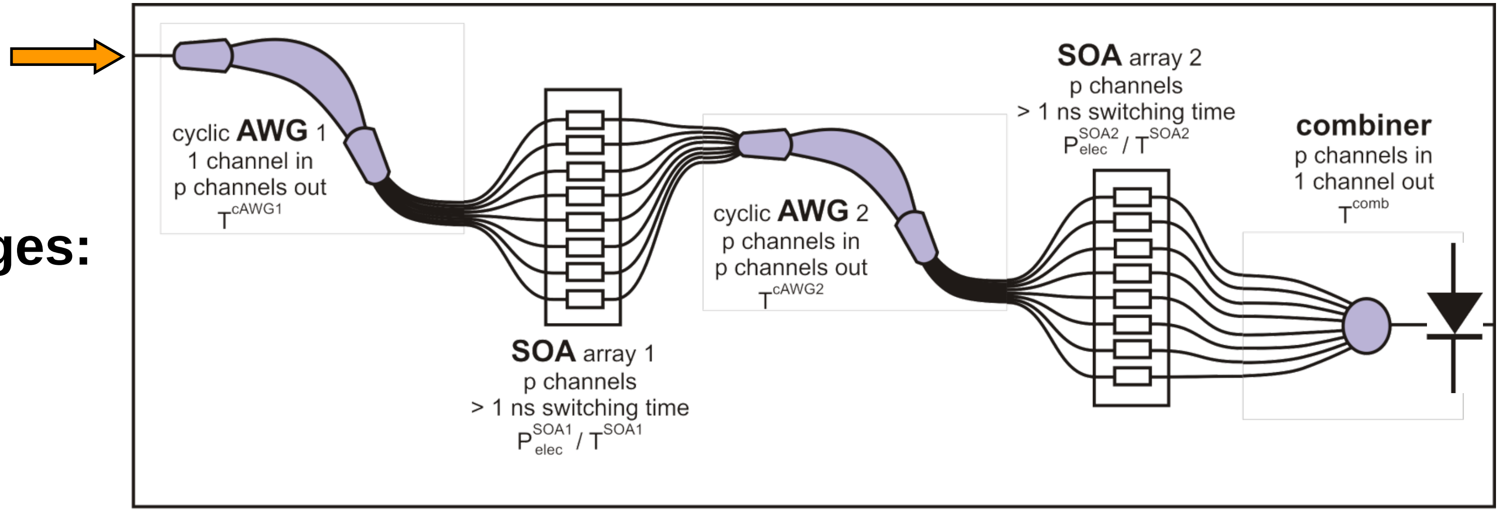
Degradation of bandwidth due to connection via RF line on low resistivity SOI

OTUS channel wavelength filter

3 filter stages:



2 filter stages:



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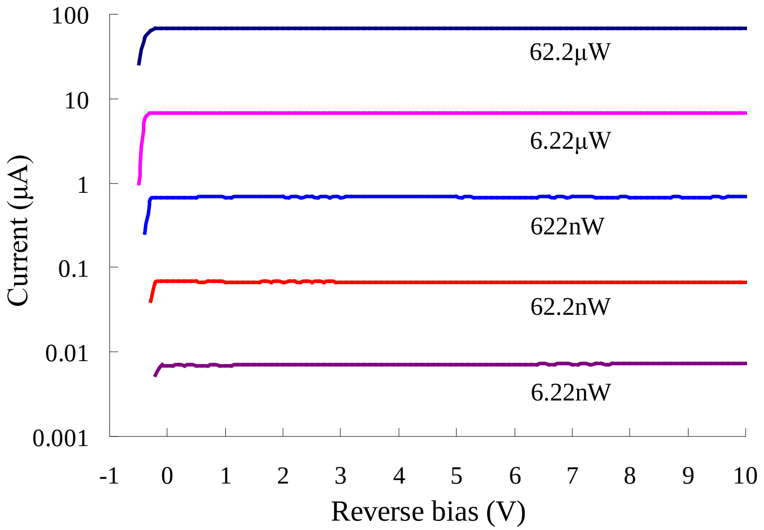
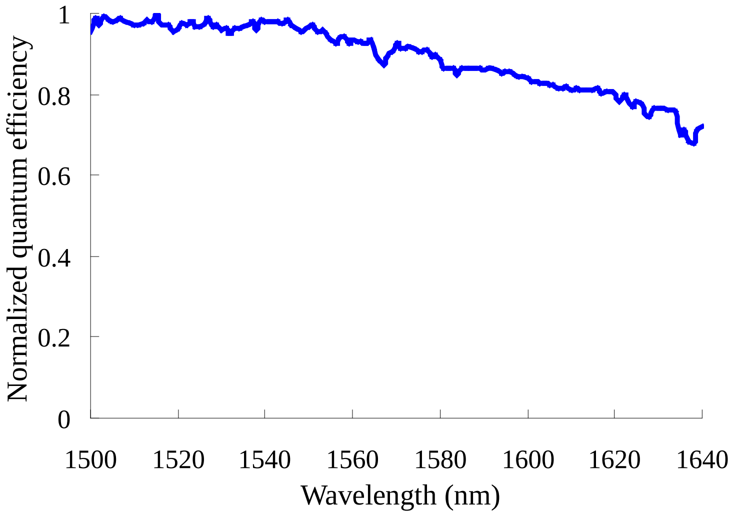
- Conclusion

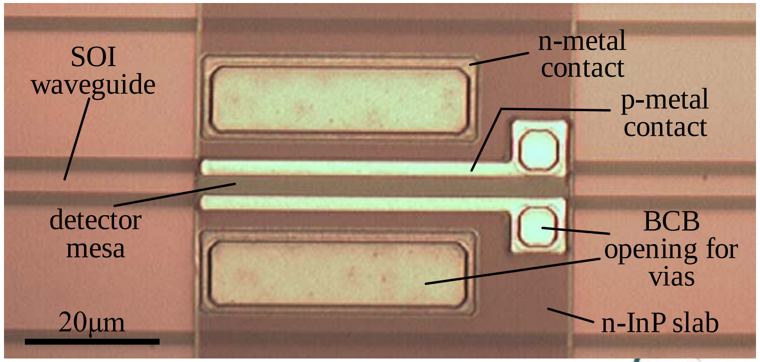
BOOM: Photodetector results

- High responsivity (1.1 A/W @ 1550 nm or 88 % quantum efficiency)
- Covering the whole S, C and L communication band
- Very low dark current 10 pA (needs very low bias voltage)





Top view (before final metallization)

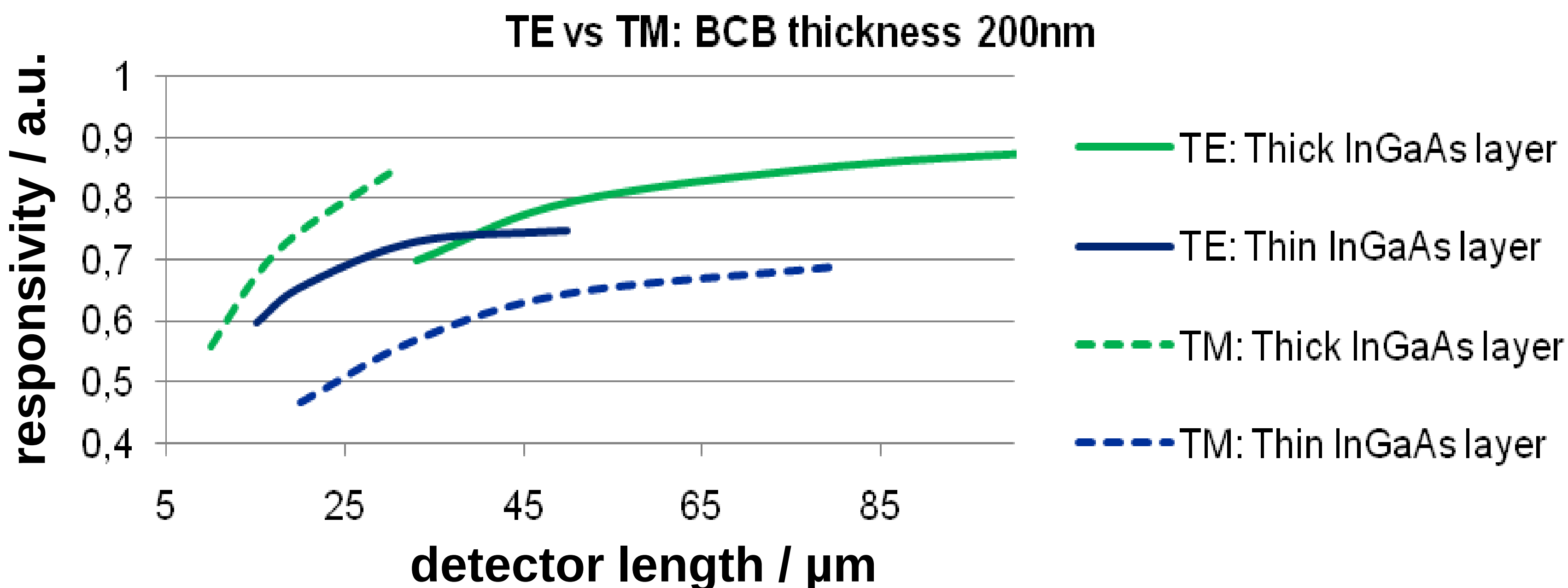


Z. Sheng, OpEx, vol 18(2), 2010

Increase high-speed performance

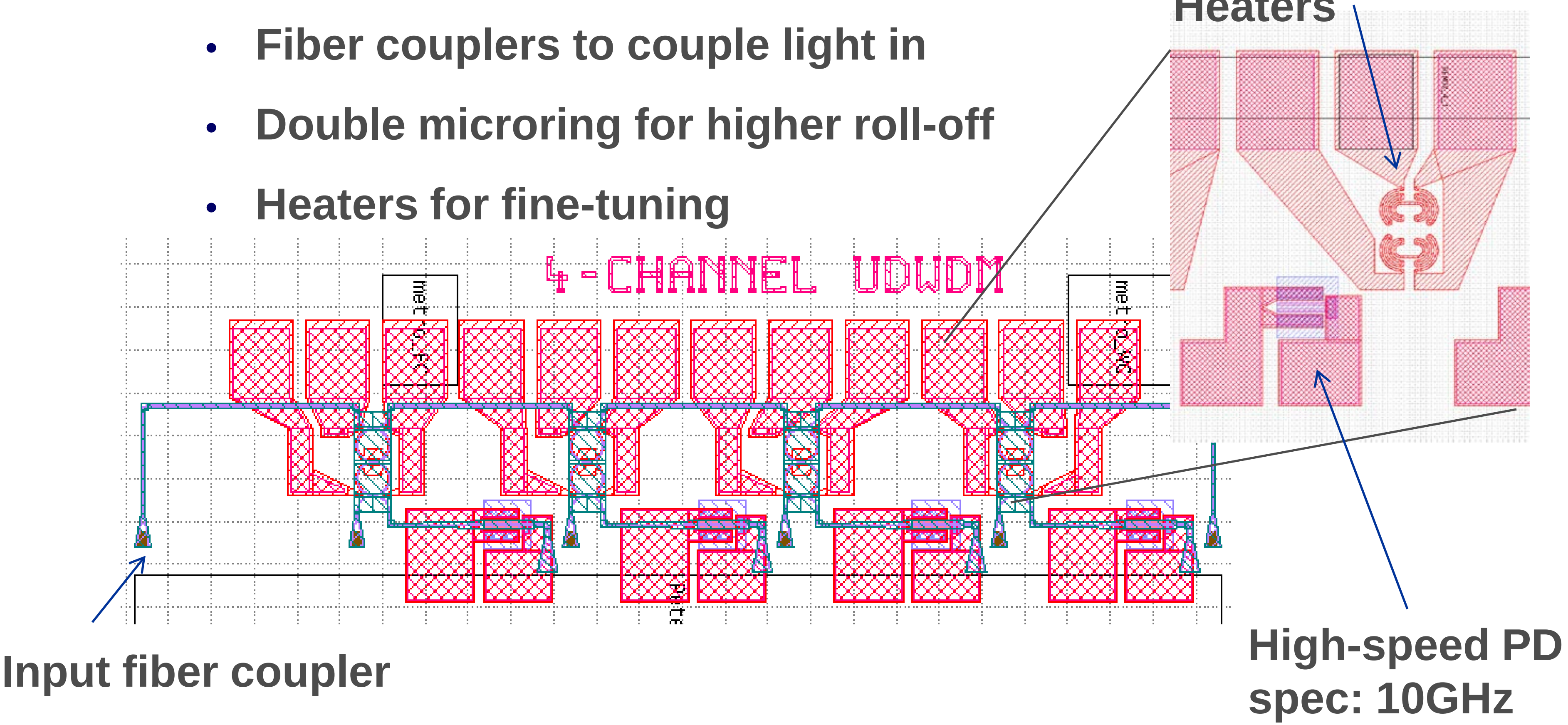
Performance is polarization dependent

- Thin InGaAs: TE higher responsivity & faster power transfer
- Thick InGaAs:
  - TM has a faster power transfer
  - Both polarizations have higher responsivity



BOOM: UDWDM Demultiplexer

- **Design: 4-channel demultiplexer**
  - **Fiber couplers to couple light in**
  - **Double microring for higher roll-off**
  - **Heaters for fine-tuning**



- **Fabrication underway**

Conclusion

- **Successful integration of InP based photodiodes with SOI waveguides via two approaches:**
  prism coupling and evanescent coupling
- **Prism coupling via a BCB prism as add-on on standard photodiode structure:**
  effective, easy to fabricate.
- **Evanescent coupling via InGaAs dies, heterogeneously integrated on top of SOI “nano” waveguides:**
  effective, more sophisticated design and technology
- **Both approaches show high responsivity with low dependence on wavelength, suitable for 10 Gb/s operation**

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Terabit-on-chip:
Micro- and Nano-scale silicon photonic integrated components and sub-systems enabling Tb/s-capacity, scalable and fully integrated photonic routers

SEVENTH FRAMEWORK PROGRAMME

European Commission, STREP - 7th framework programme (ICT-2007-2, Contract no. 224375

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