Realization and Characterization of 8 × 8 Resonant Cavity LED Arrays Mounted onto CMOS Drivers for POF-Based Interchip Interconnections

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***Abstract*— An 8 × 8 array of resonant-cavity light-emitting diodes (RCLED's) emitting at 980 nm and flip-chip mounted onto complimentary metal–oxide–semiconductor (CMOS) integrated drivers, is presented. The RCLED's are optimized for maximal extraction efficiency into the numerical aperture of polymer optical fibers ($NA = 0.5$) and minimal optical crosstalk. Design of the optimal cavity structure is presented, and 8 × 8 arrays are realized and mounted directly onto standard CMOS chips using a solder reflow technique. The CMOS integrated drivers are designed for high-speed operation and low-power consumption, and are realized in 0.8 and 0.6-μm CMOS technology. The electrooptical modules have been realized and characterized, and over 50-μW optical power coupled to POF at 3-mA drive current is reported. Open eye diagrams at operation speed up to 250 Mb/s are presented. These characteristics are compatible with CMOS integrated low-power receivers.**

***Index Terms*— Driver circuits, light-emitting diodes, optical interconnections, resonant cavity.**

I. Introduction

DUE TO THE increasing component density, chip size and clock frequencies, the electrical interconnections in and between chips may present a bottleneck in the next years. Parallel optical interconnect with direct access to any location within a CMOS chip, has been proposed as a solution to the problems inherent to the electrical interconnect [1]. The light sources in these applications must meet specific requirements, as high-efficiency low-beam divergence, low thermal dissipation, electrical compatibility with standard CMOS-circuitry (e.g., drive voltage <3.3 V), high yield, possibility of realization of large arrays and flip-chip mounting compatibility (i.e., through-substrate emitting devices). Resonant-cavity LED's are suitable light sources for that kind of interconnect systems since they can be integrated into large 2-D arrays. Moreover, they have a high efficiency at low current (no threshold), a low thermal and electrical resistance and emit light vertically. Although 2-D arrays of high-performance vertical-cavity surface-emitting lasers (VCSEL's) for optical interconnect applications have been reported recently [2]–[4], we believe that RCLED based interconnect may present a better solution if reliability, yield, price and eye-safety issues become important. Moreover, VCSEL's need a larger voltage drop, because they operate at higher current densities through smaller circuit apertures, implying larger series resistances. On the other hand, VCSELS are inherently faster (due to the fast stimulated emission), emit low-divergent beams (even diffraction limited for single mode VCSEL's) and are more efficient at higher current densities.

Standard planar LED's have a low efficiency due to the total internal reflection at the semiconductor-air interface. However, if the active layer is sandwiched between two mirrors, the microcavity effect alters the radiation pattern, resulting in a more directed beam and smaller emission spectra [5]–[7]. These devices are called RCLED's. Compared to standard LED's, more power is emitted within the solid angle of escape, resulting in an increased extraction efficiency. This effect has been used to increase the total extraction efficiency, up to record values of 22% [8] (this overall quantum efficiency is the combination of the microcavity effect and the photon recycling effect). RCLED's have been used as tunable light sources [9] and are integrated with GaAs driver to built smart pixels [10]. The realization of 8 × 8 arrays of RCLED as a grayscale image display has been reported [11]. However, these RCLED's had an absorbing metal outcoupling mirror, reducing the overall efficiency of the devices.

This paper reports an interchip parallel (8 × 8) polymer optical fiber (POF) based interconnect link using RCLED's as light sources. The envisaged interconnect link is given in Fig. 1, and is part of a system demonstrator, built within the framework of the ESPRIT OIIC project [12]. This demonstrator consists of several optically interconnected field programmable gate ar-

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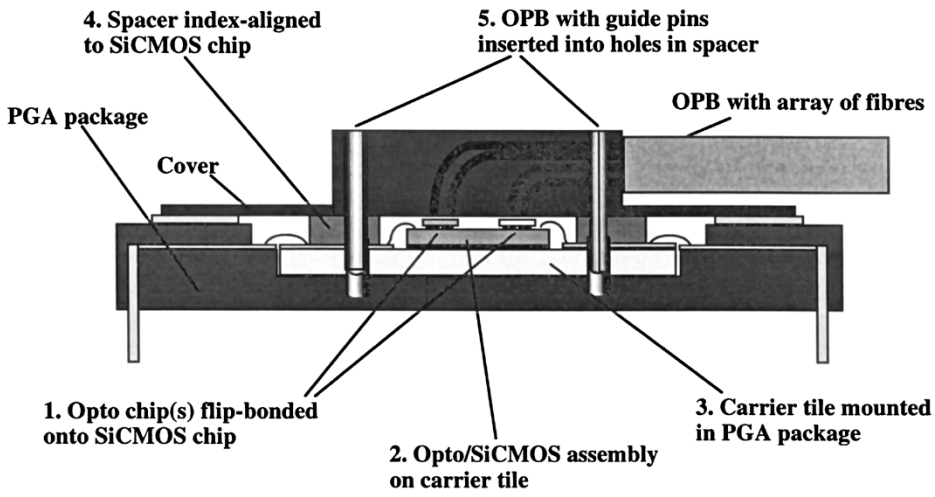

Fig. 1. Demonstrator assembly: Side cross-sectional view.

rays (FPGA's), resulting in a 3D stack of interconnected gates with a low latency and a large programmability flexibility. The 8×8 RCLED array is mounted onto a CMOS chip, containing the FPGA cells and the analog circuitry to drive the RCLED's. The emitted light is coupled into a waveguide system, and detected by InGaAs detectors, which are flip-chip mounted on another CMOS chip. The waveguide system is based on plastic optical fibers (POF's). The POF is cheap, flexible, easily connectable and it has very small bending losses [13]. Moreover, it has a large NA (0.5), allowing much light to be captured in the fiber. Its disadvantages are the high losses (about 12 dB/m at 980 nm). Although green emitting (InGaN-based) LED's seem to be more suitable for POF links [14], InGaAs-based RCLED's are used, because of their intrinsic high internal quantum efficiency. The fiber absorption becomes negligible when short (few tens of centimeters) interconnect links are used. Moreover, the GaAs substrate is transparent at this wavelength, allowing the compact integration of substrate emitting devices on the CMOS.

Other approaches to parallel interconnect include free-space links, waveguide links and fiber bundle links [15]. The free space links are more difficult to fabricate, because the sources, optics and detectors have to be aligned together. The maximal transmission distance is limited by optical crosstalk. They permit higher data densities, as the pitch does not depend on any waveguide dimension. Several free-space links have been demonstrated, most of them using microlens arrays to collimate the light beams (for example, [16]). There have been LED-based CMOS-integrated systems reported using through-Si-substrate light paths [17] The polymer waveguide approach allows communication over longer distances, at the expense of lower data densities. The third option is the fiber bundle approach. It combines long distance datatransmission with the higher data density [18]. However, these waveguides have typical large numerical apertures, resulting in a very broad emission pattern at the outcoupling side. This results in more crosstalk at this side of the link, unless buttcoupling of the fiber bundle and detector is used.

In this paper, we describe the RCLED-CMOS module. In paragraph II, the design of the RCLED will be discussed, with emphasis on the optimization of the layer structure to maximize the extraction efficiency into a given NA. The realization of the device will be discussed in paragraph III. The design of the CMOS driver will be discussed in paragraph IV. Paragraph V will discuss the mounting issues : first the backprocessing of the CMOS chip, followed by the mounting of the arrays using a solder reflow technique. The measurements on the single and mounted devices will be presented in paragraph VI.

II. Design of RCLED Optimized for Coupling in NA

This paragraph describes the optimization of the RCLED structure for maximal coupling into the POF. The quality of the coupling is described by the overall quantum efficiency (QE). This parameter is given by the product of the extraction efficiency, the injection efficiency and the internal quantum efficiency. The injection efficiency is defined as the part of the current that is injected in the active region and depends on the geometry of the device and the current density. The device structure is shown in Fig. 2. The current is injected through the gold contact which also serves as the upper mirror of the cavity. To reduce the surface recombination, and increase the injection efficiency, the mesa diameter was choosen 20 μm longer than the contact diameter. The internal QE is determined by the ratio of the radiative recombination to the nonradiative recombination, and depends strongly on the material quality of the active layer. The RCLED's have high-quality InGaAs quantum wells, with an estimated internal quantum efficiency of over 80%.

The extraction efficiency of LED's is defined as the fraction of the internally generated light which escapes the device. However, the internal light generation is isotropic, and most light is reflected at the semiconductor–air boundary, and is lost by absorption in the substrate. This results in small extraction efficiencies (2% for GaAs-based devices).

There are several ways to increase the extraction efficiency of LED's. In single devices, it is possible to extract the light from the sidewalls [19]. However, this approach is not compatible with the integration in arrays. Another technique make use of the reabsorption of the internally emitted light by the active layer, followed by reemission, with a new

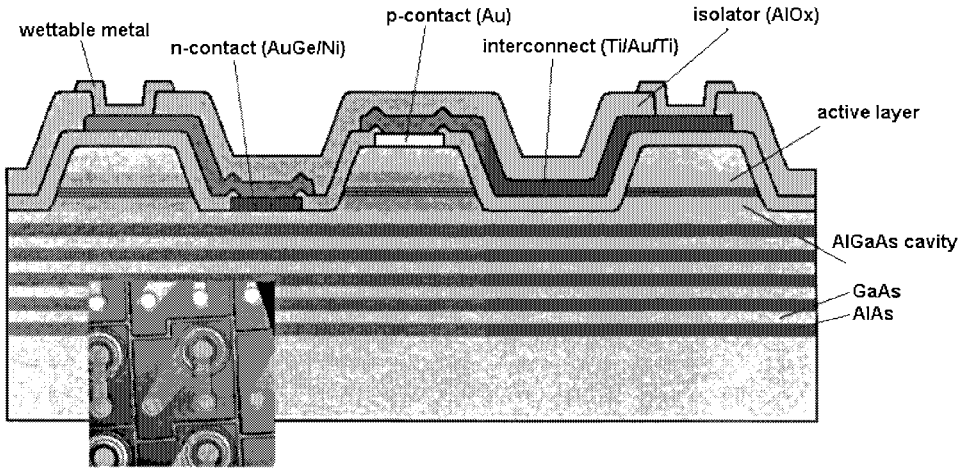

Fig. 2. Sectional view of processed RCLED. (Inset: photograph of RCLED).

chance to escape the device [20]. However, this process slows down the emission dynamics. LED's with roughened surfaces also show high extraction efficiencies, as the light is reflected at the irregular interface until it intercepts the boundary at a small angle and escapes the cavity [21], [22]. Up to now, this roughening technique is not demonstrated on CMOS-mounted devices. In this paper, devices with increased extraction efficiency, based on the microcavity effect, are presented.

Fermi's Golden Rule predicts that the spontaneous emission into a certain optical mode depends on the optical mode density and the dipole matrix element [23]. This means that, in an RCLED, the spontaneous emission in a certain direction at a certain wavelength can be enhanced or inhibited. This effect depends on the amplitude of the standing wave at the active layer. The amplitude of the electric field at the active layer depends on the propagation direction, the wavelength and the cavity parameters. The cavity enhancement is defined as the ratio of the emission lifetime inside the microcavity to the emission lifetime in free space. Fermi's Golden rule implies that this cavity enhancement factor equals the ratio of the magnitude of the electrical field inside the cavity to the magnitude of the electric field as if there was no cavity. This cavity enhancement factor depends on the cavity parameters and the wavelength. The Fabry–Perot cavity parameters (that is the cavity thickness and the mirror reflectivities) must be designed to maximize the emission into the desired direction and at the desired wavelength. This is done by maximizing the cavity enhancement factor for the given wavelength and propagation direction. In this short-distance interconnect application, the emitted spectrum is of no importance, and the cavity is designed to maximize the extraction efficiency into the given NA.

Fig. 3 shows a representation of the intrinsic spontaneous emission and the cavity enhancement (or inhibition) in k-space [24], [25]. A vector in this k-space presents a planar wave, travelling in the direction of the vector. The magnitude of this vector is inversely proportional to the wavelength ($k = 2\pi/\lambda$). In this k-space, the amplitude of the intrinsic spontaneous emission at a certain wavelength is represented by a grayscale

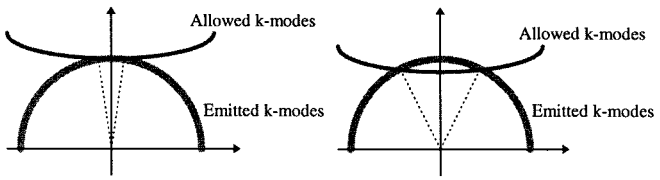

Fig. 3. k-space representation of microcavity enhancement and intrinsic spontaneous emission.

value. The cavity enhancement factor is represented by the black curve (see Fig. 3). The internal emission pattern of the active layer inside the cavity consists of the product of the intrinsic emission pattern and the cavity enhancement.

The intrinsic spontaneous emission is isotropic: the active layer emits light in all directions with a certain spectral distribution. In k-space, this can be represented as a spherical shell with a thickness proportional to the spectral width of the spontaneous emission spectrum. The cavity enhancement in a certain direction is maximized if the resonance condition is fulfilled. The resonance condition implies that the phase round-trip of the cavity is an integer times 2π. This condition direction can be written as

$$-2k\cos(\theta)nL + \varphi(k,\theta) = m2\pi, \qquad (\varphi(k,\theta) = \varphi_1(k,\theta) + \varphi_2(k,\theta)). \qquad (1)$$

This condition determines the relationship between the cavity length L, the cavity resonance k_{res} (related to the cavity resonance wavelength λ_{res}) and the order of the mode m. $\phi_1(\phi_2)$ is the phase of the reflection of the upper (bottom) mirror. In general, this phase depends on the wavelength and propagation direction. In case of a DBR, this phase dependency is described by a penetration depth.

The maximum of the cavity enhancement is represented by flat planes. Extensive numerical simulation have shown that the resonance plane of metal mirror/DBR cavities is curved. The flat plane approximation is only valid for almost perpendicular propagating planar waves. This is justified, as the realistic RCLED's consist of high-index materials, and only the (almost) perpendicular directions escape the cavity and build up the external emission pattern (= in air). This

approximation is valid to investigate the far field pattern of the RCLED's. However, this k-space picture is not valid to predict the change in spontaneous emission lifetime in the cavity, as this spontaneous emission lifetime is determined by the complete internal emission pattern. Other authors have investigated the change in spontaneous emission lifetime in planar microcavities consisting of a metal mirror and a DBR, and indicated that the change in spontaneous emission lifetime is small, certainly if this enhancement is averaged over all emitted wavelengths [26]. In conclusion, this approximation gives us a qualitative method to investigate the influence of the detuning of the cavity resonance.

The emission in perpendicular direction is optimally enhanced if the intrinsic spontaneous emission peak wavelength equals the cavity resonance wavelength (resulting in a "resonant cavity"). However, to maximize the extraction efficiency in a given NA, the position of the plane should not necessary coincide with the top of the intrinsic emission sphere. There is an optimal "detuning," as shown in Fig. 3. This detuning also influences strongly the external emission profile. The emission profile of the overtuned cavities (cavity thickness larger than the cavity resonance thickness) obtains its maximum at nonperpendicular directions, as the cavity enhancement plane cuts the intrinsic emission sphere. This resulting broad emission profile ("rabbit-ears" like) is highly undesirable in parallel interconnect systems, as the crosstalk to neighboring channels is increased. These rabbit-ears are an unavoidable property of highly efficient RCLED's [27], [28]. The external emission profile of an undertuned cavity (cavity thickness smaller than the cavity resonance thickness) is narrower, but the total overlap is also smaller, and the total extraction efficiency decreases.

The reflectivity of the mirrors determine the peak value and the spectral width of the cavity enhancement factor. To maximize the extraction efficiency, the peak value must be large (indicating a high Q-factor) and the whole intrinsic emission spectrum must be enhanced (indicating a moderate Q-factor).

A numerical tool was developed to calculate the extraction efficiency of planar LED's [29], [30]. The accuracy of the calculated characteristics of the microcavity rely on the accurate presentation of the intrinsic spontraneous emission profile. The spontaneous emission in the InGaAs quantum well is presented by horizontally oriented electric dipoles [31]. This corresponds to the heavy hole–electron recombination, which appears to be the dominant transition in the strained InGaAs quantum wells. The emission pattern of the dipoles inside the cavity is calculated by expanding the field of the dipoles into a set of planar waves. This tool takes also the photon recycling into account: a part of the emitted light is captured in a lateral waveguide mode, defined by the metal mirror, the cavity and the DBR. This light can be reabsorped by the active layer, and again be emitted. This effect increases the apparent internal QE, as a photon has more chance to escape the cavity. However, this effect is negligible at high current densities (as the reabsorption of the active layer decreases [32]), and for small diameter LED's (as most of the light escapes the cavity laterally before it is reabsorbed). RCLED's for parallel interconnect applications are typically small (to capture all the external emitted light in the fiber) and driven at relatively high current densities (to increase the modulation speed). For this reason, the recycling effect in neglected.

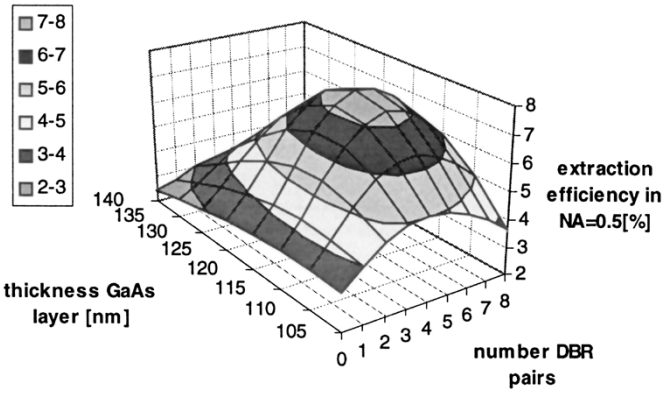

Fig. 4. Simulated extraction efficiency as function of the thickness of the phase matching GaAs layer and of the outcoupling mirror reflectivity.

The exact extraction efficiency, taking into account the full angle and wavelength dependence of the mirrors and the Purcell effect (i.e., the change of the spontaneous emission lifetime in the cavity as compared to the lifetime in free space), were calculated to get an accurate value of the extraction efficiency. The results are summarized in Fig. 4, where the extraction efficiency into NA $= 0.5$ is plotted as a function of the thickness of the GaAs phase matching layer and the number of DBR pairs. The intrinsic spontaneous emission spectrum is assumed to be Gaussian-like, with a FWHM of 30 nm (corresponding to a current density in the order of 100 A/cm^2) and peak wavelength at 980 nm. No photon recycling is taken into account. The evanescent coupling of optical modes to the absorbing metal mirror is neglected, because the large distance between the active layer and the gold contact. The optimal GaAs layer thickness was found to be 121 nm, the corresponding cavity resonance wavelength is 981 nm. This cavity is slightly overtuned: the design results in an optimized extraction efficiency into NA $= 0.5$, whereas a perfect tuned cavity (resonance wavelength is 980 nm) maximizes the overlap in perpendicular direction. The optimal reflection of the DBR (at an intrinsic spontaneous emission spectral width of 30 nm), is 70.8% amplitude reflection (50.2% power reflection), corresponding to a five-pair GaAs–AlAs DBR. For the given device structure, the maximal extraction efficiency into NA $= 0.5$ is found to be 7.8%. In that case, the total extraction efficiency is 19.7%.

III. Realization of RCLED Array

A. Growth of the Layer Structure

The designed layer structure is grown in a horizontal MOCVD-reactor at low pressure (76 torr). Source materials are arsine (AsH_3) for As, TMG (Trimethylgallium) for gallium, TMA (trimethylaluminum) for aluminum, TMI (trimethylindium) for indium. N-dopant is Si (source material SiH_4), p-dopant is Zn (source material is DEZ-DiEthylZinc). After growing a 200-nm-thick buffer layer, the cavity was

grown, consisting of a five-pair Si-doped ($n = 5\ 10^{17}$) AlAs–GaAs DBR, followed by a 50.6-nm-thick $Al_{40}Ga_{60}As$ spacer, of which 40 nm was n-doped. The active layer consists of 3 $In_{20}Ga_{80}As$ quantum wells (thickness is 6 nm) and 6-nm $Al_{20}Ga_{80}As$ barriers. To obtain better interfaces, a 2-nm-thick GaAs layer was inserted between the well and the barrier material. The growth temperature of the active layer (650 °C) was optimized to maximize the photocurrent peak [33]. Above the active layer, a 50.6-nm-thick $Al_{40}Ga_{60}As$ upper spacer was grown, of which 20 nm was undoped, and the remaining 30.6-nm Zn doped ($p = 5\ 10^{17}$). Finally, a 120-nm-thick p-doped GaAs phase matching layer was grown, of which the upper 40 nm was p^{++} ($p = 2\ 10^{19}$) doped. The growth temperature for AlGaAs cavity and DBR was 700 °C.

B. Processing of the RCLED's

Several RCLED arrays, compatible with solder reflow flip-chip mounting, were realized. A cross section of the RCLED is schematically represented in Fig. 2. The processing starts with (wet) mesa etching. The n-metallization (Au–Ge–Ni) is deposited in the moat, followed by an alloy step to reduce the ohmic resistance of the contact. Then the Au p-metal, also serving as highly reflecting mirror, is deposited. After that step, no high-temperature steps are allowed, because this would degrade the highly reflecting GaAs–Au interface. Afterwards, a first isolation (120-nm Al_2O_3) is deposited at room temperature, followed by the interconnect wiring (Ti–Au). The postprocessing of the devices, necessary for the flip-chipping, consisted of a second isolation (400 nm Al_2O_3), and a wettable metal deposition. In a first processing, Pt was used as diffusion barrier. In order to relief the stress induced by the Pt, a rather complex metallization was used: Ti–Cu–Ti–Pt–Au. 5-μm-thick Sn–Pb solder was deposited.

Three different mesas and mirror diameters are available: 70-μm mesa (with 50-μm mirror), 52-μm mesa (with 32-μm diameter) and 40-μm mesa (with 20-μm mesa). The mirror diameter is 20 μm smaller than the mesa to reduce the nonradiative surface recombination by reducing the current density at the border of the device. This also influences the injection efficiency, since a part of the current flows next to the mirror. Fig. 2 shows the 70-μm mesa (50-μm mirror) devices.

IV. CMOS Integrated Drivers

The LED driver array design aims at high-speed operation, uniform current switching while keeping minimal silicon area, minimal power consumption and minimal supply noise injection. The RCLED forward voltage leaves only a small headroom to the 3.3-V supply voltage. In this paper, we choose differential current switching. In this configuration, the current drawn from the supply lines is constant. The concept minimizes supply noise, and introduces a better signal integrity of the mixed analog–digital CMOS chip. It also allows high speed operation, but increases the power consumption as compared to single ended switching. A constant modulation current is switched between the driver output and an internal dummy load (Fig. 5). The switching circuit is realized by pMOS field effect transistors in common source configuration. The

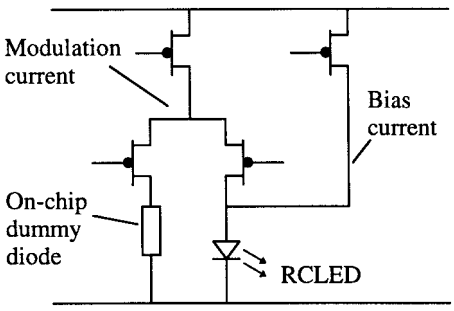

Fig. 5. RCLED driver principle.

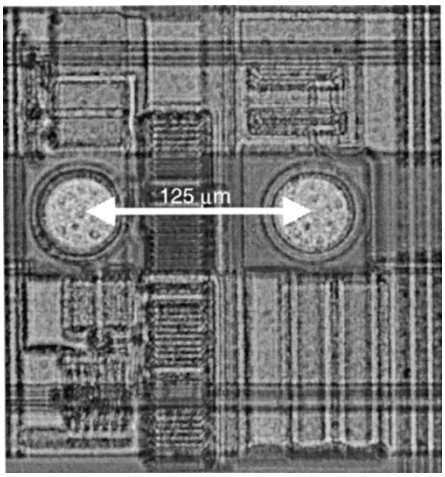

Fig. 6. Picture of a single driver cell. On the left the solder bump contact of driver output and on the right the solder bump contact for ground connection, connecting to LED p- and n-electrodes.

differential, skew-free CMOS signals to control the switching circuit are generated by two inverter chains having the same delay but the inverse polarity. The current sources are realized by current mirrors, where a reference current has to be supplied externally.

The operating speed of the driver is determined by three delays: RC delay of wiring, switching delay, RC delay of driver-LED interface. The RC delay caused by interconnects can limit the speed if not properly designed. The switching delay depends mainly on the technology used. The RC delay of driver-LED can limit the speed, if series resistance of LED and capacitance seen at driver's output are too high. Power dissipated on the driver chip depends on supply voltage, LED forward voltage, driving currents and number of used CMOS inverter gates.

The main part of chip area of a single driver cell is used by the current source transistors. The dimensioning of these transistors is strong correlated with desired maximal driving currents and matching criteria. To achieve high matching (below 2%) no minimal gate length should be used.

The LED driver chips have been implemented in commercially available 0.8- and 0.6-μm CMOS technologies. A single driver cell of a 2×8 array is shown in Fig. 6. Special test chips have been designed to characterize a single driver cell. These chips have been measured in a free space optical link setup. We could operate the drivers with a low impedance VCSEL

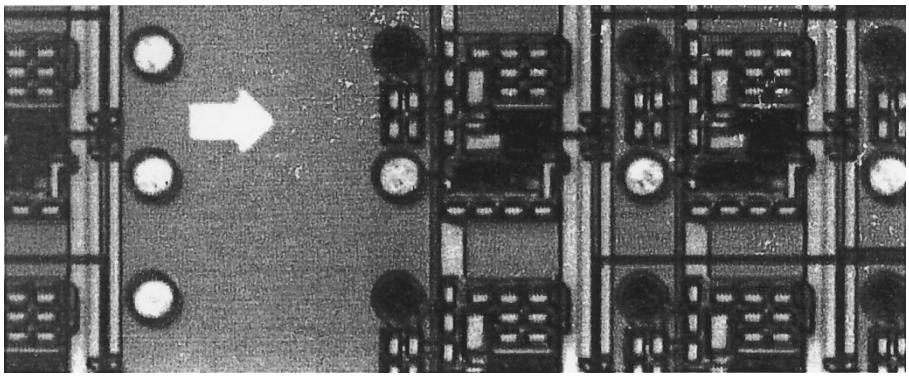

Fig. 7. Photograph of an array of gold-terminated solder pads and alignment marks on CMOS.

from DC up to a bitrate of 600 Mb/s (0.8-μm CMOS) and 800 Mb/s (0.6-μm CMOS), respectively.

V. Realization of the RCLED-Driver Array

A. A Backprocessing of the CMOS

Standard bonding pads on CMOS chips are made of aluminum. This metal oxidizes in air, and the resulting aluminum oxide skin is responsible for unreproducible and large contact resistances. Moreover, solder metal (PbSn) does not wet aluminum, and therefore solder balls do not adhere to aluminum bonding pads. Furthermore, PbSn diffuses into other metals, and can cause reliability problems in the CMOS chip. For these reasons, CMOS chips have to undergo postprocessing prior to the flip-chip process.

Photoresist is spin-coated on the CMOS wafer, and the area of the bonding pads intended to accept solder are opened by contact exposure and development of the resist. The wafer is loaded in a metal sputtering system. In the sputter system, the exposed bonding pads are cleaned from aluminum oxide by Argon sputtering. Without breaking the vacuum, this treatment is followed by sputtering of about 10 nm of Ti, 130 nm of Pt and 20 nm of Ni, followed by evaporation of 30 nm of Au. The metal pads are then defined by liftoff in an ultrasonic acetone bath. The platinum serves as diffusion barrier to solder. The gold defines the solder-wettable pad. The standard dielectric layers that cover the CMOS chip and that surround the gold-covered pads act as nonwettable layer to stop the flowing of the solder at the bonding pad edges. Fig. 7 shows a photograph of an array of gold-terminated solder pads and alignment marks on CMOS.

B. Mounting of RCLED's

Key requirements for the hybridization of optoelectronic arrays on silicon CMOS are: electrical interfaces with minimal crosstalk, compatible with high data rates; efficient thermal dissipation path; minimal modifications to the Si CMOS or the opto devices; low-stress mounting to avoid compromising reliability; and correct registration of array elements. A hybrid flip-chip solder bonding process developed for mounting and aligning optoelectronic devices has been developed and extended to apply to 2-D arrays of both sources and detectors. This relies on molten PbSn solder minimizing surface tension,

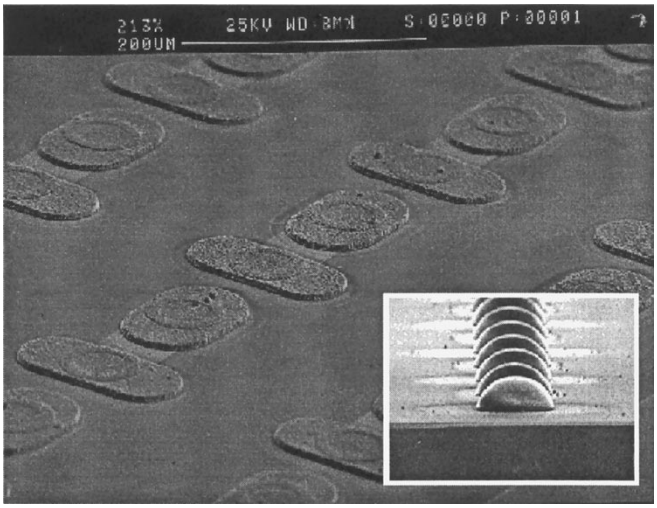

Fig. 8. Oval solder pads prior to reflow (inset: solder pads reflowed into solder bumps).

pulling the array from an initially poor (up to 30 μ m) misalignment into a well aligned (± 2 μm) position [34]. Careful control of the volume of solder evaporated on the wafer, and constraint by nonsolder-wettable dielectric regions around the solder-wettable pads limits the variation in bond height to <3 μm. A common pad grid has been devised for both source and detector array chips to give alignment, mechanical support, a thermal path and low-capacitance interconnect.

To minimize the postprocess requirements on the Si CMOS, the solder is deposited on the optoelectronic device wafer during chip fabrication. On the Si CMOS devices, the normal chip passivation acts as a nonsolder wet layer so the only postprocess operation required is the deposition of solder-wettable pads to match the solder bumps on the opto devices. The optoelectronic device wafers are required to tolerate the solder reflow temperature of $\sim$230 °C. Three additional process steps are needed on the RCLED wafer: patterning of a nonsolder-wettable dielectric layer with vias to access the interconnect tracks; deposition of solder-wettable pads 60 μm diameter, correctly set in registration with the active elements, terminating the interconnect tracks to the active regions; and deposition of solder layers over the pads. The solder is defined by a float-off process into oval pads (Fig. 8). The solder is flowed into near-hemispherical bumps in the presence of flux, pulling-in off the nonwet areas (Fig. 8 inset). Test diodes were

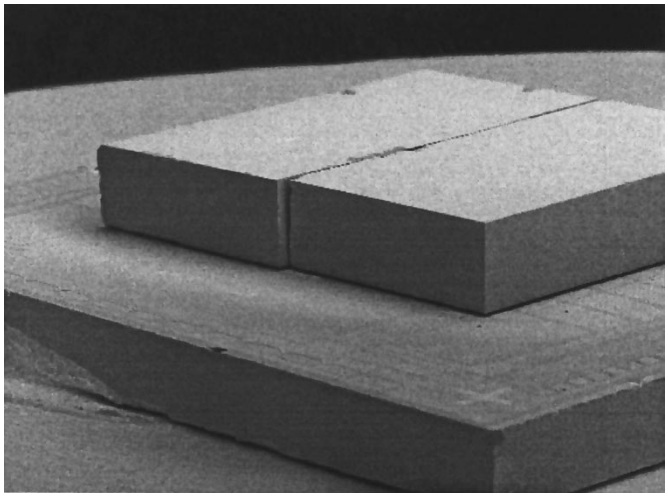

Fig. 9. Two (4 × 8) RCLED array chips mounted side-by-side on a Si CMOS chip.

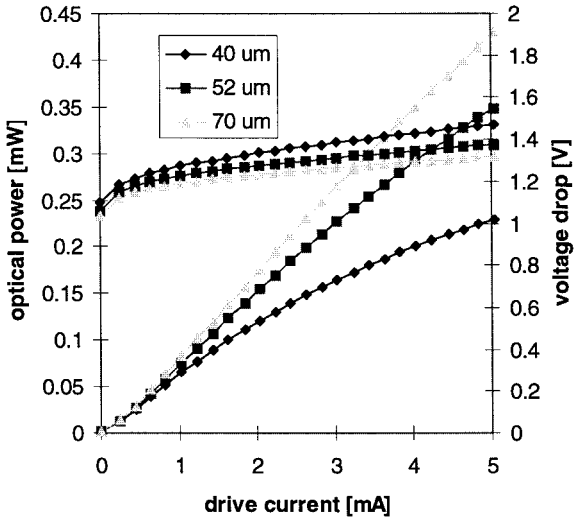

Fig. 10. Measured (P, I, V) characteristics of 3 different diameter RCLED's.

not degraded by the reflow process. Inspection of features on test chip/carrier structures confirmed the alignment in the X, Y chip plane to be within ± 3 μm. The chip-to-carrier separation, set by the volume of solder between the solder-wettable pads, was 15 μm (as designed) with a mean variation of 2 μm.

CMOS carrier styles included a version with a 4×8 array of solder-pads connected directly to test points on the carrier periphery, and a version with two blocks of (4×8) arrays of solder-pads connected to arrayed driver circuits. A 64-element RCLED array, interfaced to an 8×8 driver array was built up by placing two "standard" 4×8 arrays side-by-side on the CMOS chip, then reflowing the solder in a single operation. A completed two-chip assembly is shown in Fig. 9. Conventional epoxy die-attach and wire-bonding processes were applied to mount the optohybrid unit on an interconnect tile into a PGA package for electrooptic characterization.

VI. Characterization

A. Characterization of the RCLED's

The (P, I) and (V, I) characteristics for three RCLED's with different mesa diameters are shown in Fig. 10. The quantum efficiency at 3 mA is 13.4% for the 70-μm mesa RCLED, 11.8% for the 52-μm mesa RCLED and 8.6% for the 40-μm mesa RCLED. The efficiency decreases as function of decreasing RCLED diameter. This is explained by the higher current density, resulting in a broader intrinsic spontaneous emission spectrum (and thus decreased overlap with the cavity enhancement). This effect results in a saturation of the output power at higher current densities, where the thermal effects become important. The internal heating results in a shift of the cavity resonance, and a decreased overlap. The efficiency decreases at very low current densities, due to the current spreading effects in the mesa.

The differential resistance at 3 mA is 48 Ω for the 70-μm mesa RCLED, 35 Ω for the 52 μm mesa RCLED and 30 Ω for the 40-μm mesa RCLED. The voltage drop across the devices is small. The emission spectrum of the RCLED has a peak at

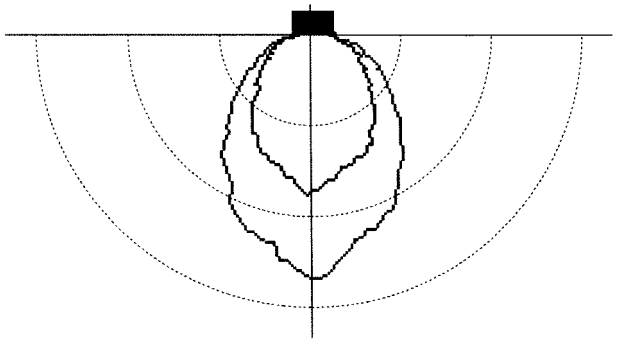

Fig. 11. Far-field pattern as function of current.

984 nm, and its width is 21 nm. The spectral width does not depend on the current level or RCLED diameter, indicating the filter effect of the microcavity on the intrinsic spectrum.

The far-field pattern of the 70-μm mesa RCLED is shown in Fig. 11. The lobe shows a small extra peak at the top, which is explained by the current spreading. A part of the current flows next to the mirror, but still within the mesa. The cavity resonance next to the mirror is at shorter wavelengths, due to the absence of the phase shift of the metal mirror. The resulting light emission is more perpendicular but not as efficient as the metal covered part of the device.

The coupling efficiency of RCLED's to POF was investigated experimentally. The absorption losses of the POF are strongly wavelength dependent in the 980-nm range. Therefore, the losses were determined experimentally for the given RCLED emission spectrum, using the cutback method. The measured absorption loss of the POF is about 12 dB/m, independent of the diameter of the fiber.

To measure the coupling from RCLED to POF, the RCLED's were flip-chip mounted onto a glass substrate and the POF was aligned to the RCLED using a XYZ-translation stage. Using this setup, we measured the coupling as a function of POF-diameter and drive current. A difficulty in the coupling experiments with the POF's is the repeatability of the fiber facet quality. A hot knife technique was used, followed by

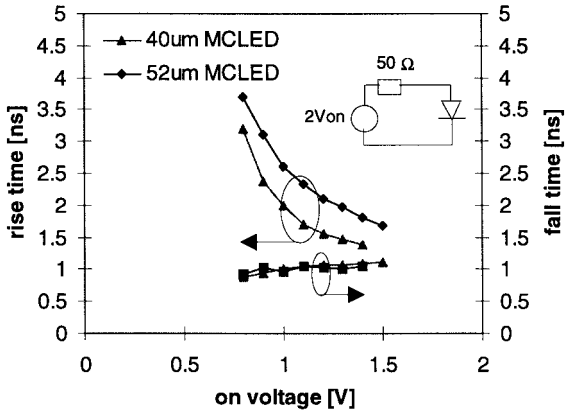

Fig. 12. Measured rise and fall time of two different diameter RCLED's.

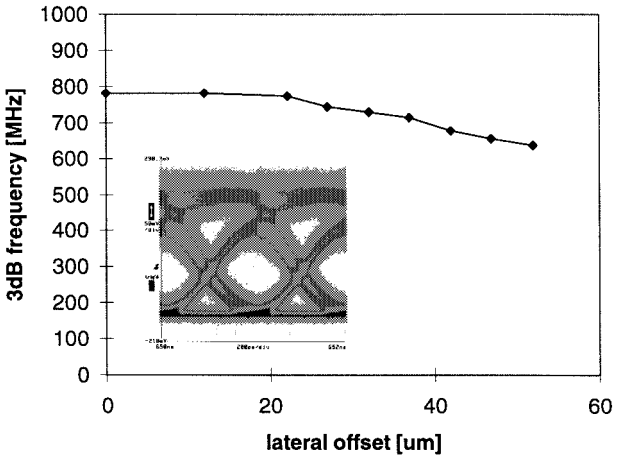

Fig. 13. Measured bandwidth of 50-μm RCLED coupled to 125-μm POF as function of lateral offset. Inset: eyediagram of 50-μm RCLED at 1 Gb/s.

a polishing step, to obtain smooth POF surfaces [35]. The measured overall quantum efficiency at 2-mA drive current into a 125-μm-diameter POF is 2.8%. This corresponds to a POF coupled power to current ratio of 35 μW/mA. A value of 3.7% was expected from the numerical integration of the measured far-field pattern. The difference can be explained by the reflectivity (fresnel losses at the POF–air interface are about 4%) and scattering at the nonperfect fiber facet.

The transient behavior of the flip-chip mounted RCLED's was evaluated using a high-speed voltage pulse generator. Fig. 12 shows the measured rise and fall times as function of the on-voltage for 2 different RCLED diameters. The on-voltage is defined in a 50-Ω environment, as shown in the equivalent circuit on the inset. The rise time decreases as function of the on-voltage, as the current density increases. The rise times of a current driven RCLED is calculated analytically assuming uniform current injection, no nonradiative recombination. The radiative lifetime is given by $t_{\rm rad} = 1/{\rm Bn}$, with n the carrier concentration in the active region, and B the bimolecular recombination coefficient. The rise time is given by

$$t_{\rm rise} \approx 1.49\sqrt{\frac{qV}{BI_{\rm on}}} \tag{2}$$

where q is the elementary charge, V is the volume of the active region, B is the bimolecular recombination coefficient, and $I_{\rm on}$ is the current (assuming 100% injection efficiency). This equals 5.5 ns for a 50-μm diameter RCLED driven at 3 mA and 2.2 ns for 20-μm RCLED's driven at the same current level. Voltage driven diodes show shorter rise times, as the current transient during switching is strongly peaked. The active layer is filled faster, and the rise time decreases. Rise times under 1.5 ns are measured (see Fig. 12). The fall time is determined by the carrier sweep-out effect: at the off-transient, the RCLED is connected to the ground by a small resistor (quasi a short-circuit) and accumulated carriers are swept out the active regions of the device [5].

Fig. 13 shows the measured bandwidth (defined as the maximal square wave frequency at which the measured peak to peak signal is the half of the dc-signal) as function of the lateral misalignment. This decreasing trend is explained by the current spreading effect in the mesa. The current density next to the metal mirror is smaller, resulting in smaller rise and fall times. For increasing misalignments, the POF captures relatively more light emitted next to the metal mirror (but still within the mesa), implying larger rise and fall times.

B. Characterization of Driver-RCLED Combination

A setup was built to measure the optical power and the time-response of the mounted RCLED chips. The CMOS chip was mounted onto an alumina carrier, and contacted using wire-bonds. The light was detected using a high-speed Hamamatsu APD-receiver combination. For the free-space measurements, the detector was placed as close as possible to the RCLED's. However, there was a rather large electrical crosstalk, due to interference with the probe needles carrying the high-speed signal. In a second approach, the light was coupled to a POF (diameter 125 μm) and guided to the detector. To measure the high-speed behavior, a 50-Ω resistor is placed in parallel between the ground and the signal pin to get an impedance-matched device. The signal ground and supply voltage ground shared the same pad, to reduce the electrical crosstalk (by reducing the HF current loop)

The emitted optical power of the mounted RCLED into a 125-μm-diameter POF under dc conditions was measured as a function of the modulation reference current and the CMOS supply voltage. The measured current to power in POF conversion efficiency is 18.8 μW/mA. This value is smaller than the previous measurement. This can be explained by small deviations on the layer thickness and material composition over the wafer, resulting in a shifted cavity resonance. The measured peak wavelength was 962 nm instead of the designed 980 nm. Simulations showed that this detuning results in a 50% decrease of the extraction efficiency, which corresponds to an ideal (e.g., without growth deviations) conversion efficiency of 36 μW/mA, which is in agreement with the earlier measurements. There is clearly no degradation of the RCLED performance due to the solder bump mounting. The influence of the ambient temperature on the efficiency is modeled by a characteristic temperature (e.g., $P = P_0 \exp(-T/T_0)$). The measured T_0 at 3-mA drive current is 124 K (device diameter is 70 μm). The thermal crosstalk was evaluated by measuring

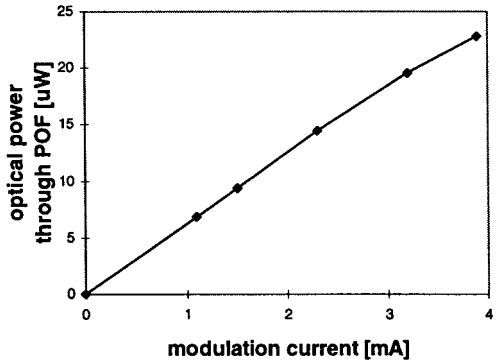

Fig. 14. Measured optical power at the output of a 40-cm-long POF (diameter = 125 μm), (RCLED diameter is 50 μm).

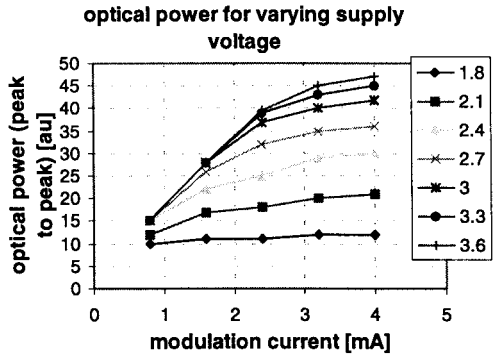

Fig. 15. Measured optical power as function of the modulation current and supply voltage (RCLED diameter is 50 μm).

the optical power of an RCLED as function of the distance to a neighboring (and dissipating) RCLED. The efficiency of the RCLED increased as function of this distance: the heating of the neighboring RCLED causes a temperature increase in the RCLED and thus a decreased efficiency. This effect is negligible at low current levels. A crosstalk coefficient ξ (defined as $P = P_0(1 - \xi I)$, with I the current through the neighboring RCLED) was measured: $\xi = 1.9$ 1/A for 250 μm RCLED distance. Even at 10 mA, the decrease in optical power due to the thermal crosstalk between two neighboring RCLED's is only 0.2%. Even if all nearest neighbor LED's are in the on state, the relative decrease in efficiency is still below 2%.

The sensitivity of the optical signal on the CMOS supply voltage is shown in Fig. 15. To reduce the dissipated power in the driver, the supply voltage can be reduced. However, the optical power saturates in function of the reference current if the voltage drop over the diode and the output transistor exceeds the supply voltage. This measurement shows that, if a current of 1.5 mA is sufficient, the supply voltage can drop to 2.7 V without decreasing the emitted optical power, but resulting in an 18% reduction in power consumption.

Fig. 16 shows the measured peak-to-peak optical power, with a square wave signal applied to the CMOS driver, as function of the frequency, for two different RCLED diameters (40- and 70-μm mesa, corresponding to 20- and 50-μm RCLED's). The bias current is 0 mA, the modulation current is 3 mA. The measured rise time is 7.4 and 3.2 ns. The deviation

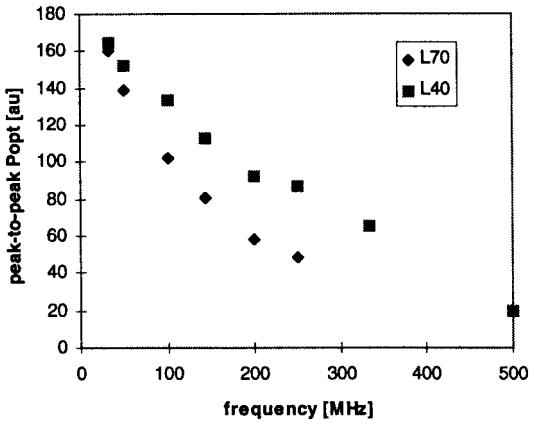

Fig. 16. Measured peak-to-peak optical power as function of the signal frequency, for two different RCLED diameters (L70 corresponds to 50-μm RCLED's, L40 corresponds to 20-μm RCLED's).

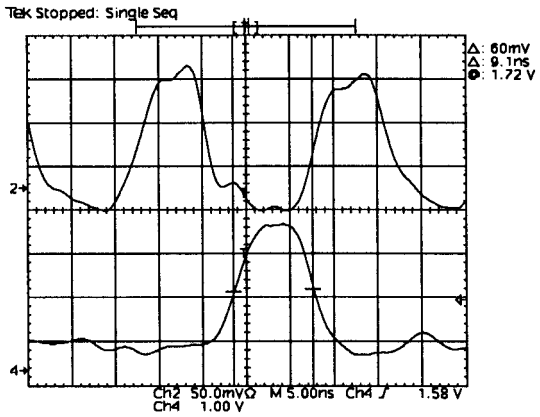

Fig. 17. Measured electrical input and optical output signal.

to the calculated values is explained by the current spreading near the RCLED mirror. This results in smaller current density at the border of the mesa.

The delay measurements of Fig. 17 resulted, after compensation for the 2.1-ns delay difference in the measurement cables, in a delay of 7 ns from electrical input pin of the chip to electrical output of the detector. According to simulations of the digital circuitry on the chip and the properties of the detector approximately half of this delay must be accounted to the combination of the driver and LED source. The shortest pulse still generating an observable output signal was between 2 and 3 ns in length.

Figs. 18 and 19 show two eye diagrams of the RCLED, driver and POF combination. The RCLED diameter is 50 μm (so these are the slowest components). The eye is still open at 155 Mb/s for a modulation current of 1 mA, and at 250 Mb/s for a modulation current of 3 mA. No bias current is applied in either case.

In the literature, several CMOS integrated receiver circuits are reported, with sensitivities of at least -20 dBm at 300 Mbit/s [36], [37]. The presented RCLED's couple over 50 μW in POF at 3-mA drive current, allowing a 7-dB loss in the optical path. This includes absorption losses and bending losses in the POF, and losses due to a bad overlap between the outcoupled light and the detector area. The efficiency of

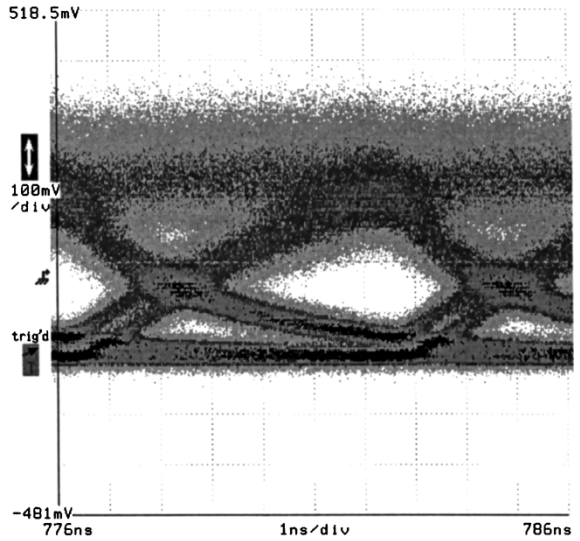

Fig. 18. Measured eye-diagram at 155 Mb/s, bias current is 0 mA, modulation current is 1 mA (RCLED diameter is 50 μm).

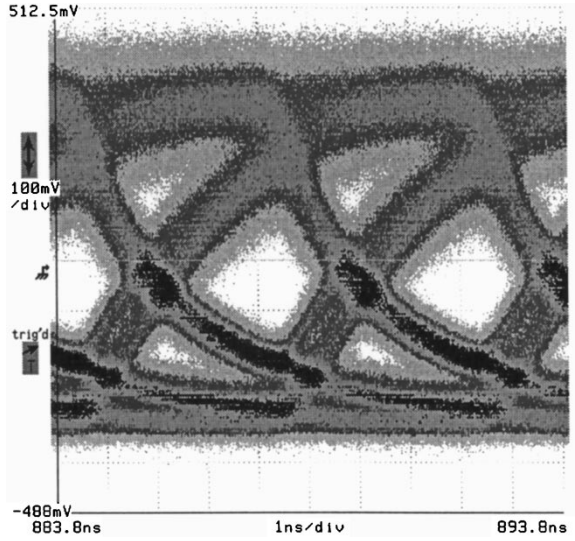

Fig. 19. Measured eye-diagram at 250 Mb/s, bias current is 0 mA, modulation current is 3 mA (RCLED diameter is 50 μm).

the RCLED's could be increased further by making use of AlOx current windows, to confine the current under the cavity mirror and avoiding current spreading.

VII. Conclusion

We have realized an 8×8 RCLED array flipchip mounted onto a CMOS circuit with an 8×8 array of drivers. The RCLED's were optimized for coupling to POF, and the calculated maximal extraction efficiency into the numerical aperture of a standard POF (NA $= 0.5$) was found to be 7.6%. In this design, a modestly reflecting outcoupling mirror (five pairs AlAs–GaAs DBR) was used, in order to enhance the whole intrinsic spectrum by the microcavity effect. The cavity resonance wavelength was found to be slightly larger than the peak intrinsic emission wavelength. The RCLED arrays were realized and characterized, and unmounted devices showed overall quantum efficiencies of 14% and voltage drop under 1.5 V at 3-mA drive current. CMOS integrated drivers were designed and realized in 0.6- and 0.8-μm CMOS technology, and showed high-speed operation up to 600 and 800 Mb/s. The arrays were mounted onto the CMOS drivers using an PbSn solder reflow technique and characterized. We measured 20-μW optical power out of a 40-cm-long POF, aligned to the RCLED array, at a modulation current of 3 mA. The measured eye-diagrams shows that 250-Mb/s operation of the 50-μm RCLED's at 3-mA drive current is achievable. Comparing this to reported integrated CMOS receivers, a power loss of over 7 dB in the optical path can be tolerated.

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Roel G. Baets (M'88–SM'96), for photograph and biography, see this issue, p. 144.

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He was a research engineer at the ATT Bell Laboratories in Murray Hill, NJ, for 12 years. There he developed fast photodetectors, projection displays with liquid crystals and avalanche photodiodes for the first demonstrations of fiber optic communication. At the ETH, he heads the Laboratory for Microelectronics and Opto-electronics with a III–V compound semiconductor technology laboratory for student training and optoelectronic and electronic device development. He is also involved in information and communication technology research for the European Union. His research concentrates on optoelectronics and electronic components, from physical fundamentals over device technology to their applications in communication and signal processing.

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Jon Hall received the Ph.D. degree in inorganic chemistry from Imperial College, University of London, London, U.K., in 1980.

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