SOI Lattice Filters Design Framework: from Functional Parameters to Layout

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In this paper we demonstrate a lattice filter based WDM framework on SOI platform. Finite Impulse Response filter synthesis routines are used to calculate the design specifications. The inputs are functional parameters: normalized cut-off frequency, free spectral range, filter order and windowing function. The obtained specifications are passed to the Caphe circuit simulator. Then we convert the design parameters to physical parameters in IPKISS for layout and mask design. The measured results prove the validity, but also the limitations of the framework. The latter, more pronounced in high order filters, are mainly attributed to errors in the weak coupling sections.

Introduction

SOI (Silicon on Insulator) photonics offers a way to reduce the footprint of passive photonic devices. Moreover the SOI processing is compatible with CMOS technology, potentially enabling mass production. Networking applications based on wavelength division multiplexing require wavelength filters for the routing and multiplexing operations: these can be based on ring resonators , AWG (Arrayed Waveguide Grating) , Echelle, MZI (Mach-Zehnder Interferometers) based filters, or a combination of them [1], [2]. We will discuss cascaded MZI filters, as shown in Figure 1. Cascaded MZIs are optical FIR (Finite Impulse Response) filters. A FIR filter is composed of n 2×2 power splitting devices and $n-1$ delay stages. Increasing the order of such device, better performance in terms of extinction ratio and roll-off can be achieved. On the other hands, increasing the order the contribution of every single stage nonidealities arise. These two requirements are the main element in the designing trade-off condition.

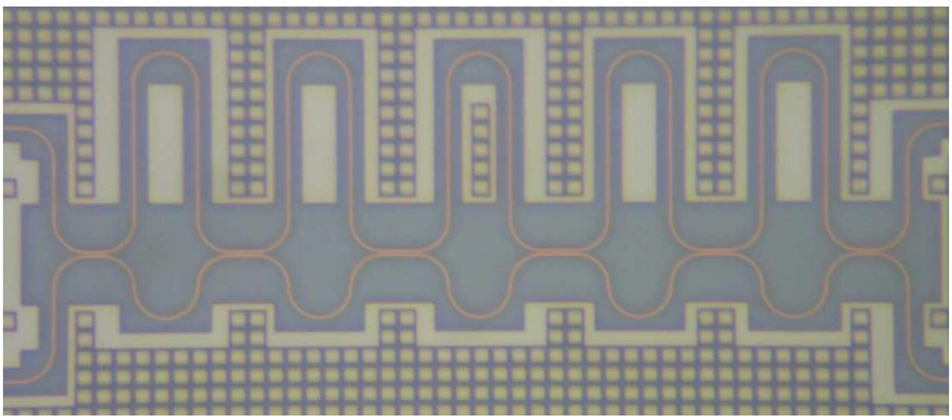


Figure 1: A Mach-Zehnder based lattice filter

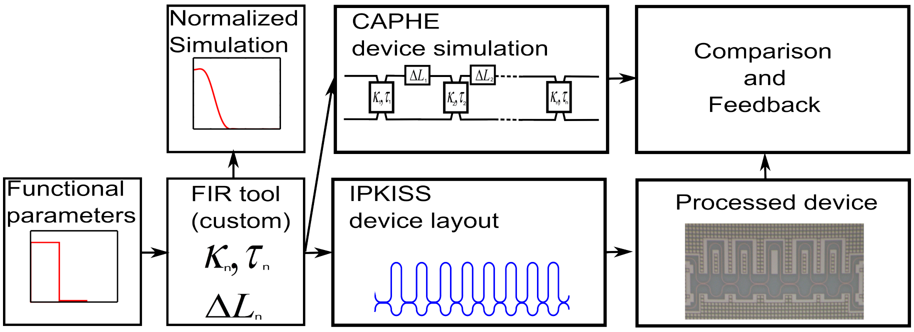


Figure 2: description of the framework

Theoretical Background

The multi-stage lattice filter can be modeled as a cascade of blocks. Neglecting any reflections back into the input ports, the initial 4×4 T-matrix can be reduced to a 2×2 transmission matrix for each elementary block. With these conditions, representative matrix are the (1) and (2) respectively for directional coupler section and delay lines section.

$$S^i_{cou} = \begin{bmatrix} \tau_i & -j\kappa_i \\ -j\kappa_i & \tau_i \end{bmatrix} \tag{1}$$

$$S^i_{del} = \begin{bmatrix} e^{-j\beta\Delta L} & 0 \\ 0 & 1 \end{bmatrix} \tag{2}$$

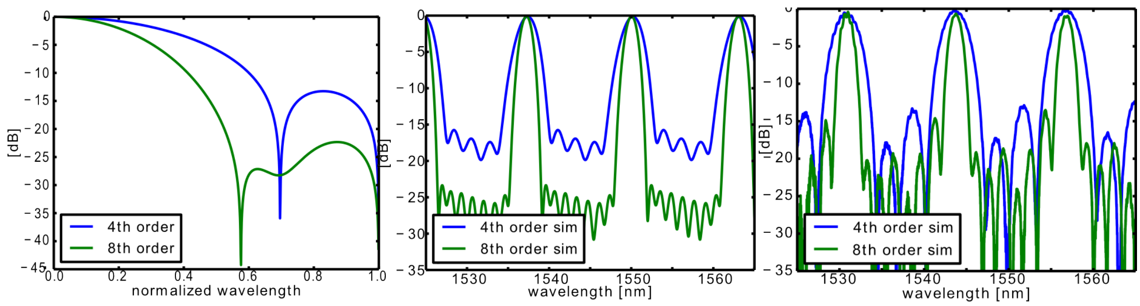
In the eq.(1) the relation in between the variables is $\tau = \sqrt{1-\kappa^2}$. In the eq.(2) the variable β is the propagation constant of the waveguides and ΔL is the physical length difference between the two arms. We assume the same type of waveguides in both arms, but the formulas can be extended for different waveguide cross sections. The final analysis formula of a n^{th} order lattice filters is represented in (3). It the product of the T-matrix of the cascaded building blocks. The (4) gives the relation to be used for the calculation of the delay length between the arms.

$$S = S_c^{n+1} \prod_{i=1}^{n} S^i_{del} S^i_{cou} \tag{3}$$

$$\Delta L = \frac{c}{g_i FSR} \tag{4}$$

Framework description

The developed framework is described in the Figure 2. The input consists of the spectral filter requirements such as central wavelength, FSR . After these basic parameters, we can set additional design specifications such as the main filter windowing function and its associated variables. We typically use a Chebyshev window, where we specify the normalized cut-off frequency and the stop band attenuation. The design values are fed in to the FIR filter design routines which calculate the required coupling ratios. The delay in the arms is calculated using analytical formulas. The FIR design tool then converts the functional specifics to design parameters. Once all the design specifics are obtained,



(a) Normalized simulation (b) CAPHE simulation (c) Measurements

Figure 3: Simulation and measurements

they are passed in parallel to the CAPHE photonic circuit simulations and IPKISS layout designer. CAPHE simulates the entire PIC (Photonic Integrated Circuit) as an optical circuit, linking the elementary building blocks together: waveguides combined together to obtain 2×2 delay sections and directional couplers. The IPKISS mask design is then used to convert functional specifications into layout specifications with physical dimensions for the directional couplers and the waveguides.

Filter Synthesis

The unknown quantities in eq.(1) and eq.(2) are τ and ΔL. The value κ in the directional couplers is related to τ. The ΔL path difference of the arms determines the FSR of the transfer function associated to the filter. The delay time between the arms is obtained form both physical path difference and group index of the waveguide used. The other parameter required is the power coupling ratios in each of the coupling sections. To calculate those, we use the FIR (Finite Impulse Response) filter synthesis tools available in scientific python. The inputs for such tools are the type of filtering window and its parameters: for the purpose of this work we mainly used Chebyshev windowing, which require at least three parameters: the order of the filter (the number of stages), the cut-off frequency and the attenuation in the stop band. Figure 3a shows the response of lattice filter in the case of 0.250 cut-off normalized frequency.

Filter Simulation

The PIC software used is CAPHE [3]. Basic n-port blocks are connected together to obtain complex photonic circuits. Each elementary block is represented by its T-matrix. Directional couplers are photonic integrated devices with a rather strong wavelength dependence. We define n directional couplers with power splitting ratios obtained by the FIR design tool. The directional couplers are chained together with the $n-1$ delay sections. The relative delay of the arms is defined according to the (4). The output of such a simulation is a replica of the Figure 3a, but shifted to the center wavelength, and with wavelength periodicity equal to the FSR. Figure 3b show the simulation of the devices chosen for testing of the framework. The FSR, at $1600GHz$, is the same for both. The simulated devices act as single channel drop filters. The same design approach can be extended to a full WDM mux/demux. By choosing the order of the filter, the response can be tailored: the plot Figure 3b correspond to a 4^{th} order and an 8^{th} design, respectively.

		IL [dB]	ER [dB]	1 dB/10dB BW	area[μm^2]
4^{th} order	4X400GHz	-0.66	15.7	0.33	4280
	8X200GHz	-1.08	14.6	0.33	4200
8^{th} order	4X400GHz	-0.40	17.9	0.33	7744
	8X200GHz	-0.55	12.1	0.32	7808
12^{th} order	4X400GHz	-0.77	5.8	0.57	11172
	8X200GHz	-2.72	8.9	0.38	11336

Table 1: Measurement results

Layout and experimental results

The parameters obtained by the FIR tool are handed over to IPKISS [4] for the layout generation. This step includes the translation of the functional parameters to physical parameters. This conversion requires good knowledge of the elementary building block characteristics. First of all the n_{eff} and the n_g of the guiding structures has to be known. The n_{eff} is used for the designing of the proper ΔL associated to the required delay. The coupling coefficients of the directional couplers can be split up in two parts: the first is the κ associated to the straight section, and proportional to the length of the coupler, and the κ_0 associated to the bent section. In general, the former dominates the latter, but when weak coupling is required (i.e. rings, lattice filters) the coupling associated to the bent section assumes a predominant rule. The coupling strengths can be extracted from physical simulations or measurements. Figure 3c shows the measurements relative to the simulated devices. The table 1 tabulates the measurement results for the different fabricated filters, in particular: IL (Insertion Loss), ER (Extinction Ratio), 1dB/10dB bandwidth ration and dimensions.

Conclusion

We present a design procedure for MZI lattice filters starting from filter synthesis techniques down to the physical circuit layout, and we show the correspondence between measured and simulated devices.

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