22.5 A 4×20Gb/s WDM Ring-Based Hybrid CMOS Silicon Photonics Transceiver

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Silicon photonics (SiPh) has been identified as a prime technology targeting cost-effective short-range optical links [1]. Wavelength-division multiplexing (WDM) is an attractive approach for enabling high aggregate transceiver bandwidth without increasing the number of optical fibers used in the link. Ring-based optical modulators and wavelength-selective filters are attractive devices for scalable WDM SiPh transceivers owing to their compact footprint and moderate power required for thermal tuning. In this paper, we report on a thermally controlled ring-based flip-chip integrated CMOS-SiPh transceiver with 4 channels operating at 20Gb/s.

A schematic of the 4×20Gb/s WDM CMOS-SiPh prototype and the characterization setup is depicted in Fig. 22.5.1(a). On the transmitter (TX) side of the SiPh chip, a cascaded array of 4 depletion-type silicon ring modulators is implemented with a 300GHz resonance wavelength spacing. Each ring modulator can be thermally tuned by a dedicated heating element and is connected through flip-chip bonding to a differential driver on the CMOS chip. On the receiver (RX) side, a collectively thermally tunable 5-channel double-ring based WDM filter with matching wavelength channel spacing is implemented to demultiplex the WDM optical beams into separate waveguides [2]. The optical signal is detected by a germanium waveguide photodiode and is further amplified and converted into a voltage by a TIA located on the CMOS chip. At the edge of SiPh chip, an array of 12 (actually 3 in this experiment) single TE polarization grating couplers, with 250μm pitch, is used to couple the optical signals from single-mode optical fibers onto the photonic chip. An array of 12 single-mode fibers are permanently attached at the edge of Si photonic chip using a planar fiber-packaging method [3]. Figure 22.5.2 summarizes the performance of the SiPh devices.

Figure 22.5.3(a) presents the schematic of the asymmetric differential CMOS driver circuit providing $1.95V_{pp}$ voltage swing (with anode stage enabled) across the ring modulator. This higher-than-V_{DD} voltage swing extends the optical modulation amplitude (OMA). The cathode stage, consisting of a chain of 12 inverters, features full V_{DD} voltage swing and provides the reversed-bias voltage to the ring modulator, while the tunable anode stage extends the voltage swing in forward bias. Transistor MN2 in the anode stage closes the charging path from MP1 providing a controllable fraction of the supply voltage at its output in order to stay below a built-in voltage to prevent carrier injection into the diode, which would slow down electro-optic modulation. The swing at the anode is controlled through transistors MP2, MP4 and MP5. Each operating driver with anode stage enabled at 20Gb/s consumes 26mW power from the 1.3V supply voltage. On the receiver side, transimpedance amplifiers based on a chain of seven inverter-based TIA and g_m stages [4] are used. The receiver circuit, shown in Fig. 22.5.3(b), is powered from 1.1V, which allows it to achieve 10Gb/s modulation speed. From a 1.3V supply voltage both the gain and 3dB bandwidth are improved enabling 20Gb/s operation with energy efficiency of 0.58pJ/b.

To compare single and multi-wavelength transmission, first we characterized each channel separately and subsequently in WDM configuration. The transmission spectra through all 4 rings characterized with and without applying a heater voltage to each ring modulator are presented in Fig. 22.5.1(b). The optical loss on the TX side is measured to be -19dB, which is higher than expected (-11.5dB) due to a yield issue. Although the experiment is originally designed for 4 channels, due to external setup limitations we test 2×2-channels running simultaneously both on the TX and RX side. The optical eye diagrams are recorded for each channel separately and subsequently with two drivers operating simultaneously (Fig. 22.5.3) to assess victim-aggressor crosstalk. The optical power to the chip is provided from a 2-channel laser source with 300GHz-spaced operating wavelengths and optically multiplexed by 50% optical splitter. Each TX driver is fed with independent PRBS-7 data streams from an external PPG using a 50Ω-terminated GSGSG probe. This allows us to enable simultaneously two drivers and to demonstrate 2×20Gb/s optical transmission. To maximize OMA, the modulators are tuned individually with the heating ring element to shift their resonance wavelengths to match the laser grid. We also use an erbium-doped fiber amplifier (EDFA) with output power set to 8dBm and subsequent optical power splitter (90%/10%) at the TX output to simultaneously provide the modulated optical signal back to the receiver on the photonic chip and to record the optical eye diagrams on a scope. In the WDM case, we use a narrow (~2nm) optical filter before the scope to select the wavelength channel of interest. The eye diagrams measured on the drivers with on-chip multiplexer (Fig. 22.5.1(a): drv2 and drv3), which selects an internal or external data source, exhibited ~8ps higher jitter in both single-wavelength and WDM tests. When the two neighboring drivers are running at the same time (drv1 and drv2) or (drv3 and drv4) the horizontal eye opening decreases by an additional ~10ps jitter coming from electrical crosstalk and increased load of TX power line. Thermal crosstalk is also observed and requires a minor adjustment of both ring modulator heater voltages to optimize OMA on both operating channels. The worst measured extinction ratio (ER) is >7dB for the WDM test and >9dB for single wavelengths.

The electrical eye diagrams at the receiver measured for each wavelength separately and also with two WDM channels operating simultaneously are shown in Fig. 22.5.5. The wavelength channels are demultiplexed to separate waveguides terminated with Ge photodiodes by the thermally tuned WDM ring-based optical filters integrated on the SiPh die. The optical power of -2dBm after the EDFA and the polarization controller is sufficient to generate up to 140μA photocurrent per channel. The RX sensitivity is estimated to be -7.2dBm of average optical power at the photodetector for BER = 10^{-12}. All the electrical eye diagrams are measured with the TIA operating at 1.3V and with the current bias set to 75μA to subtract the average photocurrent to provide the appropriate input bias to the TIA. We measure the eye diagrams of both receiver outputs subsequently using a 40GHz GSG probe. The timing jitter generated by the electrical mux in front of two TX drivers is also observed in the received eye diagrams. The BER on one of the RX outputs for single and two-wavelength transmission is measured and plotted in function of average optical power at the detector (Fig. 22.5.5). Due to increased jitter on the TX in case of WDM transmission (additional ~10ps) and worse eye quality, we observe on average about 1.5dB optical power penalty to maintain the same BER compared to the single-wavelength case. The electrical energy efficiency (excluding laser power) of the optical link at 2×20Gb/s is measured to be 1.9pJ/b/ch in addition to 7.1mW/nm/ch of the heater power for tuning ring modulators and WDM filter.

Figure 22.5.6 presents the transceiver performance summary and a comparison table. Figure 22.5.7 presents a picture of the CMOS chip fabricated in a 40nm low-power technology and the Si-photonic chip fabricated in imec 200mm pilot line using a subset of 0.13μm CMOS processing modules [2], and the flip-chip integrated transceiver on a PCB with attached fiber array.

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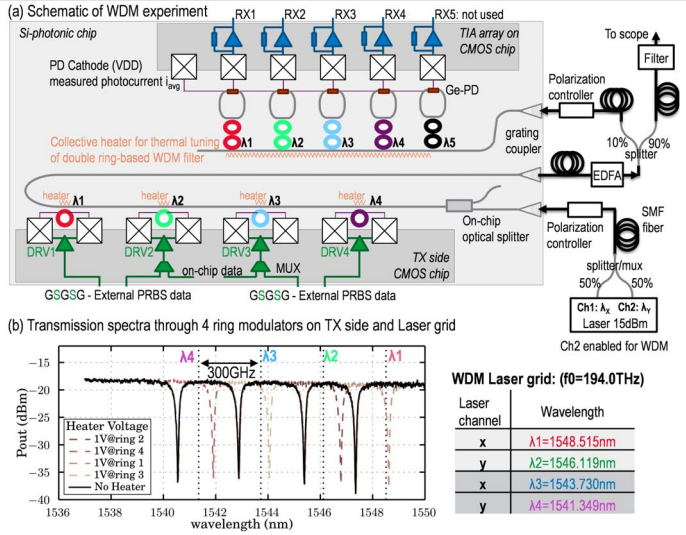

Figure 22.5.1: (a) Schematic of 20Gb/s WDM optical transceiver. (b) Transmission spectra of TX and laser grid settings.

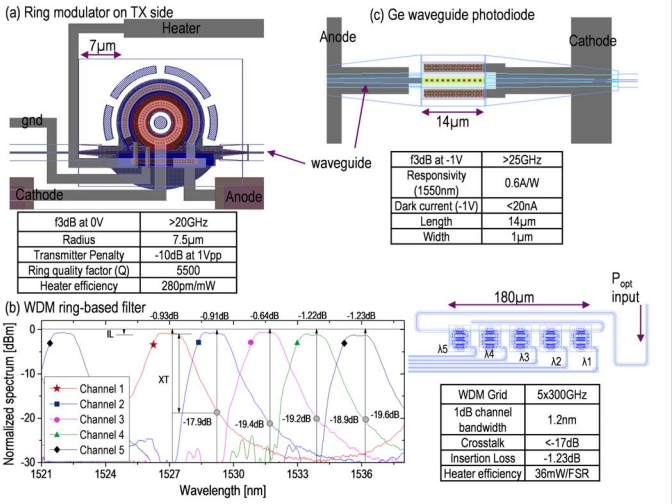

Figure 22.5.2: Key SiPh devices: (a) ring modulator with integrated heater (b) ring-based WDM filter with integrated collective thermal tuning (c) Ge waveguide photodiode.

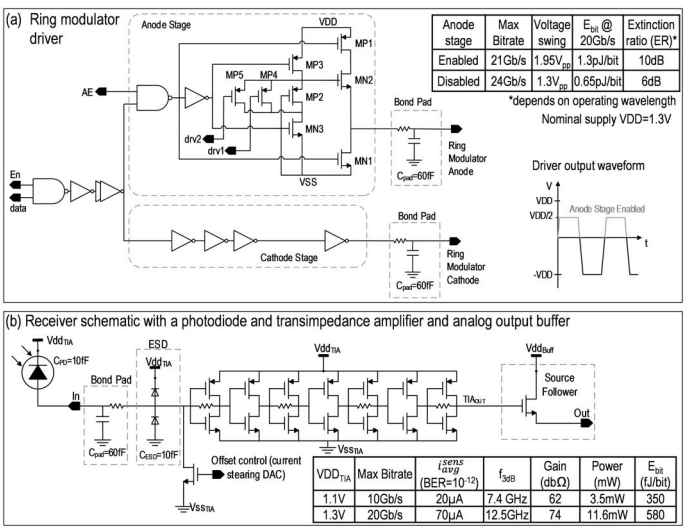

Figure 22.5.3: Schematics and performance tables of the ring modulator driver and TIA for 20Gb/s.

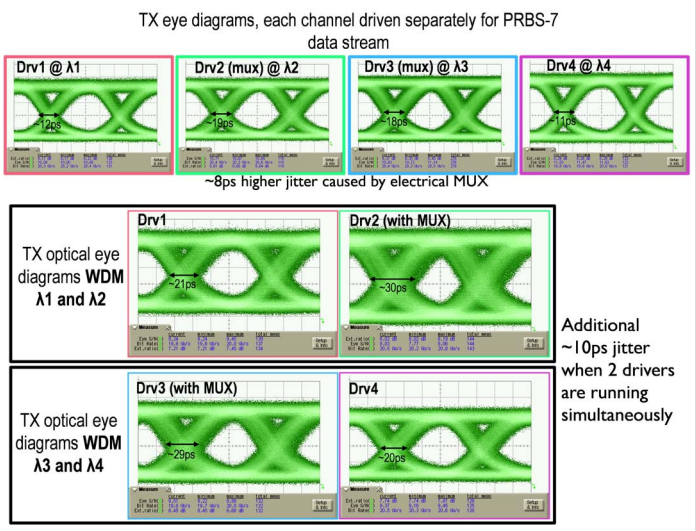

Figure 22.5.4: Measured 20Gb/s TX eye diagrams for each wavelength separately and in 2-WDM configuration.

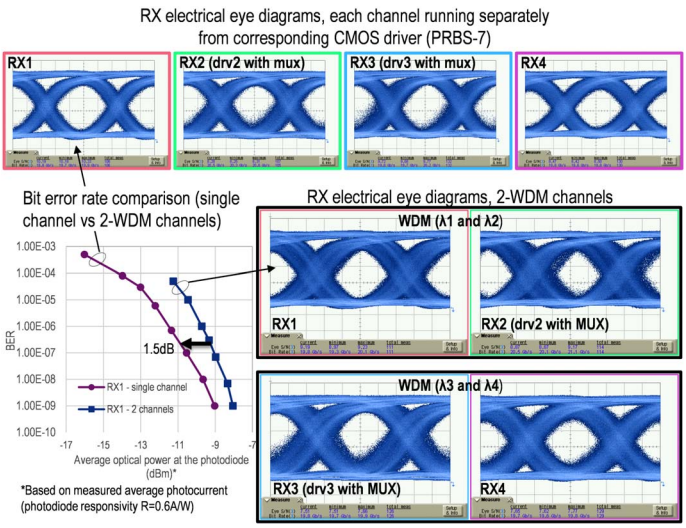

Figure 22.5.5: Measured 20Gb/s RX eye diagrams and BER (single wavelength and 2-WDM operation).

	This work	[5]	[6]	[7]
Integration Method	Hybrid	Hybrid	Hybrid	Monolithic
Technology (CMOS)	40nm LP CMOS	65nm CMOS	40nm CMOS	130nm CMOS SOI
Technology (Photonics)	130nm SOI	130nm SOI	130nm SOI	
Wavelength	1540-1550nm	1310nm	1550nm	1560nm
Supply Voltage	1.3V	1V,2V,2.5V	1V,1.3V,2V	1.2V/-1.2V
Data Rate	20Gb/s	5Gb/s	10Gb/s	25Gb/s
Tuning Method	Thermal	Voltage Bias	Thermal	N/A
TX				
Ring radius	7.5µm	2.5µm	12µm	7.5µm
Ring Mode	Depletion	Carrier-injection	Depletion	Depletion
Ring Q factor	~5500	~8000	~15000	~13000
Driver power	26.12mW/ch	4mW	1.35mW	207.6mW
ER	>7dB	12.7dB	7dB	6.9dB
#WDM channels	4	N/A	8	N/A
Heater power	6.2mW/nm/ch	N/A	1.25mW	N/A
Total TX energy at max bitrate	1.6pJ/bit/ch	0.8pJ/bit	0.26pJ/bit	8.3pJ/bit
RX				
Total Input capacitance	~80fF	>200fF	40-60fF	20fF
TIA power	11.6mW/ch	2.2mW	3.95mW	48mW
#WDM channels	5	N/A	N/A	N/A
WDM filter collective tuning	0.92mW/nm	N/A	N/A	N/A
Rx sensitivity	-7.2dBm@20Gb/s	-9dBm@8Gb/s	-15dBm@10Gb/s	-6dBm@25Gb/s
Total RX energy at maximum bitrate	0.73pJ/bit/ch	0.44pJ/bit	0.40pJ/bit	1.92pJ/bit

Figure 22.5.6: 20Gb/s CMOS-SiPh transceiver performance summary and comparison table.

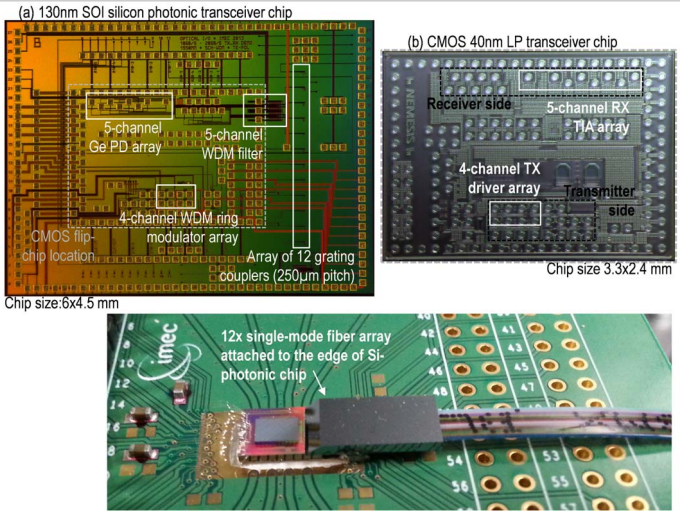

Figure 22.5.7: Si-photonics and CMOS chip pictures. Flip-chip integrated optical transceiver demonstrator with attached fiber array, glued and wire-bonded to a PCB.

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