4x25Gbit/s Silicon Photonics Tunable Receiver using Transfer Printed III-V Photodiodes

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Abstract—We demonstrate a 4-channel silicon photonics thermally tunable micro-ring receiver by transfer printing an array of commercial III-V C-band photodiodes. 25Gbit/s open eye diagrams were obtained for each receiver channel.

Keywords—silicon photonics, receiver, transfer printing

I. INTRODUCTION

Silicon photonics is an interesting platform for realizing advanced optical transceivers. It enables a CMOScompatible fabrication process, which allows high-yield, low-cost and volume fabricated devices. The high index contrast silicon-on-insulator (SOI) waveguide platform enables compact and efficient optical functions. Over the years a number of passive optical components have been developed on this platform to realize efficient tunable filters for wavelength-division multiplexing (WDM) together with high speed active devices (e.g. Ge photodiodes) and their monolithic co-integration. However, the complete process involves over 30 mask level processing steps in a fab, which results in a fairly long turn-around time. Moreover, monolithic III-V device integration in a silicon photonics platform is still challenging. Using a transfer printing

approach [1] one can effectively tackle these issues. In transfer printing III-V semiconductor devices are densely patterned on a III-V source wafer and released from its source wafer, allowing for a structured elastomeric PDMS stamp to selectively pick up the devices and print them on the SOI target wafer with high alignment accuracy $(\pm 1 \text{ um},$ 3σ) realizing potentially sparse integration in a massively parallel way. This allows to restrict the silicon photonics processing to passive silicon waveguide circuitry and adding the active functionality through transfer printing. In this paper we present the transfer printing of commercial surface-illuminated III-V photodetectors on a passive silicon photonic integrated circuit to realize a 4x25Gbit/s receiver using a thermally tunable micro-ring demultiplexer. We discuss the receiver design, its processing as well as measurement results.

II. RECEIVER DESIGN

The single polarization 4-channel receiver circuit is depicted in Fig. 1. Each channel consists of double ring filter which enables a flat-top filter response. The design and properties are more thoroughly described in [2]. Each micro-



Fig. 1. Schematic of the single polarization 4 channel tunable ring receiver, zooming in on the double ring filter used, the landing site for the photodetectors and a released commercial photodetector on a III-V source wafer.

ring is selected to have a coupling length of 9 µm, and a radius of 5 µm. The gaps are chosen to be 205 nm between the waveguide and the ring, and 340 nm between the rings. The ring resonators have a free spectral range of 11 nm. In this experiment, a commercial C-band surface illuminated photodiode design was adapted to enable transfer printing (i.e. the inclusion of an InAlAs release layer below the p-i-n layer stack). Photodiodes with 10 µm aperture were realized on a 75 x 75 µm coupon, which were released from the III-V substrate by underetching the InAlAs release layer, while being anchored to the substrate using photoresist tethers. More about the transfer printing process of III-V on SOI can be found in [3]. The photodiodes are to be printed on a silicon photonic grating coupler structure and therefore operate by bottom surface illumination. Tetris-brick alignment markers were added to the silicon photonic target structure to aid the high-alignment accuracy transferprinting.

III. PROCESSING

The passive silicon waveguide circuit was processed in imec's 200mm pilot line through a multi-project wafer run. The post-processing is performed on the standard passive SOI devices with 1.2 μ m top oxide layer. Micro-ring heaters were defined by depositing ~350 μ m long, 2 μ m wide and spiral-shaped Ti /Au wires (see inset in Fig. 2).



Fig. 2. A microscopic image of the one receiver channel after post-processing.

In a second step the above described photodiodes were transfer printed onto the grating coupler of each of the 4 channels, using a DVS-BCB adhesive bonding layer. After the printing the photoresist anchoring layer is removed by a ~35 minutes oxygen plasma. Then a ~4 μ m thick DVS-BCB layer is spin-coated and fully cured at 280°C to encapsulate the devices. Next, the DVS-BCB is etched back to access the photodiode electrodes and ~1 μ m thick Au tracks are deposited to form GSG contact pads. Last, the DVS-BCB was fully etched at the contact pads of the heaters to access the metal pads for DC probing. Fig. 2 shows the top-view of the receiver channel 1 after finishing the post-processing.

IV. MEASUREMENT RESULTS

Static I-V characteristics of the transfer printed device were measured. The devices have a dark current of about 20 nA at -2 V, with a series resistance of about 4 Ω . The waveguide-referred responsivity of the detectors is >0.5 A/W (at -2V bias) over the C-band. The ring resonator filters show a flat pass-band with a 1dB bandwidth of 0.74 nm.

Large-signal measurements were performed for every receiver channel. An arbitrary waveform generator (AWG) is used to generate a non-return-to-zero (NRZ) pseudo-randombit-sequence (PRBS) with a pattern length of 2^9 -1 at 25Gbit/s. A LiNbO₃ modulator was used in the experiments. The photodiode was biased at -1.5 V and the radio frequency output was connected to an oscilloscope through a bias-T. By applying a separate DC bias to the heaters, the resonance wavelength of every channel was tuned to obtain a 2.5nm channel spacing and eye diagrams at all four channels were measured. Fig. 3 shows open eye-diagrams at 25 Gbit/s for every channel.



Fig. 3. Eye diagrams of each channel at 25 $\overline{\text{Gbit/s}}$ by tuning the resonance of the micro-ring. The applied electrical power on the rings: a) 0 mW; b) 30 mW; c) 56 mW; d) 83.6 mW.

CONCLUSIONS

In this paper we demonstrated a C-band 4x25Gbit/s micro-ring resonator receiver with flat-top transmission characteristics by transfer printing commercial III-V p-i-n photodetectors. Using a heater, the resonance wavelength of each filter was tuned to achieve a channel spacing of $\Delta \lambda = 2.5$ nm. Open eye diagrams at 25 Gbit/s were obtained for each channel of the receiver. This demonstrates cost-effective and time-effective realization of III-V/Si photonic integrated circuits. While demonstrated on die-level, the technique is scalable to wafer level.

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