Integration of etched facet, electrically pumped, C-band Fabry-Pérot lasers on a silicon photonic integrated circuit by transfer printing

JOAN JUVERT,[1,2,*] TOMMASO CASSESE,[3] SARAH UVIN,[1,2] ANDREAS DE GROOTE,[1,2] BRAD SNYDER,[4] LIEVE BOGAERTS,[4] GERALDINE JAMIESON,[4] JORIS VAN CAMPENHOUT,[4] GÜNTHER ROELKENS,[1,2] AND DRIES VAN THOURHOUT[1,2]

[1] *Photonics Research Group, INTEC-department, Ghent University-IMEC, Technologiepark-Zwijnaarde 15, 9052 Ghent, Belgium*
[2] *Center for Nano- and Biophotonics (NB-Photonics), Ghent University, Technologiepark-Zwijnaarde 15, 9052 Ghent, Belgium*
[3] *Scuola Superiore Sant'Anna, Pisa, Italy*
[4] *IMEC, Kapeldreef 75, 3001 Heverlee, Belgium*
[*] *joan.juvert@ugent.be*

Abstract: We report on the heterogeneous integration of electrically pumped InP Fabry-Pérot lasers on a SOI photonic integrated circuit by transfer printing. Transfer printing is a promising micromanipulation technique that allows the heterogeneous integration of optical and electronic components realized on their native substrate onto a target substrate with efficient use of the source material, in a way that can be scaled to parallel manipulation and that allows mixing components from different sources onto the same target. We pre-process transfer printable etched facet Fabry-Pérot lasers on their native InP substrate, transfer print them into a trench defined in an SOI photonic chip and post-process the printed lasers on the target substrate. The laser facet is successfully butt-coupled to the photonic circuit using a silicon inverse taper based spot size converter. Milliwatt optical output power coupled to the Si waveguide circuit at 100 mA is demonstrated.

References and links

1. G. Roelkens, L. Liu, D. Liang, R. Jones, A. W. Fang, B. Koch, and J. E. Bowers, "III-V/silicon photonics for on-chip and intra-chip optical interconnects," Laser Photonics Rev. **4**, 751–779 (2010).
2. Z. Wang, A. Abbasi, U. Dave, A. De Groote, S. Kumari, B. Kunert, C. Merckling, M. Pantouvaki, Y. Shi, B. Tian, K. Van Gasse, J. Verbist, R. Wang, W. Xie, J. Zhang, Y. Zhu, J. Bauwelinck, X. Yin, Z. Hens, J. Van Campenhout, B. Kuyken, R. Baets, G. Morthier, D. Van Thourhout, and G. Roelkens, "Novel Light Source Integration Approaches for Silicon Photonics," Laser Photonics Rev. **11**, 1–21 (2017).
3. T. Komljenovic, S. Srinivasan, E. Norberg, M. Davenport, G. Fish, and J. E. Bowers, "Widely Tunable Narrow-Linewidth Monolithically Integrated External-Cavity Semiconductor Lasers," IEEE J. Sel. Top. Quantum Electron. **21**, 1501909 (2015).
4. Y. H. Jhang, K. Tanabe, S. Iwamoto, and Y. Arakawa, "InAs/GaAs quantum dot lasers on silicon-on-insulator substrates by metal-stripe wafer bonding," IEEE Photonics Technol. Lett. **27**, 875–878 (2015).
5. S. Keyvaninia, M. Muneeb, S. Stanković, P. J. Van Veldhoven, D. Van Thourhout, and G. Roelkens, "Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate," Opt. Mater. Express **3**, 35–46 (2013).
6. B. Snyder, B. Corbett, and P. Obrien, "Hybrid integration of the wavelength-tunable laser with a silicon photonic integrated circuit," J. Light. Technol. **31**, 3934–3942 (2013).
7. B. Tian, Z. Wang, M. Pantouvaki, P. Absil, J. Van Campenhout, C. Merckling, and D. Van Thourhout, "Room Temperature O-band DFB Laser Array Directly Grown on (001) Silicon," Nano Lett. **17**, 559–564 (2017).
8. L. Megalini, B. Bonef, B. C. Cabinian, H. Zhao, A. Taylor, J. S. Speck, J. E. Bowers, and J. Klamkin, "1550-nm InGaAsP multi-quantum-well structures selectively grown on v-groove-patterned SOI substrates," Appl. Phys. Lett.

111, 032105 (2017).
9. B. Corbett, R. Loi, W. Zhou, D. Liu, and Z. Ma, "Transfer print techniques for heterogeneous integration of photonic components," Prog. Quantum Electron. **52**, 1–17 (2017).
10. H. Yang, D. Zhao, S. Chuwongin, J. H. Seo, W. Yang, Y. Shuai, J. Berggren, M. Hammar, Z. Ma, and W. Zhou, "Transfer-printed stacked nanomembrane lasers on silicon," Nat. Photonics **6**, 615–620 (2012).
11. A. De Groote, P. Cardile, A. Z. Subramanian, A. M. Fecioru, C. A. Bower, D. Delbeke, R. Baets, and G. Roelkens, "Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters," Opt. Express **24**, 13754–13762 (2016).
12. J. Zhang, B. Haq, J. O'Callaghan, A. Gocalinska, E. Pelucchi, A. J. Trindade, B. Corbett, G. Morthier, and G. Roelkens, "Transfer-printing-based integration of a III-V-on-silicon distributed feedback laser," Opt. Express **26**, 8821 (2018).
13. M. a. Meitl, Z.-T. Zhu, V. Kumar, K. J. Lee, X. Feng, Y. Y. Huang, I. Adesida, R. G. Nuzzo, and J. a. Rogers, "Transfer printing by kinetic control of adhesion to an elastomeric stamp," Nat. Mater. **5**, 33–38 (2006).
14. N. Hatori, T. Shimizu, M. Okano, M. Ishizaka, T. Yamamoto, Y. Urino, M. Mori, T. Nakamura, and Y. Arakawa, "A hybrid integrated light source on a silicon platform using a trident spot-size converter," J. Light. Technol. **32**, 1329–1336 (2014).
15. C. Bower, D. Gomez, K. Lucht, B. Cox, and D. Kneeburg, "Transfer-printed integrated circuits for display back-planes," in *Proceedings of International Display Workshop* (2010), pp. 1203–1206.

1. Introduction

Due to the lack of a viable silicon light source for silicon photonics, several techniques for the heterogeneous integration of III-V lasers on SOI photonic chips are being explored [1, 2]. Special attention has been devoted to bonding techniques [3–6], III-V growth on silicon [7, 8] and transfer printing [9–12].

Transfer printing is essentially a pick and place technique where a specially pre-processed component, henceforth called *coupon*, is mechanically picked up from its native substrate by an elastomeric stamp, typically Polydimethylsiloxane (PDMS), and subsequently placed on the target substrate, where it can bond to an adhesive layer such as Benzocyclobutene (BCB) or directly to the substrate via Van der Waals forces. The speed at which the stamp moves away from the coupon will determine the strength of the adhesion between the stamp and the coupon [13]. For pick up from source wafers, the stamp moves quickly in order to achieve a higher bonding strength than that between the coupon and the native substrate, whereas for the printing operation to target wafers the stamp moves slowly in order to achieve a lower bonding strength than that between the coupon and the target substrate.

The transfer printing process is scalable through the use of multi-post stamps that allow the parallel transfer of arrays of components from source to target, which gives this technique an advantage over traditional flip-chip bonding. Furthermore, it is possible to carry out successive transfers from different source wafers onto the same target, which allows e.g., the integration of lasers operating at different wavelengths on the same target photonic chip, each laser being fabricated on its own native substrate, which is difficult to achieve with other bonding techniques [1]. Furthermore, the source material is used more efficiently than with other bonding techniques, where the dies to be bonded are on the mm scale. As with any other pick and place technique, placement accuracy is of paramount importance, which can be mitigated by a careful design of misalignment tolerant coupling structures.

In this paper we report on the integration of electrically pumped C-band, etched facet Fabry-Pérot lasers on a photonic chip by transfer printing. The laser coupons are pre-processed on their native InP substrate and transfer printed into a trench defined on an SOI photonic chip. The trench exposes the silicon substrate of the SOI chip. The lasers are therefore bonded directly on the silicon substrate without any adhesive layer, which should help with heat dissipation. By careful design of the epitaxial stack of the InP source wafer, the quantum wells in the transfer printed coupons are level with the silicon layer on the photonic chip and the laser output can be directly coupled into a spot size converter (SSC) on the photonic chip (see Fig. 1). With this approach the vertical alignment is ensured by the predefined height of the n-cladding of the III-V laser coupon.

In Section 2 we will discuss the three steps of the fabrication, that is the pre-processing of the
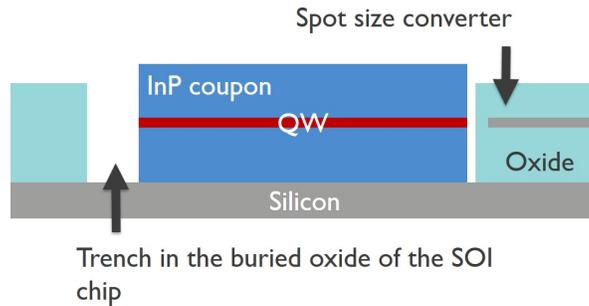
Fig. 1. Proposed integration strategy. The III-V coupons are transfer printed directly on the silicon substrate for better thermal dissipation. The laser output is directly coupled into a spot size converter on the SOI side.
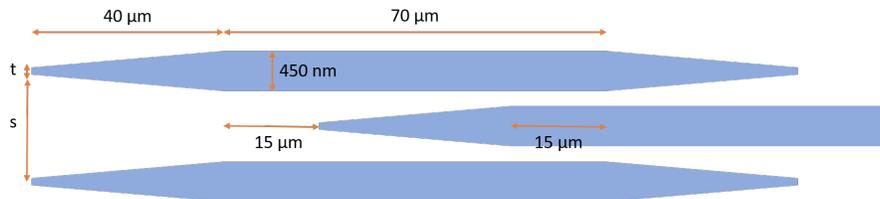
Fig. 2. Schematic representation of the trident SSC. t stands for the width of the tip and s for the distance between the centers of the two tips.

laser coupons on the native InP substrate, the transfer printing from the III-V substrate to the SOI photonic chip, and the post-processing on the SOI. In Section 3 we will discuss the results of the integration, in particular the alignment achieved during transfer printing, the performance of standalone lasers and the coupling to the photonic circuit. Finally, we will wrap up with a few concluding remarks in Section 4.

2. Fabrication

The general process flow consists of three steps: pre-processing of the laser coupons on the III-V substrate, transfer printing to the SOI chip, and post-processing on the SOI. The silicon circuits were fabricated on a 300 mm SOI wafer using 193 nm immersion lithography. The SOI wafer has a 220 nm device layer thickness and 2 µm buried oxide layer thickness. The chips consist of an array of SSC structures connected to a grating coupler by a waveguide, with a trench defined in front of the SSC. The etch of the oxide stops at the silicon substrate with minimal overetch into the substrate. Each trench has a different SSC, either a single inverted taper or a trident structure [14]. Different trenches use different parameters of the SSC, such as the tip size for the single inverted tapers and the tip size and space between tips for the tridents. The inverted tapers have a length of 100 µm and tips of 100, 125, 150 and 175 nm. The trident structures (see Fig. 2) are combinations of different tip widths t and tip separations s. The tip widths are $t = 100$, 125, 150 and 175 nm, whereas the distance between the centers of the tips is $s = 800$, 900 and 1000 nm. Figure 3 shows one side of two adjacent trenches each populated with a laser coupon. The trenches are 800 µm long and 100 µm wide.

During pre-processing on the III-V source wafer we define the main mesa of the transfer printable coupons, including the etched laser facets, as well as the III-V waveguide. We define the release layer pedestal, deposit n-contacts and encapsulate the coupons. Finally, a high selectivity
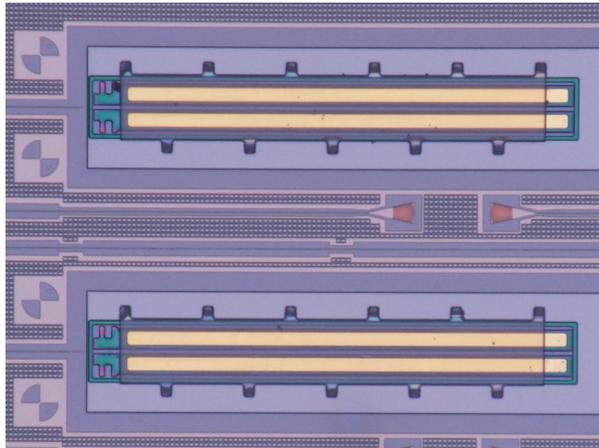
Fig. 3. Coupons transfer printed in the BOX trench. The bowtie features are used for pattern recognition during transfer printing. The coupling structures can be seen immediately to the left of the coupons.

etch using $FeCl_3$ is used to undercut the coupons by removal of the release layer, leaving them ready to be picked up.

The transfer printing involves picking up the coupons, aligning them on the target sites by using pattern recognition using marks on both the coupons and the target sites, and finally printing the coupons.

The post-processing involves deposition of a metal mirror on the back facet of the coupons to improve the feedback of the laser cavity, followed by the passivation of the whole chip with BCB. Vias are then opened on the BCB to access the pre-deposited n-contacts and to expose the top p layer on the III-V waveguide. Finally, the metal tracks to probe the laser are deposited.

2.1. Pre-processing

The process flow for the pre-processing of the lasers on the III-V substrate is schematically shown in Fig. 4.

The epitaxial stack (Fig. 5), grown at Smart Photonics, consists, from top to bottom, of: 100 nm sacrificial InP; 200 nm p-InGaAs; 1500 nm p-InP cladding with doping transition; 4 InGaAsP multi quantum well barrier/well pairs (12 nm/6 nm) sandwiched between two 50 nm InGaAsP separate confinement heterostructure layers (red in figure 4); 1950 nm n-InP cladding; 100 nm undoped InP used as an etch stop in the release process; a 500 nm InGaAs release layer (green in Fig. 4); 100 nm undoped InP etch stop layer and an InP substrate.

The first step is to partially etch the main mesa and the III-V waveguide (Fig. 4(a)). For that we use a dry etch process in an ICP-RIE with a nitride hard mask. The dry etch process in the ICP-RIE results in smooth and vertical sidewalls. We etch below the quantum wells until there is approximately 1 μm left of the n-cladding.

Next, the whole structure is protected with 250 nm of plasma enhanced chemical vapor deposition (PECVD) silicon nitride (Fig. 4(b)). The PECVD nitride will be deposited on the sidewalls as well, thus protecting the quantum wells from the following steps.

The nitride protection layer is removed outside the mesa and a second dry etch step in the ICP-RIE masked by the nitride etches the mesa further until almost reaching the InGaAs release layer. The thin InP remaining in the n-cladding is then removed by a wet etch in HCl (Fig. 4(c)). At this point the mesas are fully etched, and the III-V waveguide is defined by the two inner trenches inside the coupon.
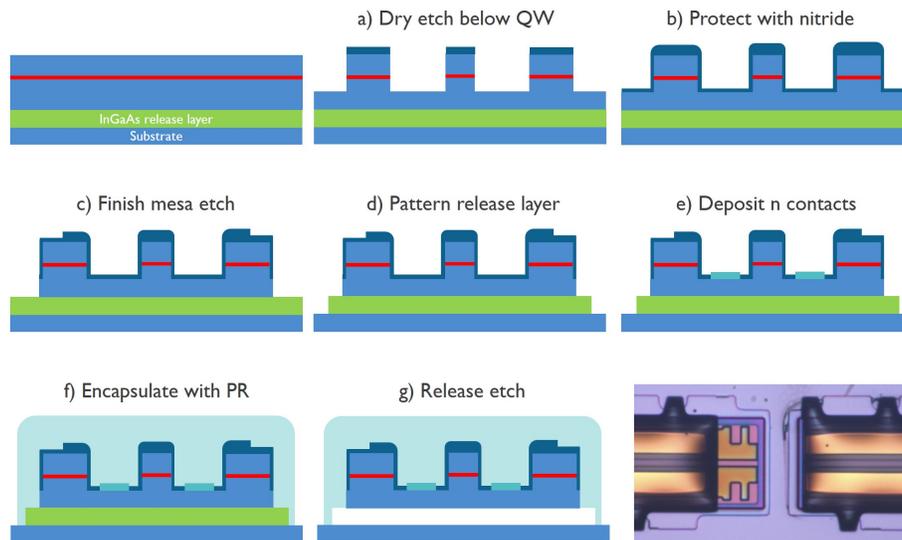
Fig. 4. Process flow for the pre-processing of the III-V coupons on the native substrate.

Fig. 5. Schematic of the epi layer stack.

The next step removes the release layer around the coupons by a wet etch with a Piranha solution. After this step, each coupon rests on its own release layer pedestal (Fig. 4(d)).

The nitride protection is then removed from the bottom of the inner trenches and the n-contacts are deposited (Fig. 4(e)).

Next, the photoresist encapsulation is defined using AZ9260 photoresist on the coupons, in such a way that photoresist tethers reach out beyond the release layer pedestal, thus anchoring the coupon to the substrate at certain places.

Finally, the coupons are undercut by a wet etch process in $FeCl_3$:H_2O that leaves them suspended by the photoresist encapsulation (Fig. 4(g)). The $FeCl_3$ solution provides an excellent selectivity between the InGaAs and the undoped InP [11], which is important to minimize any dishing effect on the bottom surface of the coupons.

The bottom right panel in Fig. 4 shows a top view of the front and back ends of two adjacent coupons on the III-V source wafer. The release layer pedestal can be seen clearly around the coupon, as well as the dark photoresist encapsulation with the tethers anchoring the structure to the substrate. The features on the front part of the inner trenches are used for the pattern recognition during transfer printing and are not covered by photoresist encapsulation. The coupons are 50 µm wide and 400 µm long. The III-V waveguide is 3 µm wide.
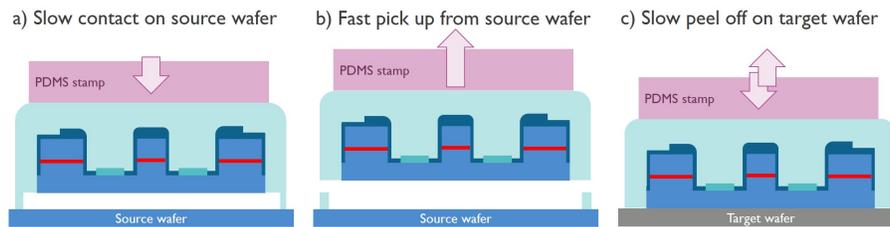
Fig. 6. Schematic illustration of the transfer printing process.

After the release etch, optical inspection of the sample indicates that all the coupons are ready to be picked up. Although we have not attempted the pick up of all 1800 coupons present on the chip, random pick ups across the whole area indicate that the process is reliable, with no collapsed, unreleased or otherwise damaged coupons.

2.2. Transfer printing

The transfer printing process is schematically illustrated in Fig. 6. A PDMS stamp with dimensions similar to those of the laser being transfer printed is slowly lowered until contact is made with the photoresist encapsulation (Fig. 6(a)). The stamp is then pulled up quickly to increase the adhesion between the PDMS and the photoresist. The photoresist tethers snap and the coupon is released from the source wafer (Fig. 6(b)). Finally, the coupon is slowly lowered until contact is made with the target substrate. Shear force is applied for a few seconds before slowly peeling off the stamp from the photoresist encapsulation (Fig. 6(c)), leaving the coupon bonded on the target substrate.

The coupons were printed one by one on the target chip. The alignment of the coupons in the landing sites is done automatically using pattern recognition. The features on the inner trenches of the coupons (see bottom-right panel in Fig. 4) and the bowtie features in front of the BOX trenches on the photonic chip (see left side of Fig. 3) are identified by pattern recognition software. These patterns are registered once, when a coupon is being held above the landing site right before a printing operation. This is done in this way in order to use reference images that are as close a possible to those the software will use to carry out the actual pattern recognition. Once done, the pattern recognition files can be reused in subsequent printing sessions. After the software identifies the patterns the position of the coupon is automatically adjusted so that the center to center distance between both patterns (coupon and target) is the desired value. In this case, the ideal position of the coupon corresponds to perfect alignment between the III-V and silicon waveguides, and laser facet in contact with the trench wall in order to minimize the distance between the edge of the III-V waveguide and the tip of the SSC. The nominal accuracy of the printing is $1.5\,\mu m\ 3\sigma$ [15].

Figure 3 shows two adjacent trenches on the photonic chip populated with one laser coupon in each. The front facet of the coupon is printed as close as possible to the wall of the trench. Immediately to the left of the coupon and separated by $3\,\mu m$ from the trench wall, we find the SSC. This distance ensures that the etch of the trench in the buried oxide will not damage the tip of the SSC, since the overlay control for the trench mask (after etch) is better than $2\,\mu m$.

The yield of the pick up operation is very high. All the coupons that we attempt to transfer print can be successfully picked up. As for the printing, 17 out of 20 trenches were successfully printed on the photonic chip, whereas 20 out of 20 landing sites were successfully printed on the dummy substrate. It is worth mentioning here that the lack of an adhesive layer makes the encapsulation design very important in order to ensure the best possible bonding, and its optimization is a work in progress.
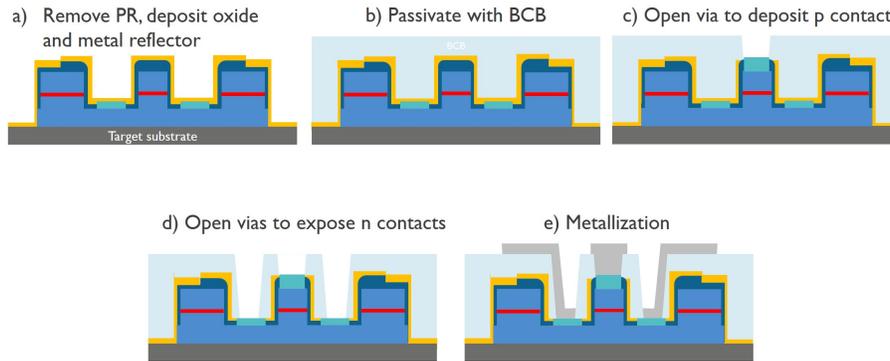
Fig. 7. Process flow for the post-processing of the coupons on the SOI target after transfer printing.
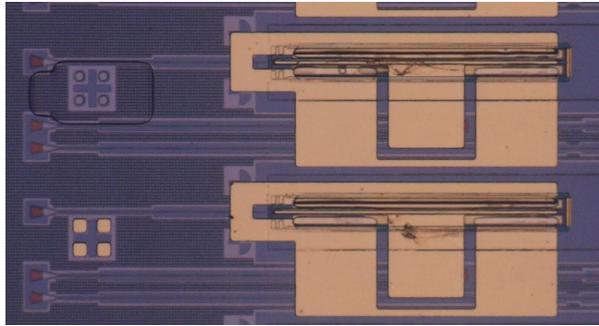
Fig. 8. Fully post-processed coupons on the photonic chip.

2.3. Post-processing

The post-processing on the target SOI wafer begins by removing the photoresist encapsulation with RIE (Fig. 7(a)). Next we deposit 200 nm of silicon dioxide with PECVD and deposit a gold mirror on the back facet (not shown in Fig. 7(a)). This is done by tilting the sample during sputtering of the gold to ensure good coverage of the back facet. The silicon oxide prevents short-circuiting the device during the gold mirror deposition.

The whole structure is then passivated with BCB (Fig. 7(b)) and a via is opened on the BCB and the nitride on top of the III-V waveguide in order to deposit the p-contact (Fig. 7(c)). Similarly, vias are opened on the trenches in order to expose the n-contacts (Fig. 7(d)).

The final step is the deposition of the metal tracks to probe the laser (Fig. 7(e)). Figure 8 shows a picture of the fabricated devices. All 17 coupons printed on the photonic chip were in working order and could be characterized.

3. Results

We printed and post-processed two batches of lasers, one on a dummy silicon substrate and another on functional SOI photonic chip. Figure 9 shows a SEM image of the front side of a laser coupon printed on a dummy substrate. The features on the substrate are used to measure the misalignment of the printed coupon with respect to its intended position.

The measured misalignment is shown in Fig. 10, where each data point corresponds to a printed coupon. The *x* axis represents the distance between the facet of the laser and the edge of the dummy mesa that stands for the edge of the trench on the SOI chip, whereas the *y* axis represents
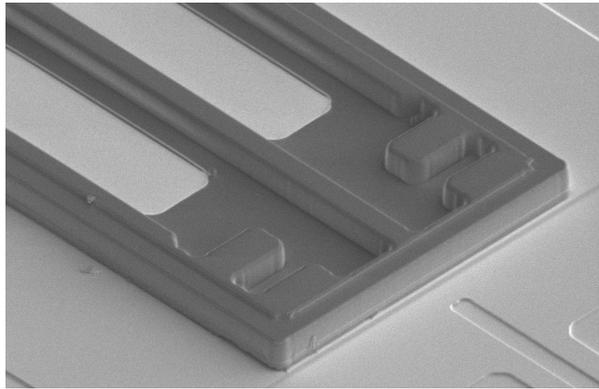
Fig. 9. SEM image of a coupon printed on a dummy silicon substrate. The features patterned on the substrate are used to measure the misalignment of the printed laser with respect to the intended position.

the lateral misalignment between the III-V waveguide and a dummy $2\,\mu m$ wide recess that stands for the SSC on the SOI chip (these dummy features can be seen in front of the laser coupon in Fig. 9). The measurement of the misalignment is carried out with the built-in calibration of a SEM observing the printed coupons in a top-down view. The error in the measurement, indicated by the error bars in Fig. 10, is estimated to be $50\,nm$ in both axis (note that the diameter of the data points in Fig. 10 corresponds to $100\,nm$ along the y axis). The average distance is $750\,nm$ with a standard deviation of $130\,nm$, whereas the average lateral misalignment is $420\,nm$ with a standard deviation of $400\,nm$.

The origin of the error in the average position stems from when the user first manually selects the patterns to be recognized. The resolution and clarity of the images are limited, which results in pattern edges that are not perfectly sharp lines but rather bands with a width of several pixels. If the pattern is a rectangle for instance, it is expected that the rectangle selected by the user based on the blurry edges of the imaged pattern will be offset by a few pixels with respect to the real position. With a resolution of $250\,nm$ per pixel, even an error as small as two pixels results in an initial systematic error of $500\,nm$. It should be noted that the average position can be tweaked in subsequent transfer printing operations by adjusting the offset that the pattern recognition software applies between the centers of the patterns on the source and the target. However, it is wise to allow for some intentional longitudinal misalignment in order to make sure that all the lasers are printed inside the trench. If we adjust the average distance to be too close to zero, then we can expect roughly half of the coupons to be printed with their front facet on top of the trench, which would prohibit optical coupling. That explains why we get a larger misalignment in the x axis in Fig. 10.

We have used Focused Ion Beam cross sectioning to examine the vertical misalignment between the quantum wells and the SOI waveguide layer and it has been found to be under $100\,nm$. This small misalignment is attributed to two possible effects. First, the epi was designed for a trench that would reach the silicon substrate interface exactly. However, the process to etch the trenches slightly overetches into the silicon substrate. Second, it is possible that the coupon does not sit perfectly flat on the substrate, so a deviation of a few tens of nm seems plausible. Figure 11 shows two FIB cross sections carried out on the SOI chip with transfer printed coupons. The left panel shows a cross section on the coupon side, whereas the left panel shows a cross section on the SOI side, where a patch of the $220\,nm$ silicon layer can be seen. The distance between the silicon substrate and both the quantum wells and the $220\,nm$ silicon can be measured from these images.

The dummy silicon substrate was cleaved very close to the facet of the coupons so that the
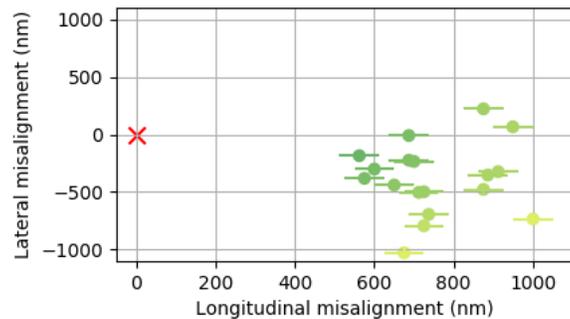
Fig. 10. Misalignment of the coupons with respect to the ideal position marked with a red *x* at (0, 0). The mean absolute lateral misalignment is 420 nm with a standard deviation of 400 nm. The mean longitudinal misalignment is 750 nm with a standard deviation of 130 nm.
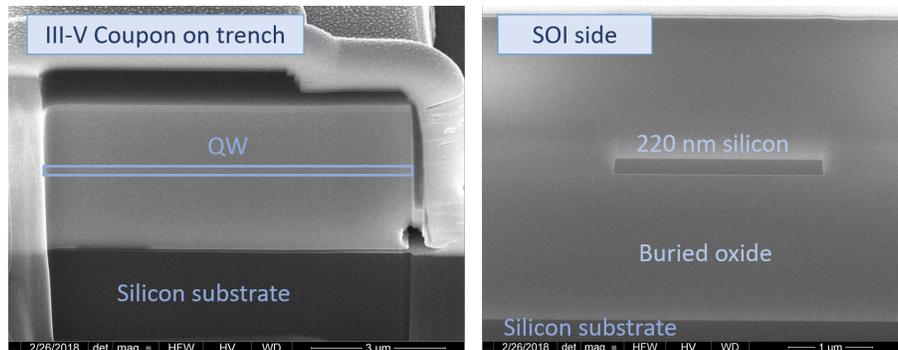
Fig. 11. FIB cross section of a printed coupon (left) and the SOI chip (right). The quantum wells have been highlighted for convenience.

output of the lasers could be measured by positioning a free space detector directly in front of the chip. The output power of the lasers as a function of the bias current is shown in Fig. 12. We observe a significant spread of the output power for different, although nominally identical lasers, nevertheless obtaining over 10 mW optical output power at 100 mA bias current for the best devices. The temperature of the substrate was not controlled in this experiment. The differential resistance at 50 mA bias current is in the range of 25 Ω to 50 Ω. The L-I curves terminate either at 100 mA or at the set compliance value of 2.5 V.

The optical power as a function of the driving current was also measured for the laser coupons that were transfer printed and post-processed on the photonic chip. In that case, the output of the lasers couples into the SSC which leads into the waveguide and a vertical grating coupler. The optical power in the photonic integrated circuit waveguide is shown in Fig. 13. In this case we also observe the spread in the curves for different lasers. The temperature of the substrate was kept at 20 ºC.

The obtained waveguide-coupled output power is slightly under 1 mW for the best structures at 100 mA drive current. With a fiber-to-chip coupling efficiency of −5 dB this results in 300 μW fiber-coupled optical power. Comparison of the power values in Figs. 12 and 13 seem to indicate an insertion loss of −10 dB. However, the fact the these lasers are printed on two different targets makes their direct comparison not straightforward, since it is not clear yet how the quality of the bonding affects performance in general and thermal dissipation in particular.
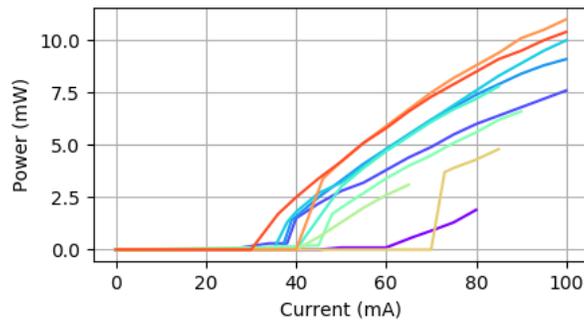
Fig. 12. Optical power of the lasers printed on the dummy silicon substrate without temperature control. The output of the lasers is measured directly by a free space detector.
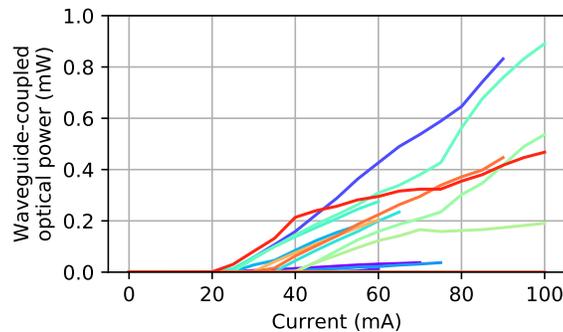
Fig. 13. Optical power in the silicon waveguide after coupling the laser output to the integrated circuit. The temperature of the substrate is kept at 20 ºC.

Figure 14 shows a representative set of LI curves at different temperatures measured on a particular laser coupon printed on the photonic chip. The power values correspond to the fiber-coupled power, after the grating coupler. The threshold current increases from 34 mA at 20 °C to 58 mA at 35 °C. The output power at 80 mA for this particular laser coupon decreases from 2.3 µW at 20 °C to 0.9 µW at 35 °C. These results seem to indicate that we have not been able to achieve a tight enough interface between the III-V coupon and the silicon substrate in order to take full advantage of its thermal conductivity.

The spectra of several lasers printed on the photonic chip are shown in Fig. 15. The legend shows the current at which each coupon was operated. The temperature was kept at 20 °C.

The free spectral range extracted from the spectra shown in Fig. 15 is around 0.8 nm, which agrees well with the value calculated from the simulations of the modes in the III-V waveguide at different wavelengths around 1550 nm, from which the group velocity can be extracted and then the free spectral range calculated.

The large variation in the L-I curves of the lasers makes it very difficult to work out the coupling losses by comparing the output power of the lasers printed on planar silicon (Fig. 12) to the output power of the lasers printed on the photonic chip (Fig. 13). Nevertheless, we believe this is an important stepping stone for the integration of III-V semiconductor lasers on a silicon photonic integrated circuit.
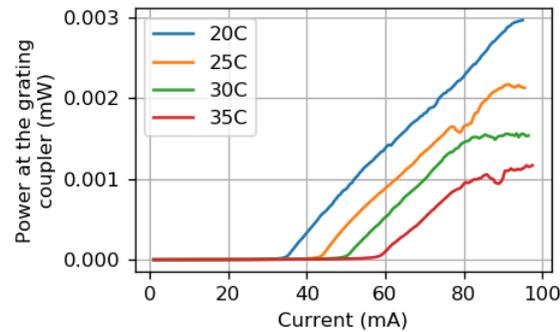
Fig. 14. LI curves measured at the grating coupler for a particular laser printed on the photonic chip. Each curve corresponds to a different temperature of the stage.
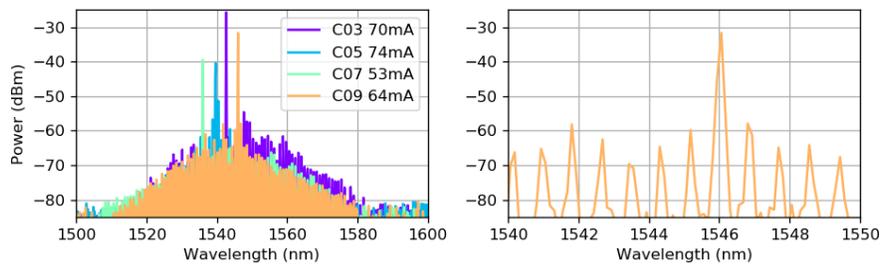
Fig. 15. (Left) Spectra of different coupons printed on the photonic chip. The measurement is taken at the grating coupler on the SOI chip. The substrate temperature is kept at 20 ºC. The legend shows the driving current for each laser. (Right) A detailed view of the area around the peak for one of the spectra.

4.   Conclusion

We have successfully integrated electrically pumped C-band, etched facet Fabry-Pérot lasers on a photonic chip by transfer printing. The lasers have been pre-processed on their native substrate, transfer printed and post-processed in a trench defined on the photonic integrated circuit, and their output has been successfully edge coupled into the photonic circuit through a SSC. After pre-processing no damaged or collapsed coupons are observed, and random pick ups across the source wafer seem to indicate a good yield of the pre-processing stage. 17 out of 20 trenches were successfully printed on the photonic chip, suggesting a good yield of the transfer printing process at this stage. All the coupons transfer printed on the photonic chip exhibited lasing.

We measured optical power as high as 1 mW in the PIC waveguide. The main limitation of the current results stems from the low uniformity in the quality of the contacts across coupons, which subsequently impact the I-V and L-I curves, and the fact that we cannot measure the emission of the same laser coupon with and without coupling to the PIC. As a result, it becomes difficult to estimate the coupling losses at the SSC. Because the lasers cannot be characterized on their native substrate, it is challenging to estimate the effect of the bonding quality on the performance of the printed lasers. Work is currently underway to address these issues and to improve the contacts and the overall performance of the lasers as well as the quality of the bonding.

Despite these shortcomings, we believe the process can be optimized to deliver improved results. Furthermore, the integration approach presented here has the potential to improve the

thermal impedance of the lasers with respect to wafer bonded devices, and the transfer printing process can be scaled beyond the capabilities of traditional flip-chip integration.

Funding