Transfer-printing for heterogeneous integration

B. Corbett¹*, R. Loi¹, J. O'Callaghan¹, L. Liu¹, K. Thomas¹, A. Gocalinska¹, E. Pelucchi¹, A. J.

Trindade², C. A. Bower², G. Roelkens³ and B. Roycroft¹ ¹Tyndall National Institute, University College Cork, Dyke Parade, Cork, Ireland ²X-Celeprint Limited, Lee Maltings, Cork, Ireland ³Ghent University-Imec, Technologiepark-Zwijnaarde 15, Ghent, Belgium *brian.corbett@tyndall.ie

Abstract: Transfer-printing provides a highly versatile methodology to heterogeneously and intimately integrate diverse photonic and electronic components in close proximity onto silicon photonics platforms. This technique can enable a manufacturing route to powerful photonic integrated circuits.

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1. Introduction

Silicon based technology has served the electronics industry well providing highly functional low cost circuits to the consumer. Photonics on the other hand has struggled to reach the mass market with the obvious exception being silicon camera chips. While monolithic integration of devices on InP has provided high performance circuits this approach is ultimately limited in scaling by circuit complexity allied to the available size of high quality InP wafers. Silicon based photonic circuits is thus a clear basis to both scaling the component count and to mass manufacturing. The challenge is to combine functional components that are optimally manufactured on specific non-silicon substrates. For example, the light source is currently best realized on an III-V substrate (InP, GaAs or GaSb) using an engineered epitaxial structure with quantum well or dots as the light emitting material. III-V or other materials can be used to provide wavelength specific detection, modulation, isolation and other opto-electronic functions. Consequently, it is necessary to integrate components providing these specialized functions with the Si based waveguides. Integration using wafer-bonding of sections of the appropriate III-V wafer materials to the prepared Si circuits followed by substrate removal and device processing is capable of providing engineered evanescent coupling between the III-V and Si waveguide and has been successfully commercialized. However, this approach requires processing of the III-V element on 150-300mm diameter wafers, employs a large area of material that is not finally used for devices and is limited in how close different photonics functionalities can be placed. An alternative proven approach is to butt couple III-V gain blocks to Si waveguides by flip-chip placement. This allows the use of known-good-die (KGD) but is limited in speed and flexibility. Our approach is to pre-fabricate devices in an environment set up for III-V materials and to transfer the essential parts of these devices (i.e. the epilayers) from their native substrate to a different target substrate based on the transfer-printing technology. Subsequently, it is possible to integrate the laser light with the following waveguides using established signal redistribution processes. This allows the III-V devices to be produced as at present, uses only the minimum amount of material and overcomes wafer size mismatch issues.

2. Transfer-print technology

Micro-transfer-printing allows the massively parallel movement of materials or devices (coupons) from source substrates to a target substrate enabling their heterogeneous integration [1]. The technique requires a means to separate the coupons from the source substrate while holding them in place in a registered manner. For III-V materials we have incorporated an additional sacrificial layer at the start of the growth of the epitaxial structure to enable this separation. We have typically used a 500nm-thick layer for the release. The composition of this layer needs to have a very high etch selectivity for the adjacent layers. We have investigated lattice-matched AlGaAs and, GaInP and AlInP as release layers for GaAs-based devices and InGaAs and InAlAs as release layers for InP-based structures. Some of these materials undercut in a highly crystallographic fashion while others etch in a non-crystalline manner. This affords advantages in different situations. Particularly, the orientation independent etch of InAlAs in ferric chloride is effective for release of all InP based devices (lasers, modulators, detectors) [2]. During the undercut, the device coupons are held in place using resist tethers. The thicknesses of the coupons depend on the device structure and are typically between 1 and 5 μ m. Following the release, the coupons are then individually suspended in an array format on the source wafer. A structured elastomeric (PDMS) stamp is then used to pick up selected devices in a grid format. Due to the rate dependent adhesion it is possible to transfer the selected coupons to the stamp by fracturing the tethers at engineered locations and then to transfer these coupons to the target substrate

with the same grid. The receiving substrate needs to be locally flat which can be achieved by suitable preparation or by using a layer (e.g. 50-1,000nm) of polymeric material. The device release is due to the slow movement and moment induced by the shear movement of the posts. In principle, many thousands of devices can be transferred in parallel. The coupons can be located on the target substrate with micron scale precision (and better) by using fiducial marks on the devices and the substrate. Coupling between the III-V device and the Si waveguide can be achieved by means of butt coupling, by evanescent means [3] or by use of gratings.



Fig.1: Schematic of the pickup and transfer process shown for an individual device. The devices are transferred in an epitaxial side up configuration.

The advantages of this scheme include that the highest quality source materials are used while making efficient use of these expensive materials. More devices per unit area can be obtained as the individual devices can be placed within 10s of microns of each other on the source wafer since space does not need to be allocated for full bond pads. The technique can use wafers of different diameters for the different source materials and can print to large diameter target substrates. The devices can be manufactured using any needed specialized processes and can be pre-evaluated prior to transfer. Precise (lithographic) alignment to underlying waveguides can be obtained by post-processing the associated waveguides on the transferred coupons. High throughput is obtained through wafer scale transfer of 2D arrays of devices in parallel with the step and repeat cycle taking <40s. Multiple source materials can be selected in sequence and be transferred to locally flat structured substrates such as fully processed target wafers. Thus, lasers, amplifiers, modulators, detectors, electronic and other components can be transferred. These devices can be transferred adjacent to each other thus allowing arrays of complex photonic circuits to be realized on the target wafers. The extra steps needed to implement the technique are a release layer (or equivalent) and the associated layers for waveguiding and height control are included in the epitaxial stack. Additional processing steps for addressing the release layer, the tethering of coupons, facet formation and redistribution may be required. A transfer method is required.

As an example, etched-facet ridge waveguide Fabry-Perot lasers emitting at 1550nm were integrated onto different silicon photonics substrates by transfer-printing. We compared the thermal performance for 500 μ m long lasers on the source InP with those printed directly, without adhesive layer, on silicon and on top of a silicon-on-insulator (SOI) wafer comprising of 220nm Si / 2 μ m SiO₂ / Si substrate. We measured the thermal impedance on the native substrate to be 57K/W which was reduced to 38K/W after printing to the Si substrate. For lasers printed on the SOI a thermal impedance of ~ 94K/W was obtained which is more than two times higher than that of the laser printed on the Si substrate [4]. These values match the simulated results and show the advantage of the thermally conductive Si over transporting the heat through the buried oxide.



Fig. 2: Front facet light current voltage characteristics of 1550nm laser transferred without adhesive to Si substrate.

3. Circuit integration

We used an end-fire approach to couple the laser light to silicon (SOI) waveguides each with an out-coupling grating. The laser structure is designed to have a large spot size with controlled thickness, an InAlAs release layer with controlled lower InP cladding thickness to match the laser mode with that of the Si waveguide. The lasers were prepared by etching the facets with the rear facet coated by a dielectric and reflective metal (i.e. Au) and the front facet with an integrated antireflection coating. The p- and n-type contacts are formed on the front surface along with probing pads. The lasers are prepared in a manner by which the front facet is free of tethers preventing any restrictions on how close the laser can be place with respect to the waveguide. The Si waveguides were processed on the imec multi-project run and feature tapered waveguides to expand the mode, improving the coupling efficiency and the positional tolerance. The facet in the Si circuit is prepared by using Cr mask and dry etching. The process is completed by wet etching of the buried oxide to have a smooth Si surface at a controlled depth with respect to the waveguide. The lasers are transfer-printed without any adhesive.



Fig. 3: Left - shows the fabricated lasers with the tethers prior to the release etch. The centre shows 4 printed lasers transfer-printed into the prepared trenches in the SOI wafer and, right, shows the alignment of the etched facet laser with respect to the Si waveguide.

The laser power was collected from the grating with a single mode fiber. The coupled power from the chip was greater than 0.3mW, implying that power coupled from the laser to the Si waveguide was greater than 2mW with an estimated coupling efficiency >40%. The same fiber was used to externally injection lock the integrated laser using an external cavity laser. A locking range of 16nm was achieved with a with an injection power in the fiber of 8mW. Direct modulation of the laser chip during optically injection resulted in the generation of tunable optical combs on the order of 40-50GHz width, at modulation frequencies from 1 to 5GHz.



Fig. 4: Left - injection locked spectra of on chip laser and right - comb spectrum under 5GHz modulation while injection locked.

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