

III-V-on-silicon Photonic Transceivers

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Abstract— In this paper we give an overview on our work on silicon photonic high-speed transceivers and the co-integration of III-V opto-electronic components on the silicon photonic platform.

Keywords— Silicon Photonics, Heterogeneous integration, Transceivers

I. INTRODUCTION

Silicon photonics is emerging as a prominent platform to realize highly-integrated high-speed optical transceivers, for use in a wide range of applications, ranging from intra-datacenter interconnects, over inter-datacenter to cloud radio access networks and metro and long-haul links. In this paper we elaborate on several implementations of such transmitters and receivers on the imec silicon photonics platform. We especially discuss the realization of 56 Gbaud and 100 Gbaud transmitters and receivers combined with BiCMOS electronics. Different modulation formats are used, including NRZ, RZ, EDB and PAM-4. While silicon photonics technology provides a comprehensive platform for building integrated transceivers, laser sources and optical amplification is a functionality that still needs to be implemented using III-V semiconductors. Therefore, we will report on some key realizations of III-V-on-silicon devices and discuss a novel III-V-on-silicon heterogeneous integration approach, micro-transfer-printing, that provides a scalable path to III-V integration on full-platform silicon photonic wafers.

II. HIGH-SPEED SiPH OPTICAL TRANSCEIVERS

A. 100Gbaud NRZ and EDB transceiver

High-speed optical modulators and photodetectors can be implemented on the Si photonic platform through selective epitaxial growth of (Si)Ge, to form (Si)Ge photodetectors and electro-absorption modulators. The compactness of these devices results in a low capacitance and hence high bandwidth, beyond 67 GHz (instrument limit). Using such devices, in combination with high-speed BiCMOS electronics incorporating a feed-forward equalizer, 100Gbps NRZ and electrical duobinary transmission and reception was realized, using the system shown in Fig. 1. In this case the lateral p-i-n structure implemented in the GeSi waveguide can serve both as electro-absorption modulator and photodetector [1].

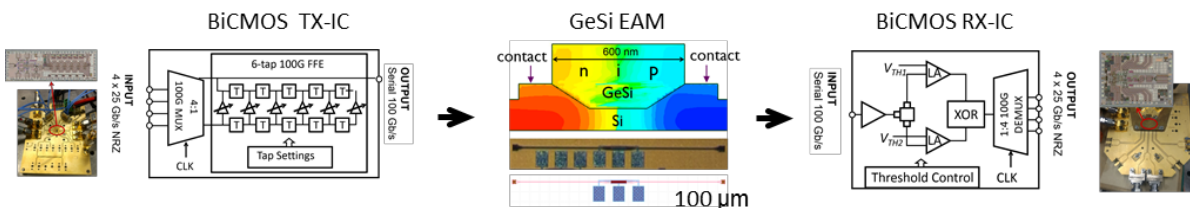


Fig. 1: (left) micrograph and architecture of the TX-IC consisting of a 4:1 MUX and a 6-tap FFE; (center) cross-section and layout of the 80 μm long, waveguide-integrated GeSi EAM/PD; (right) block diagram and micrograph of the RX-IC consisting of 2 comparators (for EDB decoding) and a 1:4 DEMUX.

B. 112Gbit/s PAM4 transceiver

Recently, the industry has adopted PAM-4 as the modulation format of choice for 100 Gbps per-lane transmission over 500 m, 1 km and 2 km distances. When using a single-modulator implementation to realize such 4-level signals, the modulator and driving electronics need to be linear to realize equidistant levels. This is however difficult to realize and often one has to resort to power-hungry digital signal processing (DSP) and digital-to-analog (DAC) converters. This way, they consume significantly more power than their NRZ counterparts at the same data rate. In order to mitigate this issue, an optical DAC scheme was devised where two EAMs were incorporated in a Mach-Zehnder interferometer (Fig. 2), such that each EAM could be driven with a NRZ signal, thereby greatly relaxing the requirements on driver, modulator and DSP [2].

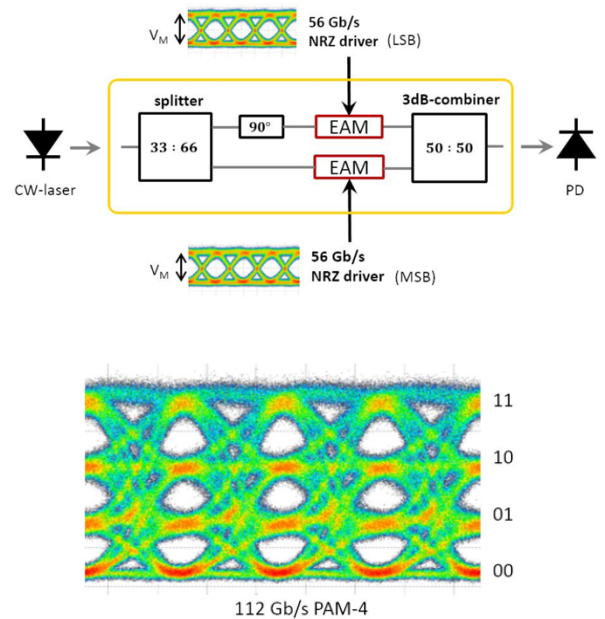


Fig. 2: (top) optical digital-to-analog conversion scheme to generate 56Gbaud PAM-4; (bottom) resulting 112Gbit/s eye diagram

C. 104Gbaud RZ/PAM4 transmitter

To realize high baud rate signals the time multiplexing of the lower baud rate electrical signals can be done in the electrical domain or in the optical domain. Implementing this functionality in optics reduces the power consumption of the multiplexing, however at the cost of requiring a short-pulse laser (typically a mode-locked laser). Such an optical time division multiplexed transmitter was demonstrated in SiPh using a 26GHz repetition rate short-pulse source that is split, delayed and fed to an array of 4 Ge EAMs, each modulated with 26 Gbaud NRZ or PAM-4 data. This allowed the demonstration of a 104 Gbaud NRZ/PAM4 transmitter [3].

III. HETEROGENEOUS INTEGRATION OF III-V SEMICONDUCTORS

In order to complete the toolkit for building photonic systems-on-chip there is a need to incorporate III-V semiconductor lasers and optical amplifiers on the silicon photonics platform. The III-V can be integrated on wafer-scale using die-to-wafer bonding or using a new integration technique, called micro-transfer-printing.

A. III-V-on-silicon devices based on die-to-wafer bonding

Die-to-wafer bonding based on molecular bonding or adhesive bonding is an established approach for the integration of III-V semiconductors (InP-based, GaAs-based) on silicon photonics. Key components that have been realized using this approach include single wavelength DFB lasers, widely tunable lasers, mode-locked lasers and high-power semiconductor optical amplifiers. In Fig. 3 high-power III-V-on-Si SOA characteristics with >17 dBm output saturation power are shown [4].

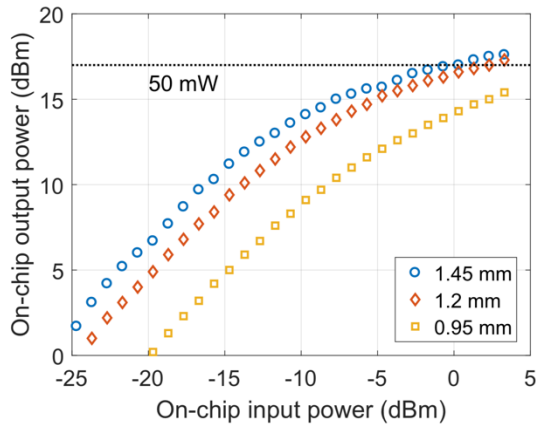


Fig. 3: On-chip optical output power versus on-chip input power for 3 III-V-on-Si high-saturation-power optical amplifiers of different length

B. III-V-on-silicon micro-transfer-printing

A newcomer in the field of III-V-on-silicon photonic integrated circuits is micro-transfer-printing (μ TP), illustrated in Fig. 4. μ TP combines advantages of flip-chip integration (pre-processing/testing of the III-V optoelectronic devices prior to heterogeneous integration) and wafer bonding (high throughput integration). The process starts with the definition of the III-V optoelectronic components (SOAs, lasers) on a III-V source wafer, which has the active epitaxial layer stack grown on top of a release layer (e.g. InGaAs for the InP material system). After

patterning of the device and the release layer, the structures are encapsulated and the release layer is selectively removed, leaving the III-V components attached to the III-V substrate by thin tethers. With a stamp one or more III-V components can be picked up from the source wafer and printed onto a silicon photonic target wafer. Then, the encapsulation is removed and the III-V devices are electrically contacted on wafer level. This approach enables pre-testing of the III-V devices on the source wafer, similar to flip-chip integration, but also massively parallel integration, similar to the die-to-wafer bonding approach. The III-V devices are micro-scale, so the silicon photonics back-end flow is not disturbed. Only a local opening to the silicon device layer is needed, similar to the flip-chip integration approach.

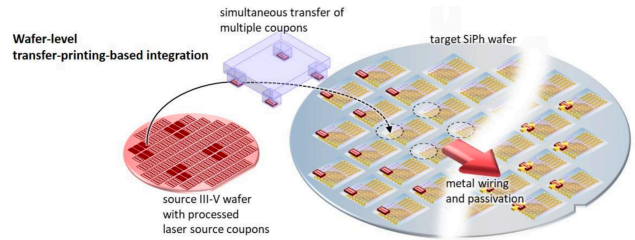


Fig. 4: Schematic of the micro-transfer-printing approach

At the conference we will elaborate on the development of the technique and the realization of different III-V-on-silicon devices using micro-transfer-printing including high-speed III-V photodiodes, semiconductor optical amplifiers, Fabry-Perot lasers, DFB lasers and widely tunable lasers [5].

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