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Invited Paper

Programmable silicon photonic circuits powered by MEMS

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ABSTRACT

We present our work to extend silicon photonics with MEMS actuators to enable low-power, large scale programmable photonic circuits. For this, we start from the existing iSiPP50G silicon photonics platform of IMEC, where we add free-standing movable waveguides using a few post-processing steps. This allows us to implement phase shifters and tunable couplers using electrostatically actuated MEMS, while at the same time maintaining all the original functionality of the silicon photonics platform. The MEMS devices are protected using a wafer-level sealing approach and interfaced with custom multi-channel driver and readout electronics.

Keywords: Silicon Photonics, Programmable Photonics, Micro-electromechanical Systems

1. INTRODUCTION

Silicon Photonics is becoming an increasingly industrially relevant technology. Its compatibility with CMOS manufacturing infrastructure has enabled the emergence of multiple industrial fabrication platforms that can scale to high volumes.[1] At the same time, the quality of the fabrication steadily increases, allowing larger and more complex circuits with good yield. This circuit scaling is also enabled by the high refractive index contrast of the silicon material system, confining light in submicrometer waveguides that can be packed closely together.

Powered by these scaling capabilities, a new type of photonic circuit is gaining traction: programmable photonic circuits.[2] In contrast with the specialized photonic integrated circuits we see today, a programmable photonic circuit consists of a more generic mesh of waveguides, tunable couplers and phase shifters. With these, the flow of light can be electrically controlled at run time. Such circuits are useful for performing optical arithmetics, such as matrix-vector multiplication,[3] but can also be used to build the optical equivalent of an electronic field-programmable gate array (FPGA).[4] They can also present an entirely new use model for photonic

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circuits, which does not require the upfront designs and fabrication of a custom chip, but can use a generic chip that can be reconfigured at run time.[5]

As photonic circuits become larger, they require an increasing amount of electrical controls, in the form of tunable couplers or phase shifters. As the light has to pass through many of these actuators, they need to have a low optical insertion loss and preferably also a short optical path length. It is also desirable that the power consumption of these elements is low, as hundreds or thousands need to be driven at the same time. And this is not trivial to accomplish with the traditional method of inducing a phase shift in a silicon photonics waveguide: a heater. Even when applying a thermal undercut[6] such heaters still require milliwatts of power, and as more heaters are deployed closely together on the same chip, the thermal crosstalk becomes difficult to manage.

The other phase-shifting mechanism which is natively present on a silicon photonics chip is carriers, also called the plasma dispersion effect.[7,8] While this provides the most common method for implementing high-speed modulators, the effect is quite weak, requires long optical lengths, and induces significant optical loss. Such phase shifters are therefore well suited for single high-speed modulators, but not cascadable into a larger circuit. Alternative phase-shifting techniques require electro-optic materials which are not always easy to integrate with an existing silicon photonics platform.[9,10]

Micro-electromechanical devices (MEMS) also make it possible to implement electro-optic actuators: by mechanically moving material around, the optical properties can be changed.[11,12] For instance, two parallel waveguides can be brought in close proximity, and the coupling rate can be controlled by adjusting the distance between the waveguides.[13] Likewise, a phase shifter can be implemented by moving a perturbation inside the evanescent field of a silicon waveguide mode.[14] This can be a strong effect, as it is actual silicon that is moved, creating a very large refractive index difference between the presence of absence of the material.

Silicon MEMS are also interesting from the point of view of process integration: MEMS are already fabricated with the same toolset as silicon photonics and electronics. However, the inherent nature of MEMS devices does not make it straightforward to combine them with existing silicon photonics. Movable waveguide components need to be free-standing, which means they need to be suspended in air or vacuum. But traditional silicon photonics waveguides are encapsulated by an cladding of silicon dioxide and other dielectrics, especially because other active elements such as modulators and germanium photodetectors are also electrically connected by metal wiring layers overhead.

This is what the European project MORPHIC has set out to do: integrate high-efficiency MEMS actuators into an existing silicon photonics platform without sacrificing functionality and enabling scaling towards large circuits and programmable photonics. This comes with many challenges:

- **Process integration**: The processing of the MEMS devices should not affect the existing silicon photonics devices. As the MEMS devices are free-standing, no subsequent deposition or liquid-based process steps can be added, so the release step should come at the very end.
- **Protection of the MEMS devices**: The free-standing silicon devices are quite strong, but still fragile. they need to be protected from particles, especially when the chips need to go through additional packaging steps.
- **Phase shifters and tunable couplers**: Given the constraint of the existing silicon photonics platform (e.g. layer composition and thicknesses), efficient phase shifters and tunable coupler actuators need to be implemented. This requires a combination of optical, electrical and mechanical design.
- **Circuit design**: Combining MEMS actuators with existing silicon photonics into larger circuits introduces the need for multiple transitions between air-clad and oxide clad devices. Partitioning to aggregate larger subcircuits into single MEMS cavities can have a positive effect on optical losses and circuit footprint.
- **Electrical interfaces**: The many compact MEMS actuators need to be connected to their electrical driver circuits. This requires many dense electrical interfaces from the photonics chip to the drivers, which is complicated by the presence of the areas with free-standing MEMS devices where no metal routing is possible.

- **Electrical driver circuits**: the high driving voltage (+20V) for the MEMS actuators requires custom driver electronics that can be scaled up easily to hundreds of channels.
- **Optical and microwave interfaces**: In addition to the large number of driving channels, the photonic chips also needs fiber interfaces to the outside world, as well as high speed microwave/RF connections for the modulators (input) and photodetectors (output).
- **Software control**: A photonic chip with hundreds of actuators needs a software layer to manage it, translating the high-level user requirements into driving strategies for each electronic channel.

In the following sections we will describe the MORPHIC approach and the current progress. We already reported earlier on this work,[15] where we discussed the initial results of the MEMS devices. Here, we will go deeper into the devices, the wafer-level protection and the scaling of the electrical input/outputs.

2. SILICON PHOTONIC MEMS DEVICES

Silicon photonic MEMS are, by themselves, not a new proposition. There have been numerous demonstrations of electrostatically actuated waveguide devices for use in phase shifters,[14,16–19] tunable couplers[20] switches,[21–24] tunable filters[25] or tunable grating couplers.[26] Most of these demonstrations have in common that they are implemented in a specialized silicon photonics platform, incompatible with existing silicon photonics devices. The difficulty of bringing together MEMS devices and traditional silicon photonics is obvious: in a traditional silicon photonics platform, the waveguides are complemented by active functions such as plasma-dispersion modulators with p(i)n junctions, and epitaxially grown germanium photodetectors.[27] These active devices are encapsulated in a dielectric stack and electrically connected using multiple layers of copper or aluminium tracks. The silicon waveguides are therefore buried under a multi-micrometer metal/dielectric stack.

Silicon photonic MEMS, on the other hand, require free-standing, movable silicon structures in the waveguide layer. This means that locally, the thick back-end-of-line (BEOL) stack needs to be removed, and the waveguides need to be released from their substrate. This has to be done locally, without affecting the performance of the surrounding active components and metal interconnects. Once the waveguide MEMS structures have been released, any material deposition or use of liquids should be avoided, which means this step should come last in the process flow.

2.1 Silicon Photonics and MEMS processing

Figure 1 shows the process flow as developed in the MORPHIC project. We started from the established iSiPP50G silicon photonics of IMEC, which boasts world-class passive performance, combines with high-speed modulators and germanium photodetectors that can operate in excess of 50Gpbs.[27] The platform also incorporates both tungsten and doped-silicon heaters, and has two layers of copper interconnects.

One of the final process modules in this platform allows for the local opening of the BEOL dielectric stack. Such a process step is often needed for specialized functions, such as waveguide sensors, where the surface of the silicon waveguides needs to be exposed. The etch of the thick BEOL stack is stopped just above the surface of the waveguide layer, resulting in a cross section that is similar to Fig. 1-4.

To release the freestanding waveguides, an aggressive isotropic etch based on vapor-phase hydrofluoric (vHF) acid is used. This mixture will attack not only the oxides around the waveguides, but also the dielectric stack elsewhere on the chip. Therefore, a protective layer needs to be deposited first. Aluminium oxide (AlOx) can be used for this purpose. To make sure that there are no unwanted channels through which the vHF can penetrate into the BEOL dielectric stack, the AlOx must be deposited directly on top of the silicon layers of the waveguides. Therefore, in a first step, the remaining oxide on top and on the side of the waveguides is removed using a wet buffered HF etch. Subsequently, atomic layer deposition (ALD) is used to deposit the AlOx protection layer. ALD is a very conformal deposition method, which covers well the edges and sidewalls. The AlOx is then opened using a plasma etch process over the metal bondpads and in the areas where the MEMS waveguides need to be released.

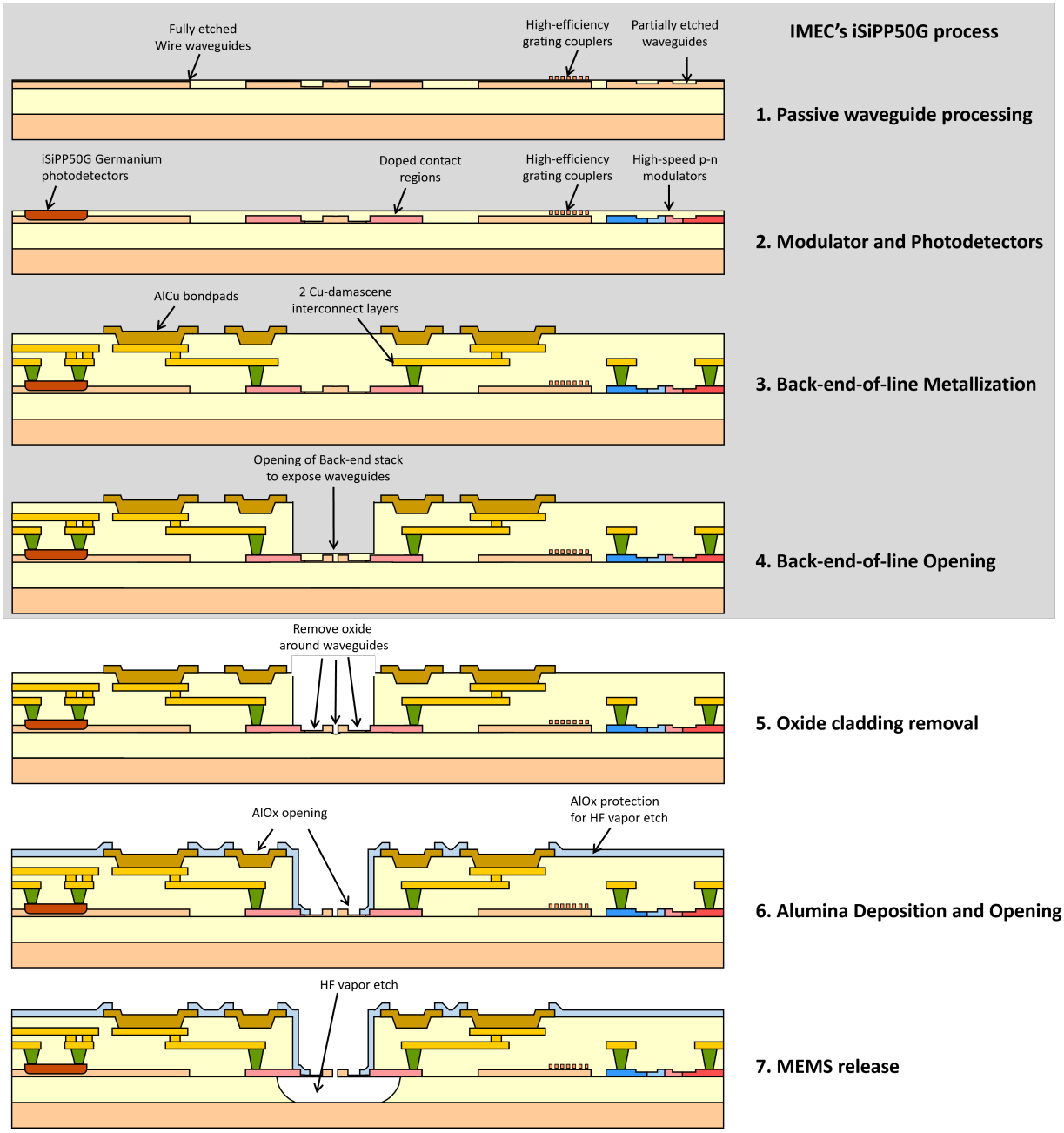

Figure 1. Fabrication Flow for Silicon Photonics MEMS. After the processing of passive and active devices, the iSiPP50g platform is finished with multiple metallization layers. These are then locally etched back, after which the remaining oxide around the waveguides is removed. An AlOx layer is deposited and opened on top of the metal contact pads and in the eares where the MEMS will be released with the final vapor-phase HF etch.

In a final step, the buried oxide underneath the MEMS waveguide devices is etched using vHF. As this is an isotropic etch process, the oxide is attacked both in the downward and the lateral directions. At least 2 μm of oxide is removed, to fully clear the silicon substrate underneath the freestanding waveguides. Further etch time determines how much the structures are laterally undercut. This undercut should not exceed the safety margin surrounding the exposed MEMS waveguide area, where a solid ring of silicon acts as a buffer to protect the BEOL stack from a vHF attach through the buried oxide.

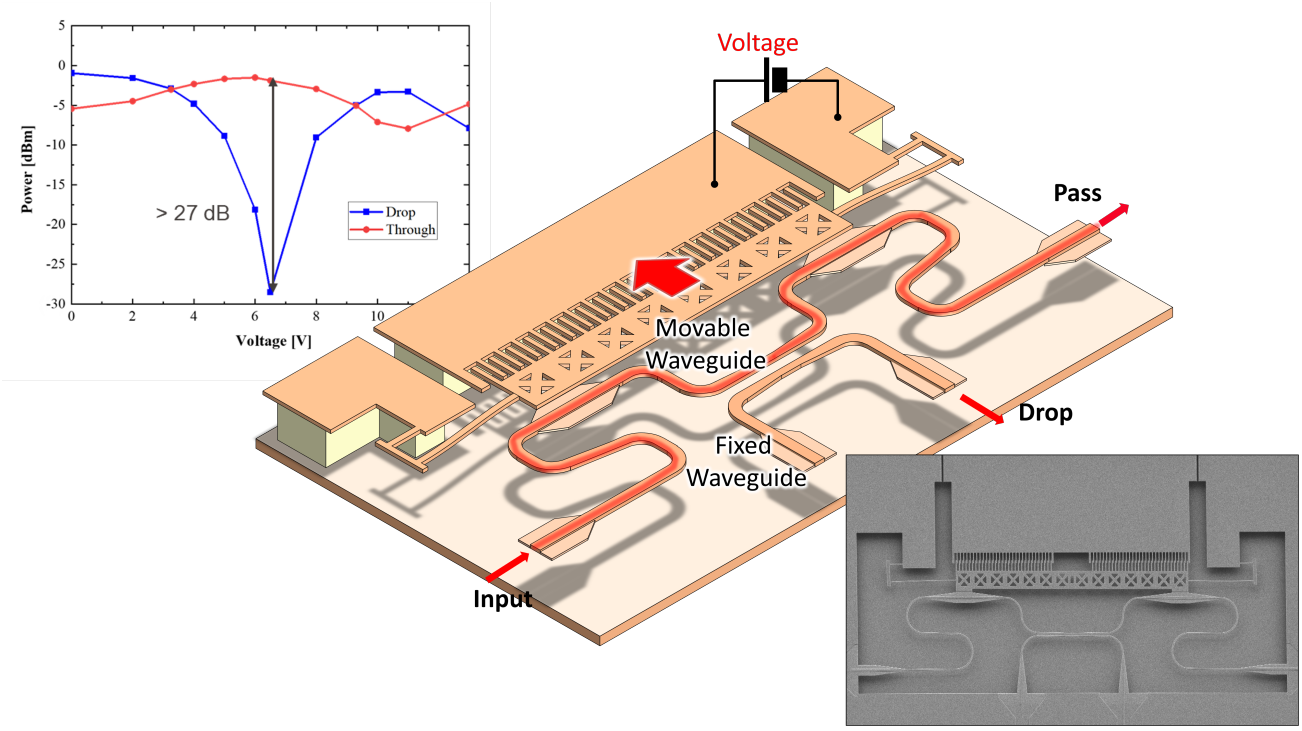

Figure 2. MEMS Tunable coupler implemented in the iSiPP50g process.[13] The light is coupled through a broadband directional coupler[28] where one side is attached to a lateral comb drive. By pulling the waveguides apart the operation can switch between bar state and cross state with 25 dB extinction ratio.

Note that all fabrication steps up to this point are compatible with wafer scale processing. IMEC's iSiPP50G process is executed fully on 200 mm wafers. For the subsequent MEMS processing, we have cored down the 200 mm wafers to 100 mm wafers, and the process steps were carried out in the Center for Micro and Nanotechnology (CMi) at EPFL.

2.2 Tunable Coupler

The basic concept of a tunable waveguide coupler using MEMS is quite straightforward. When two waveguides are brought in close proximity, they act as a tunable coupler. The narrower the gap between the waveguides, the stronger the coupling. Small displacements ¡1̃ µm are sufficient to change a directional coupler from 100% coupling to almost 0%, and the physical modification of the geometry enables large tuning of the extinction ratio. In Fig. 2 we see an example of such a tunable directional coupler where the spacing between the two waveguides is controlled by an electrostatic comb drive.[13] One waveguide is suspended by anchored in place, while the other waveguides has a curved path which acts as a mechanical spring.

The challenge with a good tunable coupler is broadband operation. A regular directional coupler in a high-contrast material system is very dispersive, and a MEMS tunable coupler would therefore only achieve the desired coupling for a single wavelength. The solution is to tweak the geometry of the coupler by tapering the waveguides. This provides a range of coupling strengths along the length of the coupler, which can be engineered to give a more broadband response.[28] With this customized directional coupler embedded in the MEMS device, we achieve an optical bandwidth of approximately 30 nm.

Instead of moving the waveguide horizontally, using a comb drive, we can also mode the waveguide vertically, using a parallel-plate actuator[29] consisting of a large area of suspended silicon and the silicon substrate. the advantage with this technique is that the device can be engineered to operate at a lower voltage, by using softer suspending springs and a larger capacitor area.

2.3 Phase Shifter

Electro-optic phase shifters are a key function in large-scale photonic circuits. Their performance is often characterized by the electrical power required to induce a π phase shift, or in the case of electrostatic actuation, the voltage V_π or voltage-length product $V_\pi.L_\pi$ to achieve a π phase shift. The MEMS phase shifters we implemented in the MORPHIC platform are based on lateral displacement in a single waveguide layer, and can be built using the same principle as the tunable coupler. Instead of using two identical waveguides which will strongly couple, we use one regular waveguide core and a much narrower beam of silicon. This acts as a perturbation but will not guide light on its own.[14] This is shown in Fig. 3. Using again a comb drive to change the separation between this thin silicon beam and the waveguide, we can tune the phase delay. Over a length of 50 m, we can already induce a 2π phase change, with a silicon beam on only one side of the waveguide.

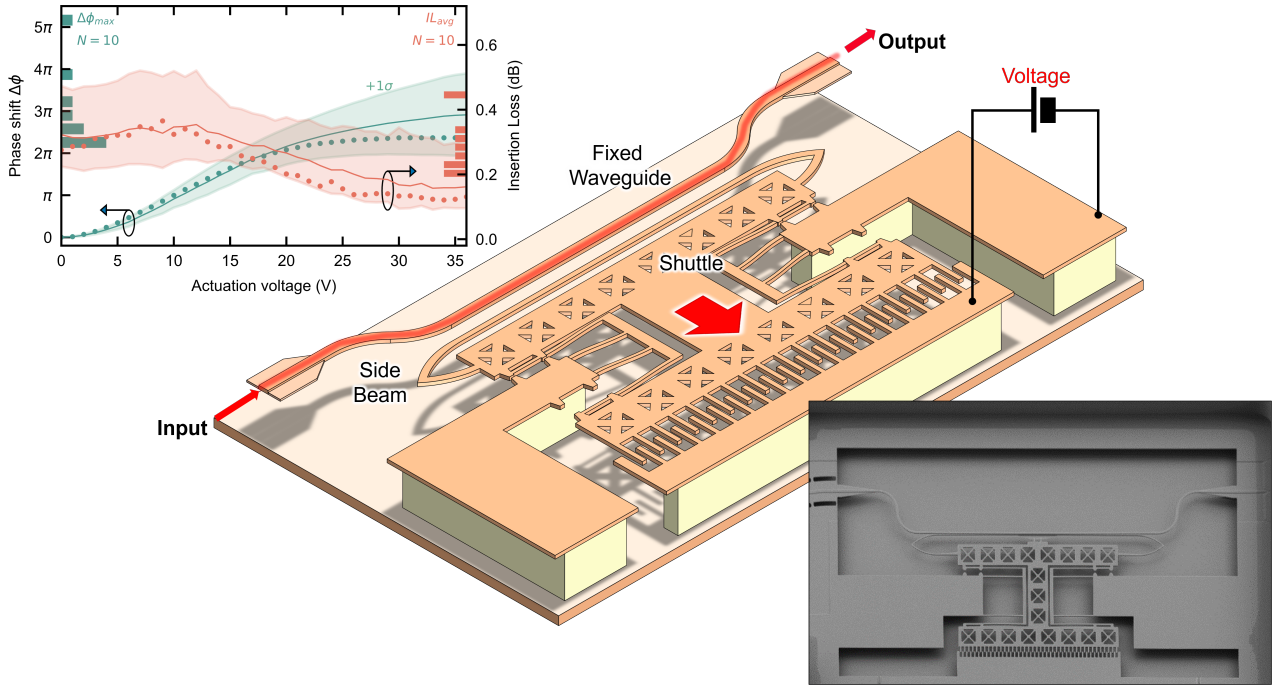

Figure 3. [14] The phase shift is induced by a narrow beam of silicon positioned parallel to the waveguide, where the distance between the beam and the waveguide can be adjusted using an electrostatic comb drive. The 50 µm long device achieves a 2π phase shift for an actuation of 20 V.

2.4 Switches

When we don't care about tuning over a full range of values (e.g. coupling between 0-100% or tuning a continuous phase range), we can further engineer MEMS devices to exhibit a more digital behaviour. An example is the 1×2 switch shown in Fig. 4.[24] This device physically switches the optical connectivity between a single input waveguide and two output waveguides by moving the tip of the input to the matching tip of the output. The device can be made very compact by optimizing the shape of the electrodes that perform the electrostatic attraction. Depending on whether a voltage is applied on either one of the electrodes, the shuttle waveguide will move towards output 1 or output 2. A strategically placed mechanical stopper makes sure the waveguide shuttle does not make electrical contact with the electrodes and prevents mechanical contact between the waveguide tips, which could lead to unrecoverable stiction.

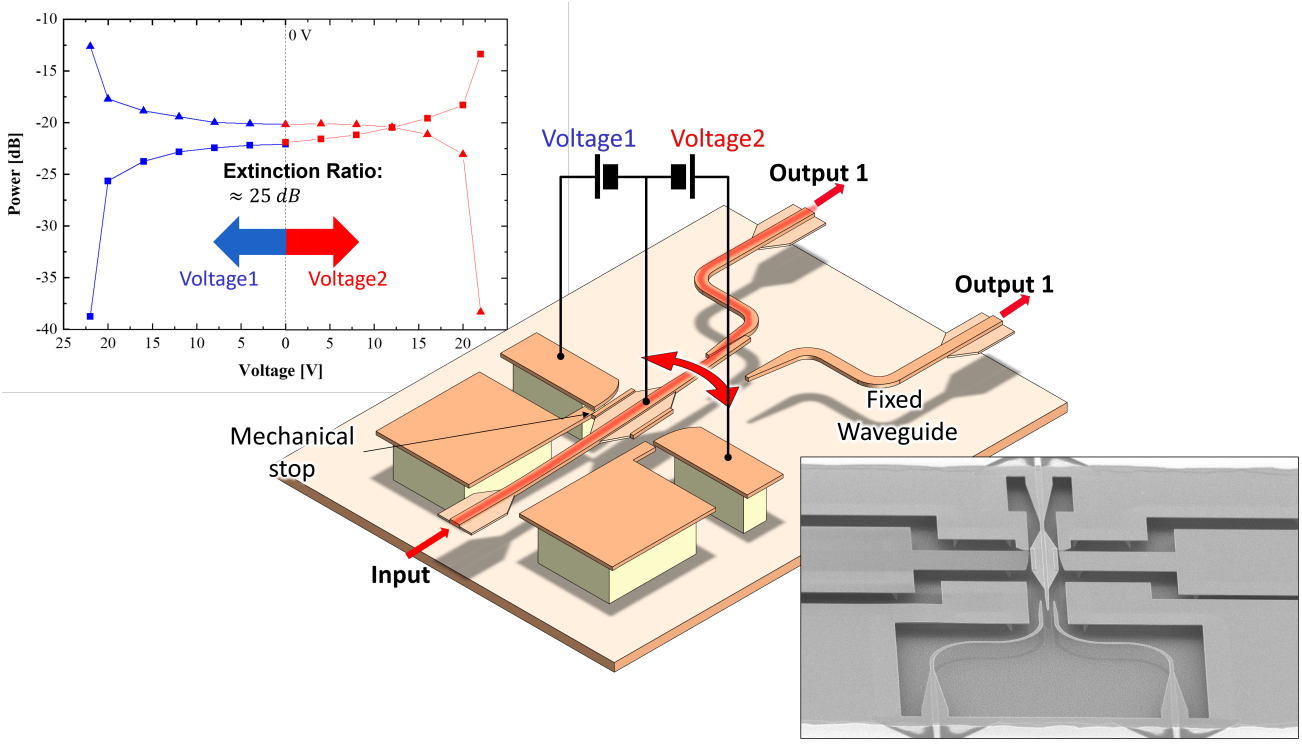

Figure 4. Compact single-pole double-throw MEMS switch implemented in the iSiPP50g platform.[24] The switch consists of a narrow suspended waveguide that can be pulled towards one of two side electrodes, coupling the narrow waveguide tip evanescently to the corresponding output waveguide.

3. PACKAGING SILICON PHOTONIC MEMS DEVICES

3.1 MEMS Protection by Hermetic Sealing

After the release process, the MEMS devices are now suspended, so they can be actuated. This also makes them very fragile: any particle from the environment or the packaging process steps can damage a waveguide both optically (scattering), electrically (short circuit) and mechanically (obstruction). This complicates any subsequent packaging processes and also makes the operation of the MEMS susceptible to any variation in the atmosphere (humidity, temperature, gasses).

The solution in the MORPHIC project is to hermetically seal the MEMS devices in a vacuum cavity using a silicon lid.[30–32] The wafer-scale process is schematically depicted in Fig. 5. The sealing lid consists of a silicon-on-insulator (SOI) wafer with a thick silicon layer. In a first step, this top layer is patterned with large 20 μm wide rings, and etched back to a thickness of 25 μm. The protruding rings then get metallized with gold (which can be either unpatterned, or removed outside the rings). Finally, a second deep reactive ion etch (RIE) is used to etch the contour of the lids.

The ring patterns on this wafer match rings defined in the AlCu bondpad metal layer of the silicon photonics wafer. Using a wafer-level thermocompression bonding process, the lid wafer and the silicon photonics wafer are fused together along these ring shapes. This can be performed in a vacuum or a controlled gas atmosphere. The process is described in detail in.[32]

When performed in a vacuum or low pressure, the hermeticity of the sealing can be verified by measuring the inward deflection of the silicon lid using white-light interferometry. This shows a high yield well over 90%,[30] and even devices which are not hermetically encapsulated are still protected from most environmental effects.

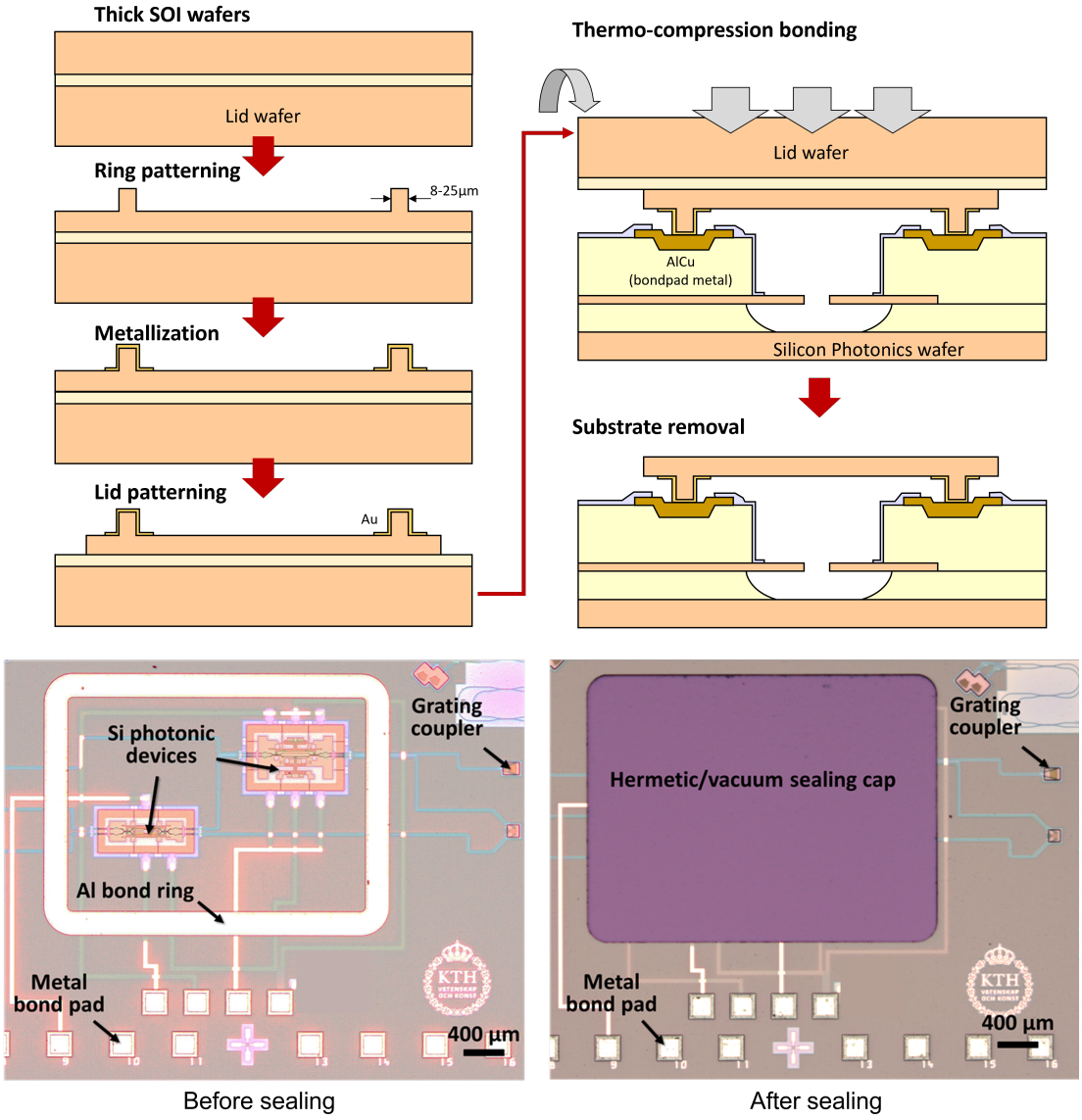

Figure 5. Hermetic sealing of silicon photonic MEMS devices. The lids are processed on a separate SOI wafer, which is then bonded on the silicon photonics wafer. Subsequently the silicon substrate of the lid wafer is etched back. The microscope pictures show an area with several MEMS devices before and after sealing.

3.2 Vibration and Temperature cycling tests

To test the robustness of the MEMS devices, we subjected the sealed silicon photonic chips to vibration and temperature cycling. The devices were attached to a mechanical shaking table and we applied increasing acceleration levels from 1g to 5g along the X, Y and Z axis for 1 hour, according to the IEC 61300-2-1 norm. Between each step, we characterized the optical transmission of the devices to assess whether the vibrations had triggered a collapse of the suspended waveguides, e.g. where the waveguides would stick to the silicon substrate. We observed no adverse effects.

Likewise, we temperature-cycled the chips 12 times between -40°C and 85°C over a time span of 92 hours. Again, the samples were optically characterized and no reduction in transmission was observed.

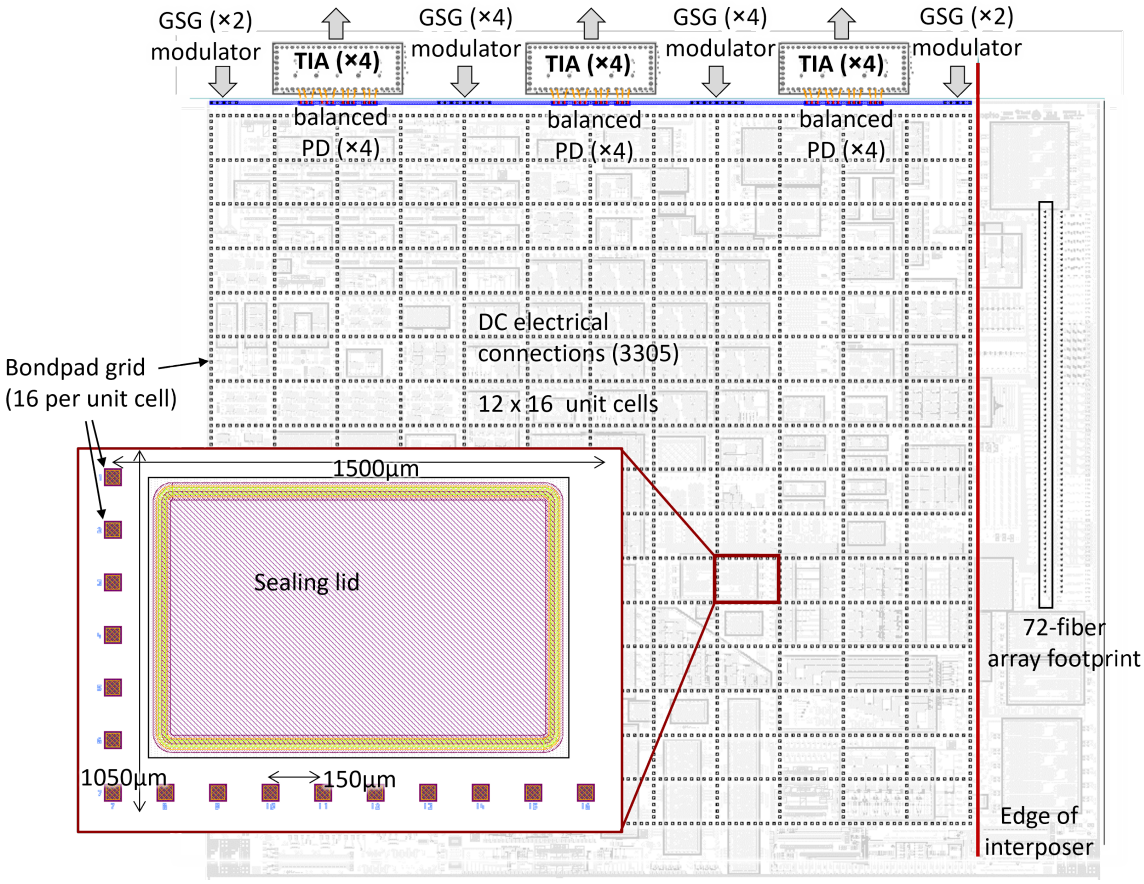

Figure 6. Layout template for a photonic integrated with a large number of electrical input/outputs (up to 3305), 72 fiber ports and 24 high-speed microwave ports (12 inputs, 12 outputs)

3.3 Electrical Packaging

One of the key challenges with the large-scale photonic circuit that we are developing in the MORPHIC project, is the need to electrically address a large number of individual MEMS devices. This translates in a large number of off-chip electrical connections, well beyond the limits of simple wirebonding techniques.

The long-term solution for this problem is to design a bespoke electronics chip that can be flip-chipped onto the photonic chip, with optimized driver and readout circuits. However, this is not an accessible solution when it comes to prototyping new photonic chips, especially since the electronic driving requirements of these new MEMS devices are not fully elaborated. Also, a custom driver solution would need to be redesigned for every chip iteration, which is a costly and time-consuming proposition.

In MORPHIC, we address this packaging challenge a high-density electrical interposer that can be used for multiple design iterations. We first established a set of design rules for the electrical interface of the photonic chip. A grid 12 × 16 unit cells provides a total of 3305 allowed bondpad locations with 150 µm pitch. A photonic circuit does not have to use all these locations, but when it only uses bondpads on these standardized locations, the rest of the packaging flow can be applied.

To break out this dense array of bondpads, a high-density ceramic interposer has been designed. This interposer with 21 layers routes all the bond pads from a footprint of 18 mm × 18 mm to a much wider grid of 98 mm × 68 mm, with a footprint that is compatible with off-the-shelf high-density spring connectors with 200 pins. The interposer, which is fabricated with low-temperature co-fired ceramics, carries a high one-time cost but can then be reused for any chip that adheres to the grid design rules.

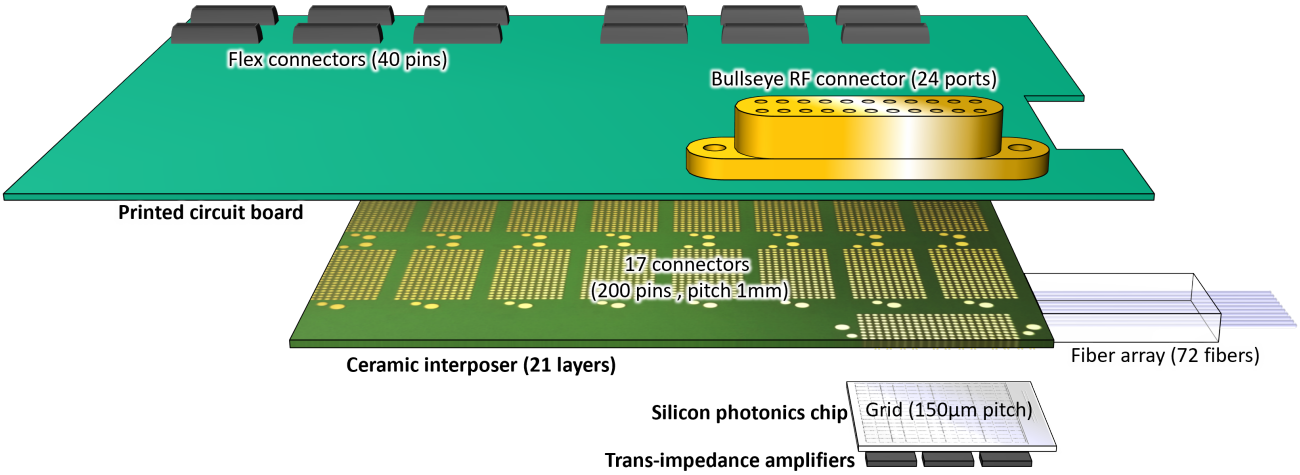

Figure 7. A silicon photonics chip that adheres to the packaging layout of Fig. 6 is flip-chipped onto a 21-layer ceramic interposer that fans out the 3305 DC connections to 17 200-pin connector pads with 1mm spacing. These are compatible for spring connectors or direct soldering onto a printed circuit board. While the interposer breaks out all electrical connections (including the high-speed ports), the printed circuit board selects only those that are effectively used on the silicon photonics chip.

To mount the photonic chip on the interposer we first apply gold stud bumps on the photonic chip. This improves the adhesion and makes sure we can use standard flip-chip processes even with the silicon lids that were used for the hermetic sealing. The corresponding pads on the interposer are populated using solder jetting, after which the two are bonded together using conventional flip-chipping.

The interposer with the photonic chip can then be mounted on a printed circuit board (PCB) which only connects the pins that are actually used by the photonics chip. PCB technology carries a much lower cost and such boards can be fabricated on short notice. Depending on the complexity of the chip (i.e. the number of electrical wires actually used), a multi-layer PCB could be needed.

In MORPHIC, these PCBs only serve as a rerouting board, connecting the interposer to a set of 40-pin flex connectors, which we then use to connect to the electronic drivers for the MEMS and the low-speed readouts of the monitor photodetectors.

3.4 Optical and Microwave packaging

Apart from the many electrical connections to control the many MEMS actuators, the silicon photonic chip also needs optical interfaces and high-speed connections to the modulators and high-speed photodetectors. For the optical inputs and outputs, we rely on single-mode fiber arrays with a standard pitch of 127 µm, going up to 72 fibers. It is possible to define multiple such arrays on the photonic chip, but only one can be connected in a given package. The fiber arrays are all located on a single side of the silicon photonics chip, where it extends over the edge of the ceramic interposer. This scheme is compatible with both edge coupling and vertical grating couplers.[33]

For the high-speed connections we use the same ceramic interposer. The input connections for 12 high-speed modulators are fed directly through the interposer, while for the high-speed photodetectors the interposer can accomodate three chips with 4 optimized trans-impedance amplifiers (TIA)[34] that can boost the output signals before also passing them through the ceramic interposer. On the other side of the interposer, both the high-speed inputs and the amplified outputs can be connected on the PCB using high-density multi-channel microwave connectors.[35]

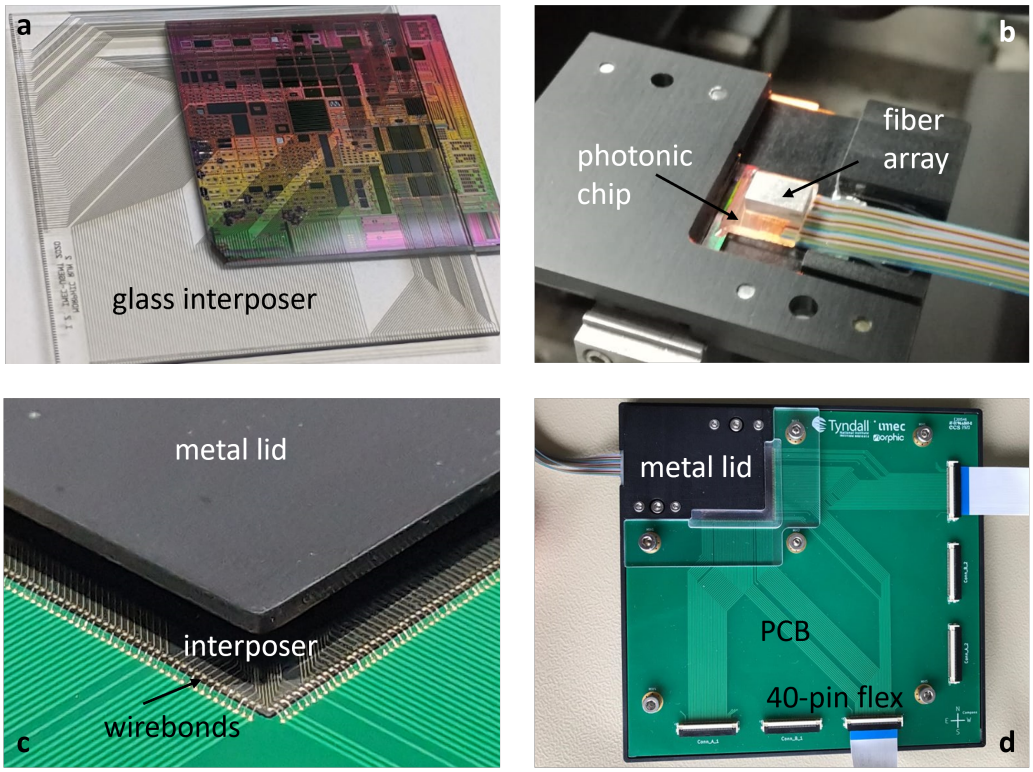

Figure 8. Example of packaging approach for smaller-scale circuits. (a) the photonic chip is moounted on a single-layer interposer (glass or Si). (b) The fiber array is attached. (c) The edge pads of the interposer are wire-bonded to a PCB, (d) The final package encapsulates the photoinc chip assembly in a metal housing.

3.5 Small-scale Photonic-Electronic packages

The large multi-layer ceramic interposer is developed for packaging very large circuits. For smaller-scale test circuits on the same chip, we have simplified the packaging procedure. when the circuit is small enough that the electrical wires can be broken out without the need for multiple interconnect layers, we design a single-layer interposer that is fabricated onto a glass or silicon wafer. The photonic chip is then mounted on this interposer using the same flip-chip process (gold stud bumps and solder balls) used for the larger-scale packaging.

As the interposer only has a single layer, there are no vias to the other side, and the fanout goes towards the edge, where they can be wirebonded to a custom PCB with flex connectors. The various steps are shown in Fig. 8

4. ELECTRONIC CONTROL AND PROGRAMMING

Large-scale photonic circuits need the electronic control, and a software layer that allows the user to configure or finetune the operation of the circuits. This is especially true for more generic programmable photonic circuits such as configurable waveguide meshes, which do not have any inherent functionality until all the tunable couplers and phase shifters are configured.[2] Therefore, in the MORPHIC project we developed the driver electronics and software layers to control large-scale programmable photonic circuits.

4.1 Electronic drivers

With large-scale photonic circuits comes the need for large-scale driver electronics. Again the long-term solution points towards custom drivers chips that can be flip-chipped or 3D stacked on the silicon photonics chips. But

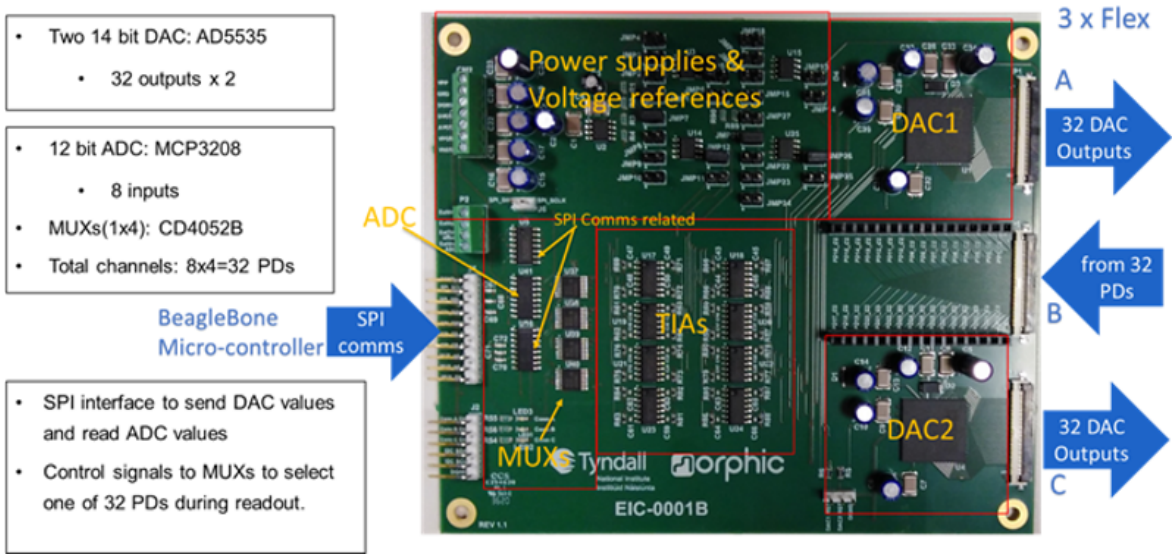

Figure 9. Electronic interface and control board with 64 MEMS driver channels and 32 Photodetector readouts.

during research and development phases of new silicon photonic circuits, a more flexible solution is needed that still allows scaling to 100s or even 1000s of driver and readout channels.

In MORPHIC we built a solution for electronic drivers that complements the packaging scheme describe above. We developed modular *electronic interface and control* boards that provide 64 parallel driver channels and 32 readout channels for low-speed monitor photodetectors. These driver boards connect through 3 40-pin flex cables to the custom PCB of the photonic chip. Each driver board is controlled by its own *BeagleBone* single-board computer, and many driver boards can operate together to control a larger chip. This makes it possible to scale to larger experimental systems, and combine boards with drivers for different voltage and current ranges.

In MORPHIC, we focused on a driver board optimized towards the MEMS actuators. The MEMS require electrostatic driving with voltages up to 50 V. We use two 32-channel DACs (Analog Devices AD5535B) to provide a total of 64 programmable voltages between 0 and 50 V to drive the MEMS with 14-bit accuracy. These driving signals are sent out to the photonic chip through two 40-pin flex connectors.

For the readout, we incorporated 32 TIAs connected to the center flex connector. Analog switches going from 4 inputs to 1 output are used to select 1 TIA out of 4 which is then routed to one of the 8 ADC inputs. The *BeagleBone* provides the digital interface to the DACs and ADCs and the analog switches. The board measures 12 × 14 cm with three flex connectors that interface with the interconnect PCB on the right. On the left side are the power supply pins, TIA and ADC offset voltage pins, and a digital interface with the BeagleBone board.

4.2 Software programming framework

To interface the many electronic control channels to the large photonic circuits, we developed a software framework that allows us to map an abstract description of a photonic circuit to different levels of the implementation. This is illustrated in Fig. 10. From the abstract schematic of a circuit (e.g. a hexagonal waveguide mesh) we can derive the circuit layout on the chip using specific building blocks for the tunable couplers and phase shifters (here they are MEMS based). But at the same time it is also possible to simulate the response of this chip when we set these individual actuators to a specific state.

The software also interfaces with configuration algorithms, and generates a graph representation that can be used by automatic routing algorithms.[36] When connected to the hardware, the framework keeps track of the electrical connections, so it can correctly map an tunable coupler or phase shifter to a specific channel on one of the multiple driver boards.

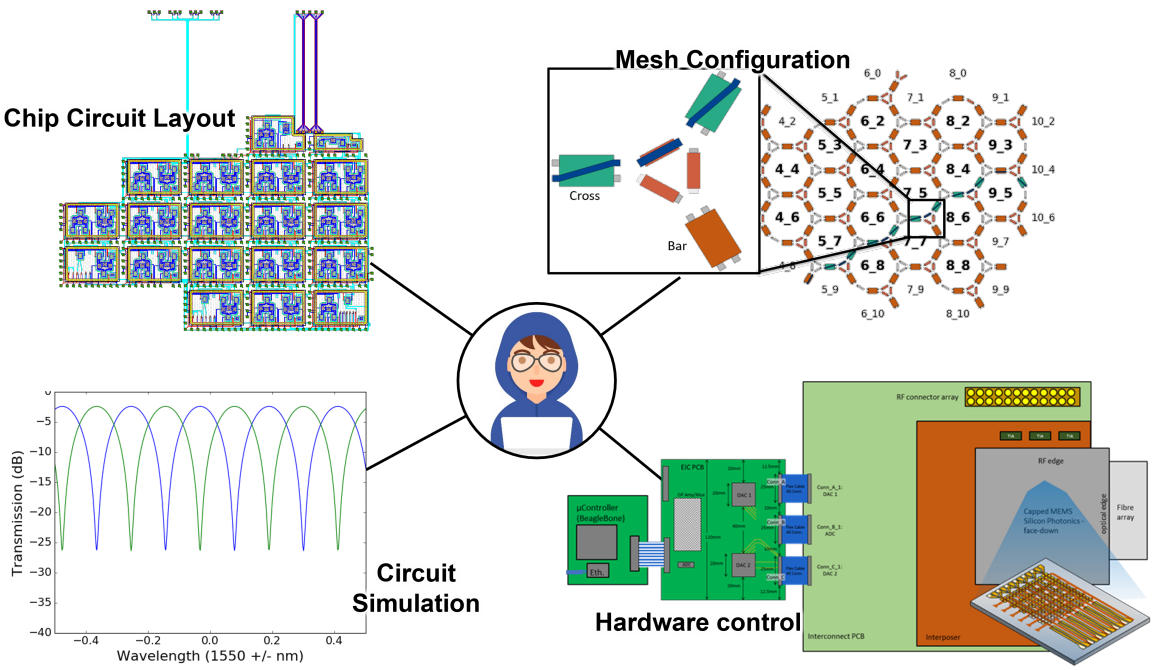

Figure 10. Software layers for controlling complex photonic circuits and programmable waveguide meshes. From a single description of the circuit connectivity or the waveguide mesh, the user can define a chip layout implementation, configure the tunable elements, perform circuit simulations and control the hardware.

Each actuator can also be calibrated so nonidealities in the response curve can already be compensate upfront in the software, reducing the impact of parasitic effects due to non-ideal coupling behaviour and multi-path interference.[37]

5. SUMMARY

This paper presents the current state of the developments in the MORPHIC projects, which has shown significant progress on the side of devices, circuits and packaging technologies since we reported earlier in.[15]

This technology is now being applied in multiple demonstrator circuits, from MEMS-based switch matrices to optical beamforming and microwave photonics. We are also implementing multiple general-purpose programmable circuits to demonstrate the scalability and flexibility of this platform.

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