Micro-Transfer-Printing Technology For Implementing Scalable III-V-on-Si Heterogeneous Integration

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There is a growing interest from industry in silicon photonics with the demonstration of highspeed transceivers and optical sensors on compact, robust, cost-efficiently fabricated silicon-oninsulator (SOI) and SiN-on-insulator chips [1]. However, the functionality of the platform is currently limited as lasers, optical amplifiers and photodetectors other than Ge photodiodes are unavailable on the platform.

To make the platform complete, a scalable III-V-on-Si integration technology is required. We propose micro-transfer-printing (uTP) [2], which is a versatile technology that combines advantages of flip-chip integration (pre-fabrication and pre-testing) and wafer bonding (high throughput integration) and works by releasing the III-V devices from their source substrate, picking arrays of those devices using a structured elastomeric polydimethylsiloxane (PDMS) stamp and printing these on a silicon photonic target wafer with high alignment accuracy (Fig. 1). This way the III-V active devices can be integrated in a low-cost manner and by efficiently using the III-V material.

In this conference we present the development of the uTP technology for silicon photonic integrated circuits and the latest results. We discuss the uTP-enabling III-V processing, parallel printing and demonstrate the technology in a range of applications.



Fig. 1. Principle of micro-transfer-printing of III-V components on a silicon photonic target wafer.

References

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