PHOTONICS Research

Wafer-level hermetically sealed silicon photonic MEMS

Gaehun Jo,[1] Pierre Edinger,[1] Simon J. Bleiker,[1] Xiaojing Wang,[1] Alain Yuji Takabayashi,[2] Hamed Sattari,[2] Niels Quack,[2] Moises Jezzini,[3] Jun Su Lee,[3] Peter Verheyen,[4] Iman Zand,[5] Umar Khan,[5] Wim Bogaerts,[5] Göran Stemme,[1] Kristinn B. Gylfason,[1,6] and Frank Niklaus[1,7]

[1]Division of Micro and Nanosystems, KTH Royal Institute of Technology, 11428 Stockholm, Sweden
[2]École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
[3]Tyndall National Institute, Lee Maltings Complex Dyke Parade, T12 R5CP Cork, Ireland
[4]imec vzw. 3DSIP Department, Si Photonics Group, Kapeldreef 75, 3001 Leuven, Belgium
[5]Department of Information Technology, Photonics Research Group, Ghent University - IMEC, 9052 Gent, Belgium
[6]e-mail: gylfason@kth.se
[7]e-mail: frank@kth.se

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The emerging fields of silicon (Si) photonic micro–electromechanical systems (MEMS) and optomechanics enable a wide range of novel high-performance photonic devices with ultra-low power consumption, such as integrated optical MEMS phase shifters, tunable couplers, switches, and optomechanical resonators. In contrast to conventional SiO_2-clad Si photonics, photonic MEMS and optomechanics have suspended and movable parts that need to be protected from environmental influence and contamination during operation. Wafer-level hermetic sealing can be a cost-efficient solution, but Si photonic MEMS that are hermetically sealed inside cavities with optical and electrical feedthroughs have not been demonstrated to date, to our knowledge. Here, we demonstrate wafer-level vacuum sealing of Si photonic MEMS inside cavities with ultra-thin caps featuring optical and electrical feedthroughs that connect the photonic MEMS on the inside to optical grating couplers and electrical bond pads on the outside. We used Si photonic MEMS devices built on foundry wafers from the iSiPP50G Si photonics platform of IMEC, Belgium. Vacuum confinement inside the sealed cavities was confirmed by an observed increase of the cutoff frequency of the electro-mechanical response of the encapsulated photonic MEMS phase shifters, due to reduction of air damping. The sealing caps are extremely thin, have a small footprint, and are compatible with subsequent flip-chip bonding onto interposers or printed circuit boards. Thus, our approach for sealing of integrated Si photonic MEMS clears a significant hurdle for their application in high-performance Si photonic circuits.

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1. INTRODUCTION

Over the past decade, photonic integrated circuits (PICs) have evolved rapidly. They have already found widespread use in telecommunication systems, where they serve as highly miniaturized optical transceivers, and are being developed for emerging applications in medical technology and sensing [1]. Especially, silicon (Si) photonics has established itself as a scalable technology that is becoming widely available via commercial foundry platforms [2–5]. Si photonics foundries offer a wide range of devices, such as high-speed modulators and photodetectors, as well as high-quality passive waveguides. Moreover, the availability of Si photonics has catalyzed new research fields that leverage the excellent mechanical properties of Si in combination with its large refractive index. For example, integrated optical sensors based on suspended Si waveguides achieve high sensitivity, due to the high Si–air refractive index contrast that allows for high mode deconfinement [6–9]. Furthermore, optomechanical coupling and optical forces can be harnessed, for uses such as particle manipulation, telecommunication, or on-chip nonreciprocal transmission [10–12]. Movable and tunable Si photonic micro–electromechanical (MEMS) components also show promise as low-power and compact reconfigurable photonic building blocks for large scale programmable photonic circuits that can be reprogrammed for a variety of optical functions [13–19], i.e., generic field-programmable PICs (FP-PICs), similar to FP gate arrays (FPGAs) in electronics. In contrast to conventional SiO_2-clad photonic devices, optomechanical and Si photonic MEMS devices feature suspended and movable parts, and exposed waveguide cores. These devices are much more susceptible

to environmental influences such as exposure to dust, gas composition, and humidity levels, and, therefore, require a robust packaging solution to ensure reliable operation over extended time periods. Hermetic sealing in inert gas or vacuum, protecting the photonic MEMS from such environmental influence, is crucial for their reliable performance, and serves as a prerequisite for their commercialization [20–22].

There exist mature wafer-level hermetic packaging solutions for traditional MEMS components that have been reported and successfully employed in the industry [23–27]. These approaches offer long-term hermeticity, and some of them include electrical feedthroughs, which are electrical connections from the MEMS device inside the sealed cavity to the outside. However, none of the traditional MEMS packaging approaches offers optical feedthroughs, which are essential for photonic devices. To the best of our knowledge, wafer-level hermetic sealing of integrated photonic MEMS devices, with incorporated electrical and optical feedthroughs, has not yet been demonstrated. Thus, there is a clear need for a cost-effective hermetic packaging technology that is fully compatible with standard PIC foundry platforms and does not block the optical interfaces of the Si photonics chip [28–33].

In this work, we demonstrate an approach for wafer-level hermetic sealing of Si photonic MEMS inside cavities with electrical and optical feedthroughs. We validate the feasibility of our approach by sealing Si photonic MEMS devices on foundry wafers from the iSiPP50G Si photonics platform of IMEC, Belgium [34,35]. Our sealing approach uses low-temperature (250°C) Au-Al thermo-compression wafer bonding that is fully compatible with the Si photonic foundry wafers [26]. We demonstrate sealing of a total of 672 individual cavities with caps that are 25 μm thick and of varying dimensions (from 0.45 mm × 0.33 mm to 2.80 mm × 2.95 mm), achieving a vacuum sealing yield of 90%. We experimentally verify the functionality of the sealed photonic MEMS devices and the optical and electrical feedthroughs, and we demonstrate that the vacuum encapsulated photonic devices feature higher mechanical quality factors (Q) and increased mechanical cutoff frequencies, due to the elimination of air damping.

2. VACUUM SEALING OF SI PHOTONIC MEMS

Our approach to vacuum sealing of Si photonic MEMS on PIC wafers consists of metal-to-metal bonding of thin Si caps on top of cavities containing the suspended Si photonic MEMS, as illustrated in Fig. 1(a), which shows a cut-away 3D illustration of a single sealed cavity. This vacuum sealing approach is fully compatible with standard Si photonic foundry wafers and their standard metallization layers. In all our experiments, we used 100 mm diameter wafers, for compatibility with our processing tools. The Si-on-insulator (SOI) based PIC wafers were downsized from 200 mm diameter foundry wafers from the iSiPP50G Si photonics platform of IMEC, Belgium [3,34,36]. The iSiPP50G platform provides an extensive component library, including state-of-the-art optoelectronic modulators and detectors, grating couplers, and a two-level copper-damascene metal interconnect stack with Al/Cu metal bond pads for the back-end electrical connections. To provide access to the photonic MEMS devices, the back-end-of-line (BEOL) oxide stack is locally etched to create open cavities. We then post-processed these cavities using vapor hydrofluoric acid (HF) etching to create suspended waveguides and movable MEMS devices, as illustrated in Fig. 1(a). To hermetically encapsulate these devices inside the cavities, we prepared 25 μm thick Si sealing caps on a separate 100 mm diameter SOI wafer, using contact lithography, dry etching, and metal deposition [Fig. 1(b), panels i–iii]. The resulting Si sealing caps on the SOI wafer consist of a flat lid section with a 20 μm wide protruding sealing ring covered by a 2 μm thick gold layer [Figs. 1(a) and 1(b) panel iii]. On the photonic device wafer, corresponding aluminum/copper (Al/Cu) metal rings [orange rings in Fig. 1(a)] were defined in the standard metal bond pad layer of the iSiPP50G process [orange pads in Fig. 1(a)]. The sealing of the cavities on the photonic wafer was performed in vacuum using a commercial wafer bonder. In this step, the Au-covered sealing rings on the cap wafer were bonded to the Al/Cu metal rings on the photonic device wafer [Fig. 1(b), panels iv and v] using thermo-compression bonding with a bond pressure of 400 MPa and a bonding temperature of 250°C for 45 min. After the bonding, we removed the handle layer of the cap wafer by deep reactive ion etching (DRIE), leaving only the 25 μm thick Si caps on top of the cavities containing the photonic devices [Figs. 1(b) panel vi and 1(a)]. A detailed description of the wafer preparation, bonding, and cap transfer process is presented in the Experiment section. Using this sealing approach, we successfully sealed Si photonic devices on wafer level as shown in Fig. 1(c), where the sealing caps are visible in a dark green color against the bright background of the iSiPP50G device wafer. A comparison of Si photonic MEMS devices before and after sealing is shown in Fig. 1(d). In the left microscope image, the suspended Si photonic MEMS devices are visible, as well as the Al/Cu metal ring around the cavity, while the right image shows the same devices encapsulated by a Si sealing cap. The image on the right shows the bond pads and grating couplers that are standard design part of the iSiPP50G platform and that connect to the electrical and optical feedthroughs, which are buried in the BEOL oxide stack [36,37]. These feedthroughs are designed using the foundry metallization layers, and are placed underneath the metal rings, thus connecting the electrical and optical input/output (I/O) to the vacuum sealed photonic MEMS devices inside the cavity [Fig. 1(a)]. Hence, the photonic devices can be easily addressed optically and electrically and characterized even after they have been sealed. Close-ups of the bond pads and grating couplers around the sealing caps are shown in the SEM images in Fig. 1(e), which also illustrate the thinness of the 25 μm thick sealing caps, and the fact that both optical and electrical interfaces remain accessible.

3. OPTICAL AND ELECTRICAL CHARACTERIZATION OF SEALED PHOTONIC DEVICES

Essential requirements on PICs containing vacuum packaged photonic MEMS devices are functional optical and electrical feedthroughs that provide connections between the photonic MEMS inside the packages and the outside world, as well as maintaining the mechanical integrity of the photonic MEMS devices during and after the sealing process. In our ap-

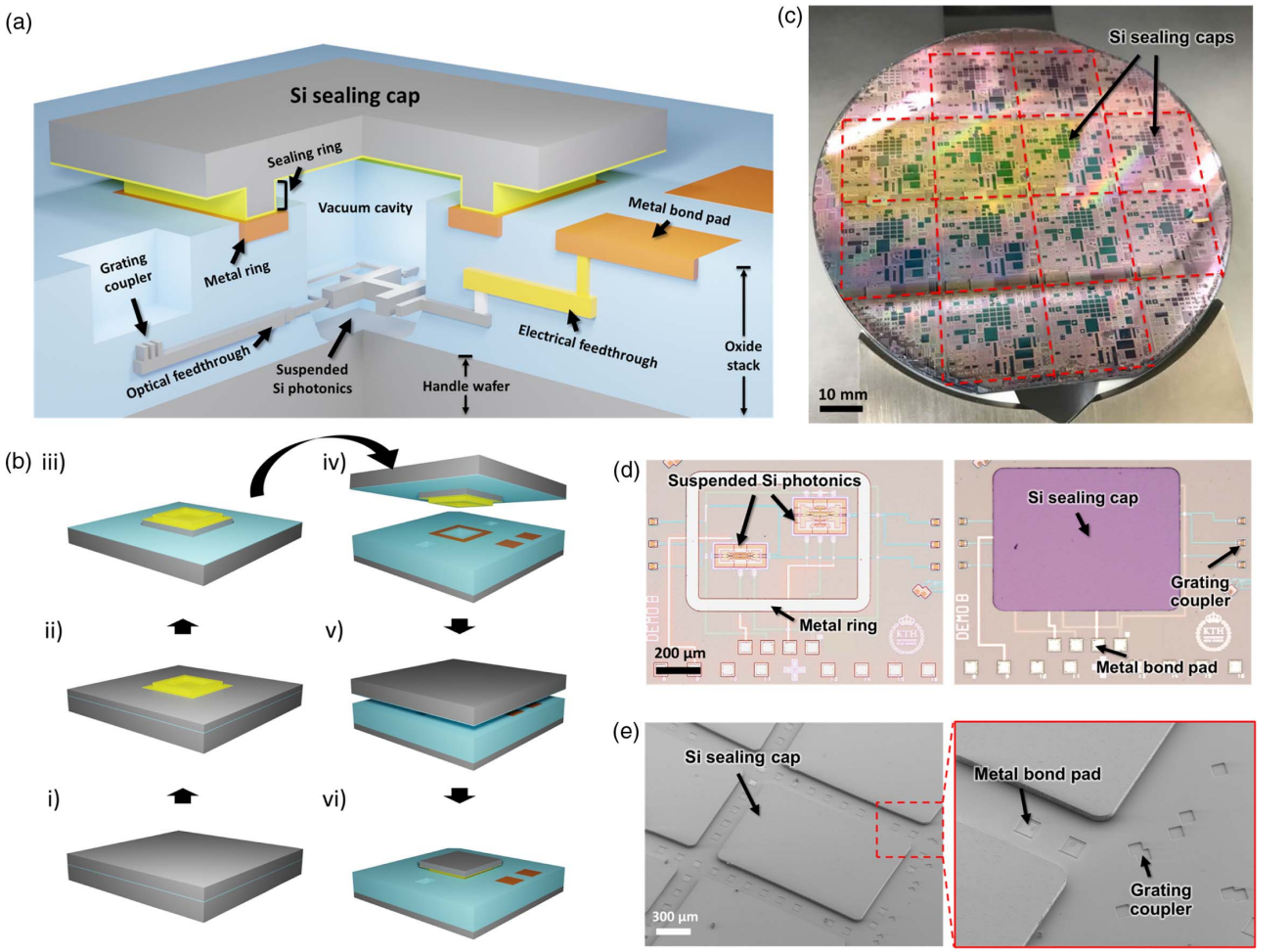

Fig. 1. Wafer-level hermetic packaging of Si photonic MEMS. (a) Cut-away 3D illustration of a hermetically sealed suspended photonic MEMS device. (b) Process flow of the hermetic packaging approach by transfer bonding of a Si sealing cap: steps (i), (ii) patterning of sealing rings by deep reactive ion etching (DRIE) on the SOI cap wafer, followed by TiW/Au deposition and etching; (iii) etching of the sealing caps; (iv), (v) wafer alignment of the SOI wafer containing the caps and photonic device wafer, and bonding of the wafers inside a vacuum chamber at 250°C; (vi) removal of the Si handle (substrate) layer of the SOI cap wafer by DRIE such that only the thin vacuum sealing caps remain on the photonic device wafer. (c) Photograph of a full wafer with sealed Si photonic MEMS. (d) Microscope images before sealing (left) and after sealing (right). (e) SEM images of the bond pads and grating couplers around the thin sealing caps.

proach, the optical and electrical feedthroughs travel underneath the metal rings of the photonic device wafer, buried within the BEOL dielectric layers that are part of the photonics foundry platform, thereby ensuring the hermeticity of the package. We evaluated optical feedthroughs that were connected to four different types of sealed Mach–Zehnder interferometers (MZIs) [split image in Fig. 2(a)]. The optical feedthroughs used here were standard iSiPP50G strip waveguides with 450 nm width and 220 nm thickness that were buried in the BEOL oxide layer. We optically interfaced all four MZI devices with grating couplers, thereby enabling connection to an external optical-fiber-coupled light source and detector. We measured the optical transmission of the devices across all 12 dies on the sealed 100 mm wafer using wavelengths from 1500 to 1580 nm. We found that the maximum transmission follows the reference envelope, without any noticeable impact of the sealing on the optical performance of the waveguides passing below the metal rings [Fig. 2(b)]. Furthermore, we assessed the impact of the sealing process on the suspended photonic structures inside the cavities, by comparing the characteristics of the four MZI devices in the cavity. All four MZI devices use a similar test circuit that differs only in the short, suspended waveguide section present in one arm of the interferometer. The suspended waveguide sections differ in length and stiffness, where device A has the most robust design (shorter and straight), and device B the least robust one (longer, multiple anchors and bends). We extracted the extinction ratio (ER) of all devices across the 12 dies on the wafer, as indicated in Fig. 2(c). If a suspended waveguide section collapses, the optical losses increase drastically as the light leaks into the Si substrate. As a result, the transmission spectrum of the corresponding interferometer has an ER of zero. Devices of types A, C, and D all display interference fringes, except for a single die on the edge of the wafer (in total 33 suspended devices out

of 36). The waveguide sections in those devices did not collapse, and this confirms that our sealing method is compatible with suspended photonic devices. Measurements of device type B showed a higher collapse count (in total 7 suspended devices out of 12), which may be because device type B has the least robust mechanical design. The most fragile suspended devices tend to collapse due to very low out-of-plane stiffness and stiction during the vapor-HF release step, and it is likely that these devices were already collapsed before the sealing. Overall, the sealing did not lead to a systematic collapse of suspended waveguide sections, which is a key requirement for a viable process for sealing of photonic MEMS devices.

Next, we evaluated the impact of vacuum sealing on the performance of a Si photonic MEMS phase shifter. To read out the phase shift as a function of actuation voltage, the phase shifter is included in one arm of an MZI [Fig. 3(a)]. It corresponds to device D in Fig. 2(a). The phase shifter consists of a fixed suspended waveguide near a slender movable Si beam. The Si beam is attached to an in-plane MEMS comb-drive actuator, and when a bias voltage is applied between the movable and fixed electrodes, the effective index of the guided mode in the suspended waveguide is decreased as the narrow Si beam is moved away from it [18]. The change in effective index in the suspended waveguide translates into a phase shift, which we

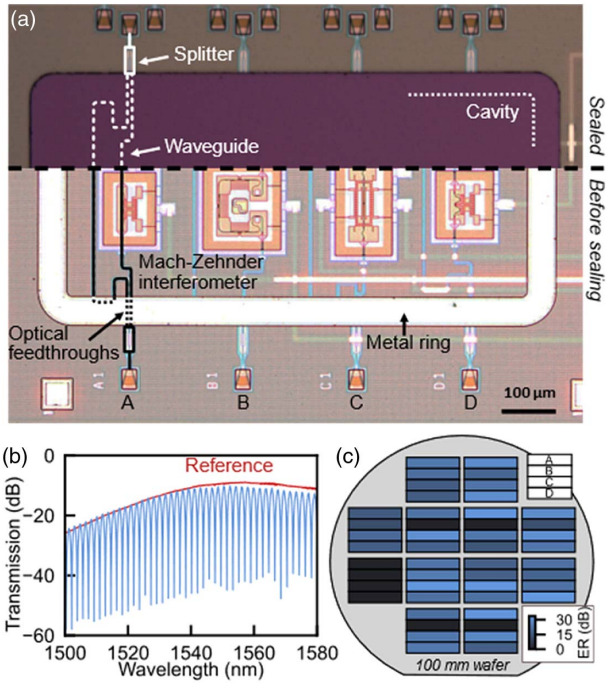

Fig. 2. Optical characterization of sealed Mach–Zehnder interferometers (MZIs) with suspended waveguide sections in one arm. (a) Split view of optical microscope images of four MZI devices before and after sealing within a rectangular cavity. (b) Example of measured optical transmission spectrum, along with the transmission spectrum of a reference grating-to-grating structure outside the sealed cavity. (c) Wafer map of the extinction ratio (ER) at a wavelength of 1550 nm of MZI devices placed on dies across the 100 mm wafer. An ER of 0 dB corresponds to collapsed waveguide sections. Four devices were measured on each die.

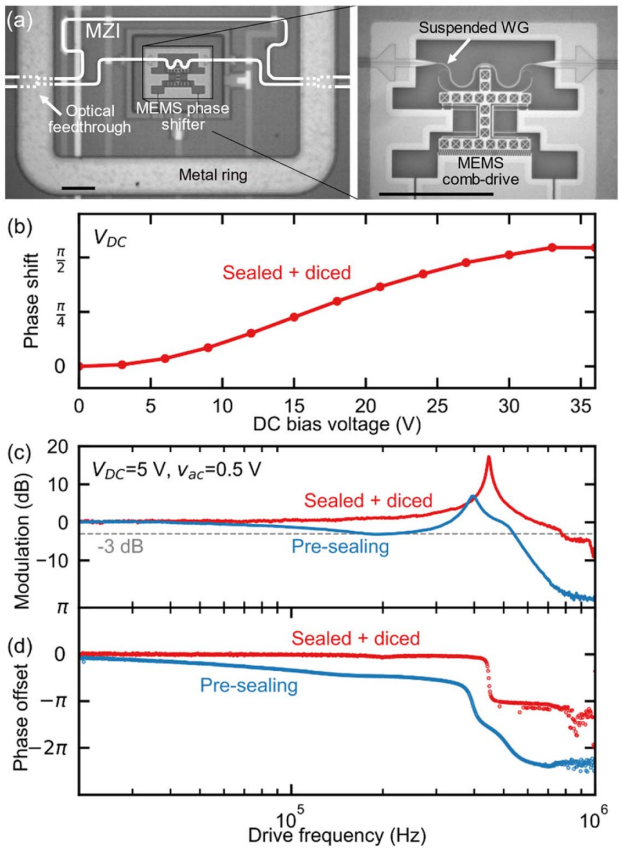

Fig. 3. Effect of vacuum sealing on the performance of a Si photonic MEMS phase shifter. (a) Optical microscope image of the phase shifter before sealing. Inset: close-up of the suspended waveguide and movable actuator. (b) Phase shifter response in DC up to 36 V at a wavelength of 1550 nm, after sealing and dicing. (c), (d) Mechanical frequency response of the device before and after sealing, with (c) modulated output from the on-chip Mach–Zehnder interferometer and (d) mechanical phase offset with respect to the driving signal.

measured after sealing and dicing [Fig. 3(b)]. The phase shifter worked as intended after sealing (and dicing), and achieved a $\pi/2$ phase shift at 36 V DC actuation, which is consistent with the device design. We also measured the mechanical frequency response of the phase shifter using a lock-in amplifier, and compared the result before and after sealing [Figs. 3(c) and 3(d)]. We applied a DC bias of 5 V to the actuator, with an AC modulation amplitude of 0.5 V. The oscillating phase shift results in a modulation of the MZI output amplitude, which was measured with the lock-in amplifier. We observed a resonance in both cases (396 kHz and 446 kHz, before and after sealing, respectively). Interestingly, the mechanical Q of the device improved significantly after sealing, from 8 to 36. Moreover, the amplitude response after sealing was flatter up to the resonance, with a −3 dB cutoff frequency increasing from 213 to 776 kHz. We attribute these improvements to a reduction of air damping when the devices operate in vacuum inside the sealed cavity. On-chip vacuum packaging has potential applications for faster photonic MEMS actuators and more sensitive optomechanical devices.

4. CHARACTERIZATION OF VACUUM SEALING CAPS

For a wafer-level hermetic sealing process to be viable in practical applications, it must offer acceptable yield. We define here the wafer-scale bonding yield as the fraction of sealing caps that are successfully transferred and bonded to the photonic device wafer and that seal the cavity without detectable gross leakage. We investigated both the yield of our process and the hermeticity of the sealed cavities, by measuring the deflection of the thin Si caps using an optical profilometer to verify the presence of a vacuum inside the cavity. If a cavity is hermetically sealed, the cap deflects to the inside of the cavity, due to the difference in pressure between the vacuum inside the cavity and the outside atmosphere, as exemplified in the deflection measurement in Fig. 4. While the cap deflection does not provide an accurate measurement of the vacuum level for low gas pressure, we estimated the vacuum pressure inside the sealed cavities to be of the order of a few mbar, based on the results from previous residual gas analysis measurements performed on test cavities that were sealed with the same approach [26]. To estimate the yield and reliability of our sealing process, we characterized a total of 128 sealed cavities distributed across four dies of a sealed Si photonic foundry wafer (all cavities had a side length of 600 μm or larger). To account for processing variations across the wafer, we selected two dies located at the center and two dies located at the edge of the wafer for this evaluation. We found that of the 128 cavities, 115 were successfully sealed directly after the sealing process, which corresponds to a sealing yield of about 90%. To investigate possible gross leakage of the sealed cavities, we repeated the cap deflection measurements after storing the sealed wafer for 21 days in ambient atmosphere. We did not observe a measurable change of the cap deflection in any of the cavities (within the ±60 nm accuracy of our measurement approach), indicating that there was no gross leak in any of the 115 successfully sealed cavities. In contrast, 13 leaked cavities clearly show flat without deflection, indicating no pressure difference inside or outside the cavities. We also evaluated the robustness and process compatibility of the sealed cavities using standard wafer dicing to cut the wafer into separate dies, which is a critically important step in component manufacturing. Therefore, we diced the wafer with the sealed cavities into 12 dies. Again, we found no difference in cap deflection in any of the 115 sealed cavities after dicing, demonstrating the robustness and resilience of the sealed cavities to standard wafer dicing.

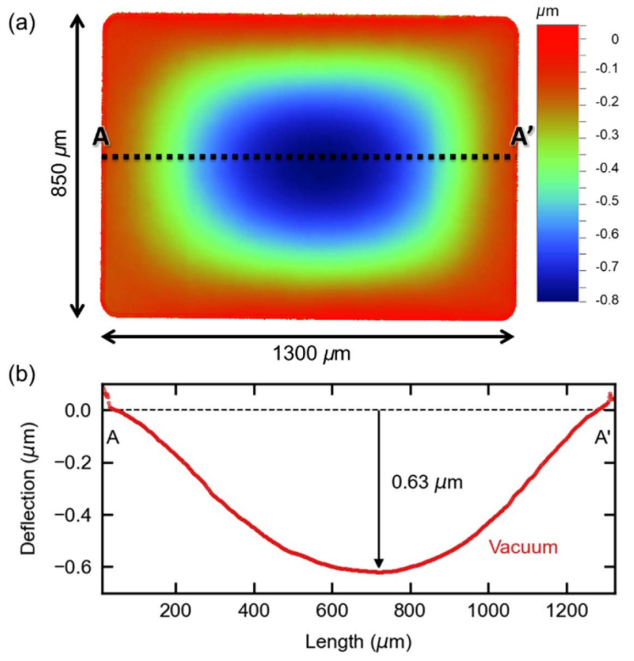

Fig. 4. White-light interferometry measurement of the deflection of a Si sealing cap. (a) Top view heatmap showing the deflection of a 25 μm thick Si cap with an area of 850 μm × 1300 μm, resulting from the pressure difference between the inside and outside of the sealed cavity. (b) A cross section of (a) shows a maximum cap deflection of 0.63 μm at the center of the Si cap.

5. COMPATIBILITY WITH HIGH-DENSITY CHIP INTEGRATION

Due to the ultra-thin caps and the compact footprint, our vacuum sealing approach is exceptionally well suited for high-density photonic system integration. Reducing the overall device volume facilitates a higher integration density and thus smaller and more powerful PIC-based components. First, an important contributing factor to the small footprint that we can achieve with our sealing approach is the narrow sealing rings that we employ in the caps. The total width of the sealing rings in this work is only 20 μm, thereby enabling a high integration density that reduces costs and improves performance due to shorter optical and electrical signal paths. The narrow sealing rings also provide the benefit of great flexibility in the sealing cap design. The caps can be designed to seal not only one device in a single cavity, but multiple devices in one or several cavities using one single cap [Figs. 1(d) and 2(a)]. This flexibility also allows for different shapes of sealing caps to be manufactured in the same process. Possible shapes include square, rectangular [Figs. 1(d) and 2(a)], triangular, and L-shaped, and can even include open regions for additional routing options. As a demonstration of the latter, we designed a donut-shaped cap where a second inner metal ring is used to ensure hermeticity, which allows for electrical probing through the opening in the center of the sealing cap, as shown in Fig. 5. To verify the electrical integrity of these feedthroughs, we included eight different metal wires featuring varying lengths, widths, and numbers of sealing ring transitions. We measured resistances between 5 and 50 Ω for all eight electrical feedthrough designs both before and after the sealing process, with no observable difference in resistance to that of identical metal lines in reference devices without sealing caps. The measured resistance values comply with the related specifications of the iSiPP50G platform.

Additionally, as the sealing caps in our approach are thinner (25 μm thick, including the protruding sealing rings) than the height of typical flip-chip Au/solder bumps (about 50 μm), the caps fit neatly between the bumps and, thus, enable face-to-face flip-chip bonding with high I/O counts of the packaged photonic devices, as illustrated in Fig. 6(a). To demonstrate the vertical chip integration capability of our packaged Si photonic

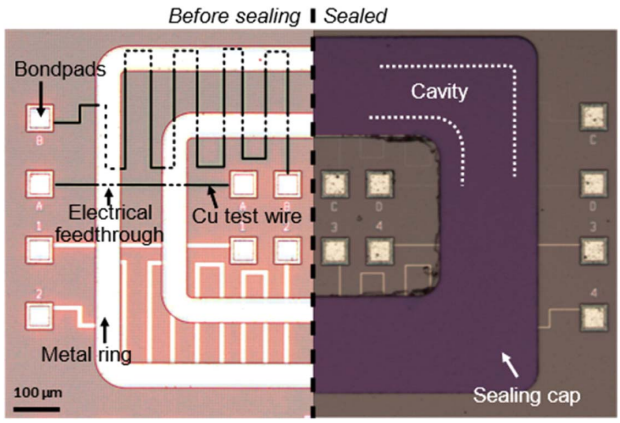

Fig. 5. Donut-shaped sealed cavity with eight different electrical feedthrough test structures. The feedthroughs pass below the metal rings and connect a bond pad outside the cap with a bond pad in the center of the donut. Left: optical microscope image before sealing. Right: after sealing.

devices, we flip-chip bonded a chip containing hermetically sealed photonic MEMS phase shifters to a glass interposer using gold stud bumping. The interface between the glass interposer and the photonic chip consisted of 599 gold stud bumps (219 functional electrical connections and 380 mechanical bumps) that were bonded to predefined bond pads (50 µm × 50 µm) on the photonic chip. We did not observe any defects in the flip-chip bonded photonic chip when visually inspecting it through the glass interposer [Figs. 6(b) and 6(c)]. These results demonstrate that the sealed photonic devices with thin sealing caps can be placed in between the Au/solder bumps [Fig. 6(c)], thus indicating that our photonic device packaging approach is compatible with large-scale flip-chip integration of photonic chips, featuring a high number of I/O connections to the sealed photonic devices in a small footprint.

6. CONCLUSION

We have presented the first wafer-level hermetic sealing solution for Si photonic MEMS that is compatible with Si photonic foundry wafers and offers ultra-thin wafer-level packages featuring optical and electrical feedthroughs. Our sealing process employs Au-to-Al thermo-compression wafer bonding at a temperature of 250°C, which is fully compatible with standard integrated circuit (IC) and photonic foundry wafers. We have demonstrated hermetic sealing of Si photonic MEMS on a photonics foundry wafer from IMEC (iSiPP50G Si photonics platform), with a sealing yield of approximately 90%. We demonstrated functional optical and electrical feedthroughs that connect to photonic devices inside sealed cavities. Moreover, we showed improved mechanical response of a photonic MEMS phase shifter that was packaged in a vacuum. The photonic packages presented here display a small and flexible footprint and offer full compatibility with subsequent flip-chip bonding with large I/O counts for high-density packaging of photonic circuits. We believe that our wafer-level hermetic sealing approach is a very promising and versatile solution for novel integrated photonics applications, such as low-power photonic MEMS-based circuits and on-chip integrated optomechanics.

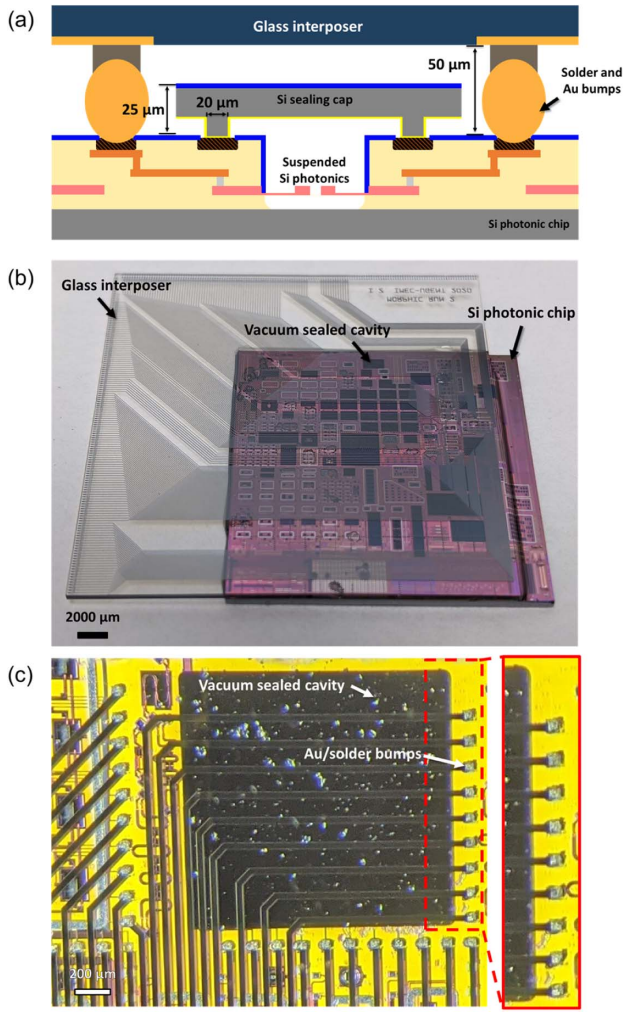

Fig. 6. Demonstration of flip-chip bonding of a chip with sealed photonic devices to a glass interposer. (a) Schematic cross section of a packaged Si photonic chip that is flip-chip bonded to a glass interposer. (b) Photograph of a packaged Si photonic chip that is flip-chip bonded to a glass interposer. (c) Photograph of the caps on top of the vacuum sealed cavities and Au/solder bumps that are visible through the glass interposer.

7. EXPERIMENT

A. Device Wafer Fabrication

The device wafer was fabricated in the standard iSiPP50G Si photonic foundry platform of IMEC, Belgium. This technology platform offers a vast range of active and passive components, such as high-speed optoelectronic modulators and photodetectors as well as high-quality passive waveguides. After receiving the processed Si photonic wafers from the foundry, they were downsized from a diameter of 200 mm down to a diameter of 100 mm, for compatibility with our 100 mm diameter fabrication tools. To create suspended photonic devices, an additional post-processing step was employed on the foundry wafers. Therefore, a hydrofluoric acid vapor-HF etching step was used to selectively remove the oxide underneath the Si waveguide and device layer, thereby realizing suspended Si

photonic devices [13,35]. During this step, a thin alumina (AlO_x) layer was used to protect the areas of the Si waveguide and device layer that were not to be under-etched [18].

B. Cap Wafer Fabrication

A 100 mm diameter SOI wafer with a 25 μm thick Si device layer, a 1 μm thick buried SiO_2 (BOX) layer, and a 300 μm thick Si handle layer was used as a donor wafer for the caps. Si sealing caps with dimensions ranging from 450 μm × 330 μm up to 2812 μm × 2945 μm were designed. First, the 5 μm high and 20 μm wide sealing rings were formed on the device layer by photolithography and Si DRIE. Then, 100 nm thick TiW and 2.1 μm thick Au layers were sputter deposited on the caps and the sealing rings. Thereafter, the Au and TiW layers were selectively etched in I_2/KI and $NH_3 \cdot H_2O/H_2O_2$ solutions using a photoresist mask. Finally, the 25 μm thick caps with the protruding sealing rings were defined by DRIE.

C. Cap Wafer Bonding and Transfer of Caps

The SOI wafer containing the caps was bonded to the Si photonic foundry wafer containing the photonic MEMS devices using Al-Au thermo-compression bonding. Therefore, the two wafers were aligned and clamped together on a bond fixture using a bond aligner tool (Suss BA8, Suss MicroTec AG, Germany), and transferred to a wafer bonder (Suss CB8, Suss MicroTec AG, Germany). First, the chamber of the bonder was evacuated to a pressure of $<7 \times 10^{-5}$ mbar, and the wafers were then held in the vacuum at a temperature of 50°C for 60 min. The purpose of this holding step before the wafer bonding is to release parts of the gas molecules that are absorbed in the wafer surfaces, thereby reducing the resulting gas pressure inside the sealed cavities. The use of longer degassing steps and higher degassing temperatures may further improve the resulting vacuum level inside the sealed cavities. Next, the wafers were joined inside the bond chamber, and the bond chuck was used to apply a bonding force of 28 kN to the wafer stack. For the total area of all the sealing rings present on the 100 mm diameter wafers of 4.85 mm^2, this resulted in a bond pressure at the bond interfaces of approximately 400 MPa. While applying the bond force, the temperatures of the top and bottom bond chucks were ramped to 250°C using ramping times of 45 min (up) and 45 min (down), respectively, and a holding time of 45 min. After the chuck temperature reached 50°C, the bond force was released and the bonded wafer stack was unloaded from the bond chamber. Finally, the Si handle layer of the SOI cap wafer was removed by DRIE, leaving the singulated Si caps bonded on top of the Si photonic device wafer and encapsulating a vacuum inside the sealed cavities.

D. Optical and Electrical Measurements

The device transmissions, as indicated in Fig. 2, were measured using a tunable laser source and wavelength domain component analyzers from Agilent (81680A, 86082A). On each chip of the 100 mm diameter wafer with the sealed photonic devices, four sealed MZIs and a non-sealed reference waveguide were characterized. We used process design kit (PDK) building blocks for all passive components in the circuit: grating coupler FGCCTE_FCWFC1DC_630_378, waveguide SWGCTE_WG_450, and multi-mode interferometer M12CTE_FC_5000_25400. For all passive measurements, we used a power of 50 μW, and the entire wavelength range of the tunable laser source, 1460 to 1580 nm. For the phase shifter response measurement [Fig. 3(b)], we added a DC supply to the setup (Keithley, 2200-72-1). The frequency response of the MEMS phase shifter presented in Figs. 3(c) and 3(d) was obtained using a lock-in amplifier from Zurich Instruments (HF2LI). In that case, the tunable laser source was set to 1550 nm, with a power of 4 mW. An external detector (Thorlabs, DET01CFC) was used for measuring the output, directly connected to the lock-in amplifier. For both passive and active measurements, we optimized the input polarization using a polarization controller from Thorlabs (FPC031). The DC and AC measurements were performed on different copies of the device shown in Fig. 3(a), each copy being on a different die.

E. Characterization of Sealing Yield

The sealing yield is defined here as the fraction of all cavities that were successfully sealed with a cap and that contained vacuum inside the cavity. Successful bonding of the caps was evaluated by optical inspection, and the presence of a vacuum inside the sealed cavities was verified by measuring the deflection of the thin caps to the inside of the cavity using white-light interferometry (Wyko NT9300, Veeco Inc., U.S.). The deflection measurements were repeated after storing the packages for 21 days in ambient atmosphere. Evaluating the cavity sealing by deflection measurements is feasible for caps that are 600 μm × 600 μm or larger in size. For smaller caps, the force exerted by the pressure difference is too small to result in a deflection that provides a reliable measurement of the sealed vacuum. Thus, deflection measurements could not be used to characterize the hermeticity of the smaller packages. Since we observed improvements of the mechanical Q of sealed photonic MEMS devices inside these small cavities due to the elimination of air damping, it is likely that most of the small cavities on our wafer were successfully vacuum sealed. For evaluating whether the packages with the Si photonic devices can survive dicing, the 100 mm diameter wafer with sealed cavities was diced into individual chips using a standard dicing saw (DAD 320, Disco Corp., Japan).

F. Glass Interposer Fabrication

Fabrication of the interposers begins with sputtering of a Cr-Au-Ti stack, with respective thicknesses of 15 nm, 150 nm, and 10 nm, on a 100 mm float-glass substrate. A direct-laser writing lithography step and subsequent ion beam etch (IBE) pattern the metal traces and contact/bond pads. Next, the whole wafer is covered with a 400 nm thick sputtered oxide, and openings over the contact/bond pads are created by another lithography step and a wet etch with buffered hydrofluoric acid (BHF) and 1% HF. The final step is to dice the wafer into individual interposers.

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