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High-efficiency dual single layer graphene modulator integrated on slot waveguides

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Abstract: This paper presents an experimental and theoretical investigation of a graphene-integrated electro-absorption modulator (EAM) based on a slot waveguide. Due to the enhanced light-matter interaction of graphene, the device exhibits an impressive modulation efficiency (0.038 $dB\mu m^{-1}V^{-1}$) and bandwidth ($\approx$ 16 GHz). Starting from these results, we carried out an extensive design study, focusing on three crucial design parameters and exploring the associated trade-offs in insertion loss, extinction ratio and bandwidth. The simulation results offer valuable insights into the influence of each design parameter, reaffirming that our slot waveguide platform holds great promise for realizing a high-performance EAM balancing optical and electrical performance. It is important to note that the slot waveguide was defined through standard deep ultraviolet (DUV) lithography, allowing seamless integration into high-density systems.

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1. Introduction

Electro-optical (EO) modulators are core components in high-capacity optical communication and high-performance computing systems [1–3]. An ideal EO modulator should possess several key characteristics, including a large extinction ratio (ER), a low insertion loss (IL), high speed, and low power consumption. Preferably the device also exhibits a compact footprint and a low driving voltage, compatible with CMOS (complementary metal-oxide-semiconductor) circuitry [4]. In addition, modulators used in high-integration density systems need to demonstrate reliability, reproducibility, and compatibility with existing CMOS manufacturing techniques. It is challenging to meet all these criteria simultaneously using pure silicon-based modulators relying on the relatively weak plasma dispersion effect [5]. Mach-Zehnder modulators based on this effect suffer from large footprints, while ring resonators have limited optical bandwidth and high sensitivity to temperature [6–10]. To overcome these limitations, the integration of non-silicon materials such as germanium [11–13], III-V semiconductors [14], polymers [15,16], and 2D materials [17–23] with silicon platforms has been intensively studied in recent years.

Among these various approaches, graphene has attracted a lot of attention due to its exceptional electrical and optical characteristics [17,24–26]. Graphene-based electro-absorption modulators (EAMs) are particularly promising alternatives to silicon modulators, given the material's broadband and tunable light absorption [27,28], as well as its inherent ultra-high mobility [29,30]. In the past decade, graphene-based EAMs have demonstrated several desirable advantages over

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pure silicon modulators. These include a broadband optical bandwidth exceeding 180 nm [19], an excellent temperature tolerance of over 30° C [18], over 40 Gbps high-speed operation capability [20–22], a low power consumption of approximately 112 fJ/bit [20], and compatibility with wafer-scale fabrication using existing CMOS infrastructure [23]. Notably, high-speed and high modulation efficiency could be achieved simultaneously by optimizing the gate oxide to preserve the intrinsic graphene quality [22]. This optimization helps to eliminate the typical trade-offs encountered in the capacitive structures used for graphene-based EAMs [18,22]. In recent years, the dual single-layer graphene (DLG) structure has gained an increasing popularity. This DLG structure, where two individual graphene layers are separated by a gate oxide, forms a capacitor integrated on top of a passive waveguide. Compared to a device based on a single-layer graphene on a doped silicon waveguide, the DLG EAM offers not only stronger modulation but also compatibility with various waveguide platforms [17]. As such, the integration of a DLG structure onto SiN [31,32] waveguides and silicon slot waveguides [33,34], has been discussed in several papers. However, it is worth noting that only limited experimental research has been conducted, which validates the theoretical predictions and explores the practical feasibility of DLG-based EAMs integrated on such alternative waveguide platforms.

In this work, we experimentally demonstrate a graphene-integrated EAM based on a silicon slot waveguide (Figure 1). The slot waveguide confines light within a thin and low-refractive-index region, thereby enhancing the interaction between light and graphene [35]. Notably, the dimensions of our slot waveguide (680 nm width with a 180 nm gap) can be defined with standard DUV lithography techniques, which enables large-scale fabrication and integration of slot waveguides in high-density systems. Figure 1(b) illustrates the slot waveguide-based DLG EAM (SLOT-DLG EAM), including a mode converter facilitating the transition between strip and slot waveguides (See Supplement 1). Using this device, we have demonstrated a modulation effieciency as high as 0.038 $dB\mu m^{-1}V^{-1}$. This is comparable to state-of-the-art DLG EAM devices utilizing high-quality exfoliated graphene and relying on the quasi TM-polarized mode, which is less preferred in practical applications [22]. Furthermore, we achieved an EO bandwidth of approximately 16 GHz. Unfortunately, the insertion loss of our devices is higher than expected. Through simulations, we attribute this loss to absorption in the metal contacts. In slot waveguides, the enhanced confinement in the small gap comes at the cost of an expansion of the evanescent field [36]. These results inspired us to carry out an extensive design study, comparing the true potential of the SLOT-DLG EAM versus a conventional strip waveguide (STRIP-DLG EAM) based graphene modulator. We focus on three crucial design parameters and explore the associated trade-offs in insertion loss, extinction ratio and bandwidth. The simulation results offer valuable insights into the influence of each design parameter, reaffirming that our slot waveguide platform holds great promise for realizing a high-performance EAM balancing optical and electrical performance.

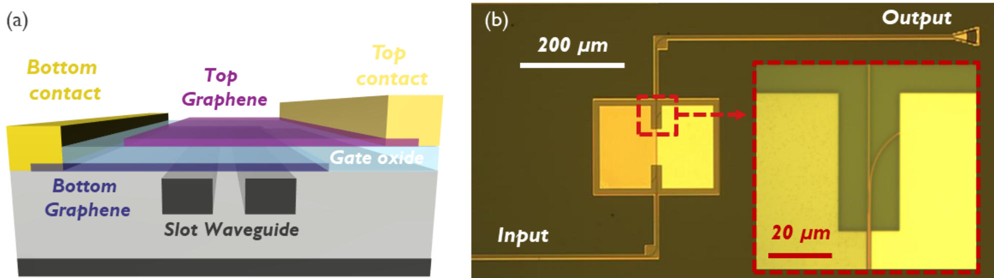

Fig. 1. (a) A 3D schematic and (b) top-down microscope image of DLG EAM integrated on a silicon slot waveguide.

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2. Fabrication and electro-optical results

The fabrication of the modulators started from a 200-mm silicon-on insulator (SOI) wafer with a 220 nm crystalline silicon (c-Si) layer and a 2 µm buried oxide (BOX), as illustrated in Figure 2(a). Standard 193 nm lithography was utilized to pattern the c-Si layer with a waveguide width of 450 nm for the STRIP-DLG EAMs and 680 nm (with a 180 nm gap) for the SLOT-DLG EAMs, respectively. After waveguide patterning and 2 µm oxide deposition, the wafer was planarized with chemical mechanical polishing (CMP) until a 10 nm-thick buffer oxide was left on top of the waveguides (see Figure 2(b)). Next, the wafer was diced for graphene processing. The first CVD-grown graphene layer (GRA1) was transferred using a wet-transfer technique, and cleaned using aceton (Figure 2(c)). After that, electron beam lithography (EBL) was employed to define the shape of the graphene layer by using a double layer resist process. The process involved using poly-methyl methacrylate (PMMA) at the bottom for protecting the graphene layer and hydrogen silsesquioxane (HSQ) on top being exposed by EBL. Note that the required patterning accuracy could be readily reached by a deep UV lithography system as we recently demonstrated [23]. After exposure and development, an oxygen plasma was used to pattern the graphene layer together with the PMMA layer (Figure 2(d)). Then, the 20 nm Pd metal contacts were fabricated through EBL and a lift-off process. Figure 2(e) schematically shows the structures after the lift-off process. The contacts covered part of the top and the edge of the graphene layer, combining two well-known contact strategies [37,38], and targeting low contact resistance. Next, the gate oxide was grown using atomic layer deposition (ALD). To generate a uniform gate oxide on the self-passivated graphene layer, we first deposited 1 nm of Al by thermal evaporation and subsequently 10 nm Al_2O_3 was deposited by ALD (Figure 2(f)). The second graphene layer (GRA2) was transferred, patterned, and contacted using the same process as that employed for the first layer. Figure 2(g) shows the finalized schematic cross-section, and Figure 2(h) and (i) shows the scanning electron microscope (SEM) images of the STRIP-DLG EAM and the SLOT-DLG EAM after the full integration process, respectively.

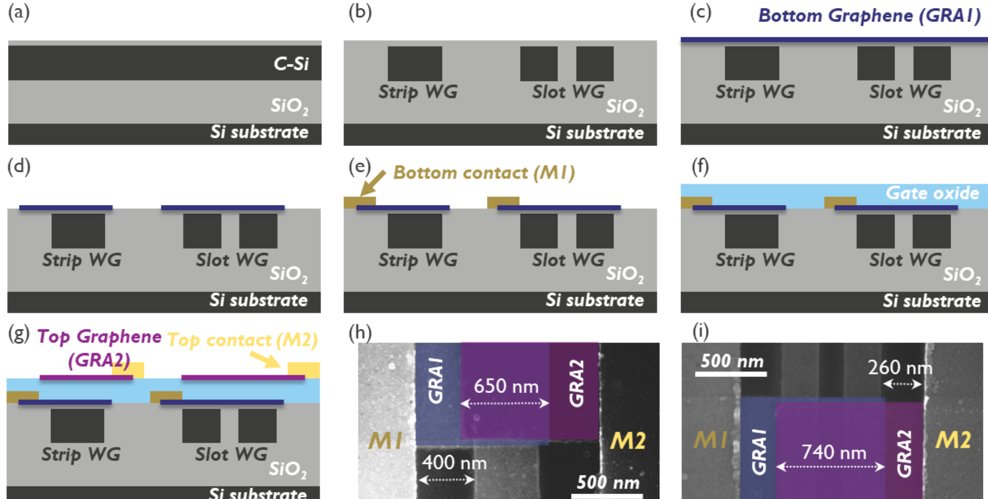

Fig. 2. Process flow for DLG EAM fabrication. (a) SOI wafer, (b) waveguide patterning and surface planarization, (c) wet transfer of first graphene layer, (d) patterning by ebeam, (e) contact with Pd, (f) Al_2O_3 deposition, (g) wet transfer of second graphene layer, patterning by ebeam, and contact with Pd. Top-down scanning electron microcope (SEM) images of (h) STRIP-DLG and (i) SLOT-DLG.

The DC performance of the DLG EAMs was characterized by applying a bias voltage, with the source at top contact and the ground at bottom contact. With our in-house EO measurement setup [39], Figure 3(a) and (b) present the measured transmission response of the two types of DLG EAMs, which are normalized by the transmission of an identical structure without DLG, at a wavelength of 1550 nm. The STRIP-DLG EAM shows the expected behavior, with a transmission which is modulatod from -2.8dB to -0.6dB when varying the normalised voltage from 0 to 9 Volt. At first sight, the SLOT-DLG EAM shows a similar behaviour, with a somewhat larger extinction ratio as expected. However, we consistently observed that the SLOT-DLG EAM exhibits significantly higher insertion loss. As both devices were fabricated on the same chip, the observed difference can not be explained solely by device-to-device variations. To understand the origin of these losses, we carried out simulations using a commercial mode solver (Lumerical). All device dimensions, including DLG width and metal distance, were taken from the actually fabricated devices shown in Figure 2(h) and (i). Four different scattering rates for the graphene layers were considered, where lower scattering rates indicate higher quality [18]. Considering initial doping values of 0.2 eV and -0.3 eV for the GRA1 and GRA2 layers respectively (See Supplement 1) and an equivalent oxide thickness of 9.5 nm (See Supplement 1), we found excellent agreement between the experimental and simulated results, as is clear from both Figure 3(a) and (b). Through these simulations, one significant factor contributing to the higher insertion loss in the SLOT-DLG EAM became evident: the short distance between the fabricated metal contacts and the slot waveguides. The slot waveguides exhibit larger evanescent wave tails outside the waveguide itself [36], necessitating a design with contacts placed further away from the slot waveguides to minimize the additional loss caused by the metal contacts. This adjustment in the layout could potentially mitigate the insertion loss and improve the overall performance of the SLOT-DLG EAMs, as will be discussed further in the next sections.

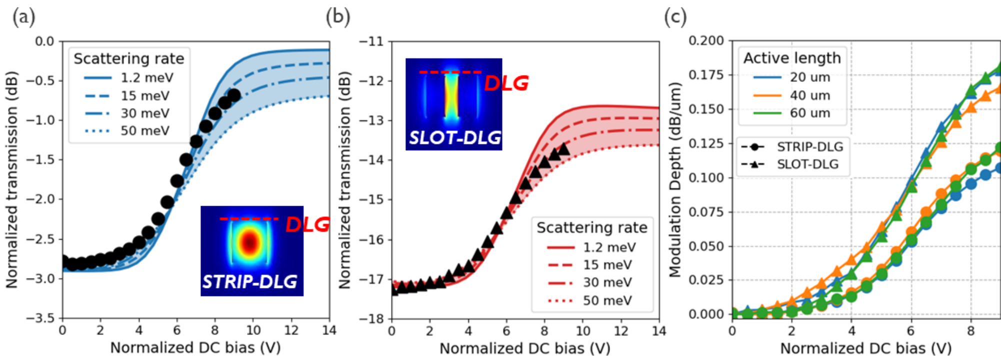

Fig. 3. Normalized transmission as a function of normalized DC bias for 20 μm (a) STRIP-DLG and (b) SLOT-DLG with simulated results in blue and red, respectively. (c) Modulation depth (MD) as a function of normalized DC bias for both STRIP-DLG and SLOT-DLG with 20, 40, and 60 μm active length.

Given this loss issue, the performance of the STRIP-DLG EAMs and SLOT-DLG EAMs was compared by normalizing their minimum transmission and extracting the modulation depth (MD). The MD excludes the effect of IL and can be used to compare the pure DC performance of the devices. Figure 3(c) presents the MD as a function of normalized DC bias for both STRIP-DLG EAMs and SLOT-DLG EAMs with varying active lengths. Both device types exhibited comparable DC performance, with maximal MD values of 0.122 dB/μm for STRIP-DLG EAMs and 0.183 dB/μm for SLOT-DLG EAMs. Within a 2V span, modulation efficiencies of 0.026 $dB\mu m^{-1}V^{-1}$ and 0.038 $dB\mu m^{-1}V^{-1}$ were measured for STRIP-DLG EAMs and SLOT-DLG EAMs, respectively. While the latter value is comparable to state-of-the-art devices [22], the

high insertion loss resulting from contact metal losses make our current SLOT-DLG EAMs unacceptable for practical applications. Therefore, in the next sections, we will delve into greater detail on potential improvement strategies and any necessary compromises.

The electro-optical (EO) bandwidth of the DLG EAMs was evaluated by sweeping the frequency from 100 MHz to 25 GHz using a network analyser to retrieve the S-parameters [39]. Figure 4(a) shows the normalized S21 values for STRIP-DLG EAMs of various lengths (20 μm, 40 μm, and 60 μm) and a SLOT-DLG EAM (20 μm). The extracted 3 dB bandwidth was determined to be 15.9 GHz for the 20 μm-long SLOT-DLG EAM and 15.9 GHz, 12.5 GHz, and 9.2 GHz for the 20 μm, 40 μm, and 60 μm long STRIP-DLG EAMs, respectively. The length-dependence in the results for the STRIP-DLG EAMs can be attributed to the influence of the 50 Ω impedance of the vector network analyzer (VNA) [23,40]. To gain a deeper understanding of our devices, the measured S11 response was fitted using the equivalent circuit model depicted in Figure 4(a). In the model, C_{gog} represents the capacitance of the DLG structures, while R_{tot} represents the total resistance, combining the contact and sheet resistance of both graphene layers. C_{air}, C_s, and R_s denote the capacitance between the metal pads, the capacitance of the silicon substrate, and the resistance of the silicon substrate, respectively. As shown in Figure 4(b) and (c), the real and imaginary parts of the S11 response were successfully fitted using this model. The capacitance values were found to be 53 fF, 45 fF, 92 fF, and 139 fF for the 20 μm (SLOT-DLG EAM), 20 μm (STRIP-DLG EAM), 40 μm (STRIP-DLG EAM), and 60 μm (STRIP-DLG EAM) long devices, respectively. The corresponding R_{tot} values were found to be 101 Ω, 116 Ω, 47 Ω, and 43 Ω. Considering all the other parasitic components, the resulting electrical 3 dB bandwidths were calculated to be 16.9 GHz, 17.8 GHz, 15.2 GHz, and 10.7 GHz, respectively, which closely align with the values observed in our experiments.

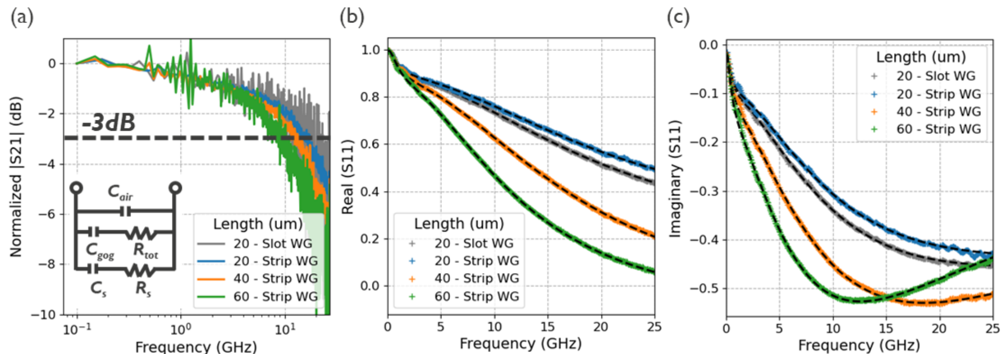

Fig. 4. (a) Normalized S21 response and the model. (b) Real and (c) imaginary part of S11 response and fitted results.

3. Discussion and simulations

To achieve a high-performance modulator, it is crucial to exhibit a sufficiently large extinction ratio (ER), a low insertion loss (IL), and a wide bandwidth at a CMOS-compatible drive voltage [4]. It is desirable to keep the peak-to-peak drive voltage (V_{pp}) as low as possible, preferably below 2 V. By doing so, one can effectively minimize system-level power consumption. By employing a slot waveguide, the modulation efficiency of a DLG EAM can be significantly improved. To fairly evaluate and compare different modulator designs more effectively, the concept of transmission penalty (TP) has been introduced [41]. The TP captures insertion loss and extinction ratio in a single figure of merit and is defined as $TP = (P_1 - P_2)/(2P_{in})$, where P_1 and P_2 are the high and low output power levels, respectively, and P_{in} represents the input power. A lower TP allows for

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reduced overall power consumption in optical networks. Our STRIP-DLG EAM exhibits a TP of 8.9 dB at V_{pp} = 2 V (See Supplement 1), which outperforms other state-of-the-art graphene-based modulators [20,22] and is comparable to Ge devices employing the Franz-Keldysh (FK) effect [11]. On the other hand, our SLOT-DLG EAM demonstrates a much worse TP > 20 dB, which can be attributed to the metal losses. To explore the true potential of a SLOT-DLG EAM, substantial simulations were conducted to investigate the impact of three device parameters: the metal offset (M_{off}), the gate oxide thickness (d_{ox}), and the width of the DLG (W_{DLG}), as defined in Figure 5(a). In the simulations, we utilized a conservative value for the graphene scattering rate (15 meV) and normalized contact resistance (500 Ω μm). It is important to note that the optical simulation was simplified by not considering initial doping. The gate oxide between GRA1 and GRA2 is Al_2O_3 with a dielectric constant of 7.8 [42,43]. The electrical bandwidth was calculated using the formula $f[Hz] = 1/(2\pi(R_{tot}[\Omega] + 50[\Omega])C_{gog}[F])$, where 50Ω represents the impedance from the driver. Although the product $R_{tot}C_{gog}$ is in principle length independent, this constant impedance introduces a length dependence in the electrical bandwidth. Devices with a shorter active length (larger resistance) are less influenced by the 50 Ω impedance compared to devices with a longer active length (smaller resistance). Therefore, determining the appropriate active length is crucial for a fair comparison. In our subsequent simulations, we choose the condition "ER = 4 dB at V_{pp} = 2 V" as the criterion for all simulated devices.

The first parameter we investigated is the metal offset M_{off}, ranging from 200 nm to 1000 nm, with d_{ox} = 20 nm and W_{DLG} = 650 nm and 740 nm for STRIP-DLG EAMs and SLOT-DLG EAMs, respectively. When the metal contacts are sufficiently far from the waveguides, the devices only exhibit the (desired) loss of the DLG EAMs, as indicated by the shaded bands in Figure 5(b). However, as the metal contacts are placed closer together, the loss increases exponentially. Figure 5(b) shows that SLOT-DLG EAMs require roughly twice the M_{off} compared to STRIP-DLG EAMs to mitigate the loss. Next, we present the absorption as a function of DC bias using a safe metal offset value (M_{off} = 1000 nm for both). Figure 5(c) shows that SLOT-DLG EAMs exhibits a higher modulation depth than STRIP-DLG EAMs but also a higher overall loss. This figure also shows that, due to the stronger modulation in SLOT-DLG EAMs, the required device length to satisfy the condition imposed on the extinction ratio is approximately half that of STRIP-DLG EAMs. After determining the length of both devices for a given DC bias, we calculate the associated TP and bandwidth, as shown in Figure 5(d). With a DC voltage V_{DC} = 7V, SLOT-DLG EAMs achieve the minimum length (around 42 μm) and the largest bandwidth (8.3 GHz). However, due to the higher loss at this point (4.9 dB), the TP value of 10.11 dB is not the best. We notice the minimal TP value (8.98 dB) occurs when V_{DC} = 8V. More importantly, it comes with only a slight reduction in bandwidth (8.0 GHz). Therefore, this point can be considered as the best compromise between TP and bandwidth. In Figure 5(e), this analysis has been repeated for devices with varying M_{off} values. Although there is a small increase in bandwidth (from 8 to 12 GHz) when M_{off} is decreased, the insertion loss (IL) and TP rise significantly if the metal contacts are placed too closely together. We found M_{off} = 450 nm and 750 nm to strike a good balance between TP and bandwidth for DLG-STRIP EAMs and DLG-SLOT EAMs, respectively. For this choice of parameters, the metal loss is less than 1e-3 dB/μm in both cases, resulting in a required length of approximately 47 μm (83 μm), IL of 3.8 dB (2.8 dB), ER of 4 dB (4 dB), TP of 9.01 dB (8.00 dB), and bandwidth of 9.2 GHz (10.0 GHz) for the SLOT-DLG EAM (STRIP-DLG EAM).

Next, the effect of the gate oxide thickness is explored for STRIP-DLG EAMs and SLOT-DLG EAMs with M_{off} = 450 nm and 750 nm and W_{DLG} = 650 nm and 740 nm, respectively. Figure 6(a) illustrates the absorption for the SLOT-DLG EAM as a function of voltage for gate oxide thicknesses ranging from 5 nm to 40 nm. Two notable observations can be made from the figure. First, at V_{DC} = 0 V, the absorption decreases from 0.29 dB/μm to 0.23 dB/μm as the thickness increases. This can be attributed to the mode profile and the increasing vertical distance between

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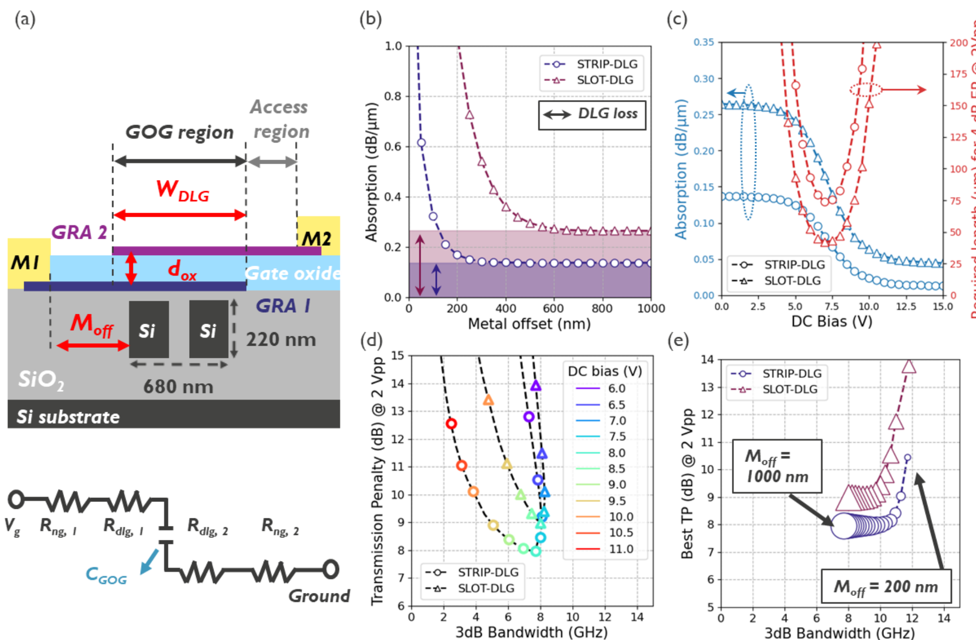

Fig. 5. (a)A 2D schematic of DLG EAM integrated on a slot waveguide. Three key design parameters are defined: M_{off}, d_{ox} and W_{DLG}. The equivalent electrical circuit of the DLG EAM is shown below, where V_g, R_{ng}, R_{dlg}, and C_{GOG} represent the input voltage, the resistance of the non-gated graphene section (including the contact resistance), the resistance of the gated graphene, and the capacitance of the device, respectively. Bandwidth is calculated with $8{\times}11^{11}$ cm^{-2} (equivalent to $E_F \approx 0.1$ eV) [44] for the graphene in the access regions to avoid an infinite resistance. A contact resistance of 500 $\Omega\,\mu m$ is considered for both graphene layers. (b) Simulated absorption as a function of M_{off} for STRIP-DLG EAMs and SLOT-DLG EAMs with wavelength = 1550 nm at the neutrality point(graphene chemical potential at 0 eV). The shaded bands indicate the (desired) loss of the DLG EAMs. The additional loss for smaller M_{off} stems from metal absorption. (c) Simulated absorption (blue curves) and required length for ER=4V at 2 V_{pp} (red curves) as a function of DC bias for both STRIP-DLG EAMs and SLOT-DLG EAMs with M_{off} = 1000 nm. (d) Simulated TP and the corresponding calculated bandwidth based on the results in Figure 5(c). (e) Best TP-bandwidth compromise for both device types with M_{off} ranging from 200 nm to 1000 nm (step = 50 nm), as illustrated by the size of the markers.

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GRA2 and the waveguide. At high voltages, where loss is minimal, the absorption becomes comparable (around 0.04 dB/μm), resulting in a greater modulation depth for devices with thinner gate oxide. Second, as the oxide thickness increases, the voltage required for graphene to enter the Pauli blocking region also increases [17]. For instance, a device with d_{ox} = 40 nm requires approximately V_{pp} = 30 V to modulate between maximum and minimum absorption, whereas a device with d_{ox} = 5 nm only needs V_{pp} = 5 V. Consequently, devices with thinner oxide can satisfy the criterion of a 4 dB extinction ratio (ER) at V_{pp} = 2 V with a shorter active length compared to devices with thicker oxide. Figure 6 (b) shows the required length for both devices at the point of achieving the best TP. The corresponding capacitance is determined by considering the required length and capacitance density for different gate oxide thicknesses. As the thickness increases, the capacitance initially decreases sharply and then gradually increase. Figure 6(c) presents the TP-bandwidth trade-off. Although the device with d_{ox} = 5 nm exhibits the best TP values of 6.30 dB and 5.84 dB for SLOT-DLG EAMs and STRIP-DLG EAMs, respectively, it also has the lowest bandwidth of 2.9 GHz and 3.7 GHz. Increasing the oxide thickness can enhance the bandwidth but worsens TP, which exhibits a steep increase when d_{ox} exceeds 20 nm. Therefore, a thickness of 20 nm is considered ideal for achieving a good balance between TP and bandwidth.

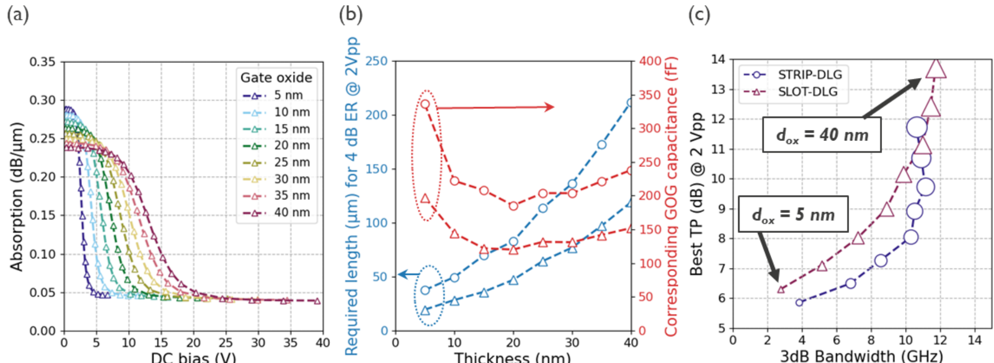

Fig. 6. (a) Simulated absorption of SLOT-DLG as a function of DC bias at 1550 nm wavelength, for gate oxide thickness ranging from 5 to 40 nm. (b) Required length (blue curves) and corresponding DLG capacitance as a function of d_{ox} for both STRIP-DLG and SLOT-DLG. (c) Best TP-bandwidth compromise for both device types with d_{ox} ranging from 5 nm to 40 nm (step = 5 nm), as illustrated by the size of the markers.

Lastly, we investigate the influence of the width of the DLG capacitive stack. Reducing W_{DLG} can decrease the capacitance of the device, leading to a larger 3 dB bandwidth. However, this improvement comes with a trade-off. With a narrower DLG width, the optical mode interacts less with the graphene-oxide-graphene (GOG) region and more with the access region (graphene layer between contacts and GOG stack). Since no initial doping is applied, the access region often exhibits high optical loss and does not contribute to modulation. Figure 7(a) shows that, as W_{DLG} decreases from 1000 nm to 200 nm, the modulation depth decreases (from 0.29 dB/μm to 0.22 dB/μm) and the minimum loss increases (from 0.03 dB/μm to 0.08 dB/μm), resulting in a deteriorated TP value. Figure 7(b) shows how the optimal TP-bandwidth compromise changes when decreasing W_{DLG} decreasing from 1000 nm to 200 nm. For completeness, we included a third device type (STRIP-TM-DLG EAM), which uses the quasi TM-polarised waveguide mode (with M_{off} = 600 nm and d_{ox} =20 nm). Figure 7(b) shows that narrowing the GOG stack of a SLOT-DLG EAM can improve the bandwidth from 7.5 GHz to 26.7 GHz, at the cost of increasing the TP value from 7.97 dB to 12.63 dB. Comparing the different device types, it can be seen that they exhibit similar optical and electrical performance when W_{DLG} is large, e.g. 1000 nm. When reducing W_{DLG}, initially the TP for the SLOT-DLG EAM deteriorates significantly,

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making it less efficient compared to the other devices. However, when W_{DLG} becomes less than 400 nm, the SLOT-DLG EAM starts to outperform the other two. For W_{DLG}= 200 nm a bandwidth of 26.7 GHz and TP = 12.63 dB is obtained. Finally, we repeated this simulations, assuming a higher quality graphene (scattering rate = 1.2 meV). Such quality can currently be obtained using exfoliated graphene and might in the future also be attainable for graphene grown using waferscale methods [45,46]. The results in Figure 7(c) clearly indicate improvements in both TP and bandwidth for each data point. Notably, compared to STRIP-DLG EAMs and STRIP-TM-DLG EAMs, the SLOT-DLG EAMs demonstrates a higher potential for achieving a good compromise between high speed and low transmission penalty while generating the desired extinction ratio at a practical drive voltage.

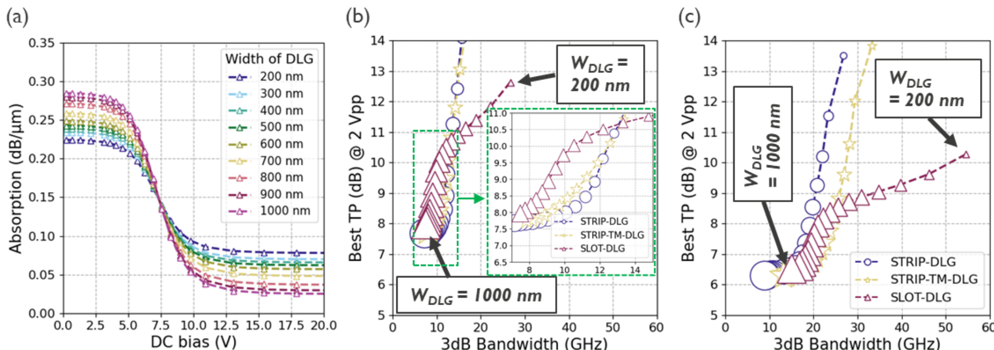

Fig. 7. (a) Simulated absorption of SLOT-DLG EAMs as a function of DC bias at 1550 nm wavelength, for DLG EAMs width ranging from 200 to 1000 nm. (b,c) Best TP-bandwidth compromise for three device types, with graphene scattering rate of (b) 15meV and (c) 1.2meV. W_{DLG} ranges from 200 nm to 1000 nm (step = 50 nm), as illustrated by the size of the markers.

4. Conclusion

In conclusion, this paper presents the experimental demonstration of strip and slot waveguide-based graphene EAMs. Leveraging the narrow mode profile and strong mode confinement on the graphene layers, the SLOT-DLG EAM was shown to exhibit a remarkable modulation efficiency of 0.038 $dB\mu m^{-1}V^{-1}$ and a bandwidth of ≈ 16 GHz. However, the current SLOT-DLG-EAM also showed a higher insertion loss than the STRIP-DLG EAM. Through extensive simulations, starting from the dimensions of the actually fabricated devices, we could show that this loss stems from the metal contacts, which were located too close to the waveguide for the SLOT-DLG EAM. Importantly however, excellent agreement between measured and simulated results was obtained for both device types. Taking these results as a starting point, an extensive design study was carried out, varying the main dimensional parameters of both devices types to find an optimum in the trade-off between extinction ratio, insertion losses and modulation bandwidth. This study shows that the SLOT-DLG EAM can indeed provide an overall better device compared to the STRIP-DLG EAM, with lower transmission penalty at higher bandwidths, if the width of the capacitive GOG stack is decreased below 400 nm and if the metal contacts are separated sufficiently far from the waveguide. This highlights the potential of slot waveguide-based devices as a superior platform for realizing high-performance EAMs and their use in next-generation data communication and telecommunications applications.

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Disclosures. The authors declare no conflicts of interest.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental document. See Supplement 1 for supporting content.

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