A Photonic Interconnect Layer on Silicon
Dries Van Thourhout – MNE ‘07

Electrically pumped Array of InP microdisk sources
Silicon wire waveguides
Towards microdetectors
Acknowledgements

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A Photonic Interconnect Layer on Silicon

Outline
- Silicon photonics: why, how, who?
- Passive structures
- Towards active devices: InP on SOI
- An application: on-chip optical interconnect
- Conclusion and outlook
**Electronics vs. Photonics**

**Electronics**
- Single material: Silicon (also provides insulator SiO₂)
- One platform: CMOS
- Large market: highly tuned, mature processes
- One main building block: the transistor
- Common ITRS roadmap (dominated by a few large companies)
- Size: 10nm → few um

**Photonics**
- Many incompatible materials: GaAs, InP, Polymers, LiNbO₃, ...
- Many processing technologies
- Limited market: primitive processes
- Many building blocks: resonators, lasers, detectors, ...
- Many factions pushing their own solutions
- Size: few um → few cm

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**Silicon photonics**

... the solution to all our problems
- Transparent at telecom wavelengths (1.3um, 1.55um)
- High refractive index contrast ➔ ultra-compact circuits
- “Compatible” with CMOS-processing
  - Highest quality processes
  - High yield, high repeatability
Typical waveguide structure

Waveguide Definition

- SiO₂ (1-2um) x Height (220nm)
- Silicon

- Similar waveguide structure used by many other groups
  - IMEC, LETI, Pirelli, MIT, IBM, Luxtera, NTT, NEC, Cornell, Yokahama ...

- Typical loss: 1.5dB/cm – 3dB/cm
  - Dominated by LER
  - (see also poster P-NSC-37 by S. Sardo e.a.)

- Pattern definition: ebeam lithography, nanoimprint, DUV litho

Our current Fabrication Process

Si-substrate
SiO₂
Si
Photoresist
AR-coating
wafer Photoresist (UV3)
Bare Soft bake AR coating Illumination (248nm or 193 deep UV)
bakePost Development
Hardening
Silicon etch Resist strip
AR-coating
Illumination (248nm or 193 deep UV)
Post bake Development Resist Hardening Silicon etch Resist strip
Basic structures

Low loss bends

<0.3dB excess loss for splitters

97% transmission in crossings

Wavelength dependent devices

[Diagram showing various structures and graphs related to optical waves and transmission characteristics]
Complex filters

- 9x16 AWG
- 16 channels, 200GHz channel spacing
- 36 arrayed waveguides
- 0.1mm² footprint

- 2.2dB insertion loss (on-chip)
- 18dB crosstalk suppression

Increasing Index Contrast

Glass photonic ICs
Low Contrast - Fiber Matched
(doped silica vs pure silica)
Waveguide: 10x10 µm
Bend Radius ~ 5 mm

Silicon photonic ICs
Ultra-high Contrast
(silicon vs silica)
Waveguide: 500x200nm
Bend Radius < 5 µm

III-V photonic ICs
Medium Contrast
(InGaAsP vs InP)
Waveguide: 2x1µm
Bend Radius ~ 500µm

Is this Nano?

- Typical linewidth: 400nm to 500nm
- Hole pitch: 300nm to 500nm

BUT

- Linewidth needs to be controlled within 1nm (or below)!
- LER < 2nm!
- Holes, gaps, narrow lines all on same litho level!
Use for sensing ...

Two dimensional strain sensor

- Silicon circuits transferred to polyimide film

Biosensor

- light from tunable laser
- light to photodetector
- optical fibers
- fluidic channel
- SOI biosensor chip
- temperature control

Silicon has indirect bandgap

- Lot of research going on to overcome this problem (nanocrystals, raman ...)
- Thus far not satisfactory

Integrate III-V with Silicon

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III-V on Silicon ???

Flip-chip bonding

Thin film device integration

III-V epi on Silicon

Integration through die-to-wafer bonding

(Duke University)

Alignment ?
Reliability ?
Mass production ?

Proposed integration process

Starting point: Processed SOI-waveguide wafer

- 248nm DUV lithography
  - Fabricated in IMEC pilot CMOS-line

Proposed integration process

Planarization

- Planarization
  - SiO$_2$-deposition and CMP (Collaboration with LETI/TRACIT)
  - or: BCB spin-on-layer (IMEC)

Proposed integration process

Die-to-wafer bonding

- Bonding InP-dies on top of planarized SOI-wafer
  - Low alignment accuracy required
  - Fast pick-and-place
**Proposed integration process**

**Substrate removal**

- Remove InP-substrate down to etch stop layer
- Remove etch stop
- Thin membrane remains (200nm ~ 2um)

**Proposed integration process**

**Hardmask deposition**

- Decontamination and hardmask deposition
  - Alignment of waveguides and devices through lithographic methods
**Proposed integration process**

**Processing of InP-optoelectronic devices**

- Mesa etching and Metallization
  - “Waferscale” processing !!! (but on 2cm² pieces)

**Die-to-wafer Bonding**

- **Molecular bonding (fusion)**
  - InP on SOI-waveguides on CMOS demonstrated (LETI, TRACIT)

- **Polymer bonding**
  - Planarization and bonding in single step (IMEC)
  - Ultra-thin bonding layers (sub 200nm demonstrated)
Bonding of III-V epitaxial layers

- **Molecular die-to-wafer bonding**
  - Based on van der Waals attraction between wafer surfaces
  - Requires “atomic contact” between both surfaces
    - very sensitive to particles
    - very sensitive to roughness
    - very sensitive to contamination of surfaces

- **Adhesive die-to-wafer bonding**
  - Uses an adhesive layer as a glue to stick both surfaces
  - Requirements are more relaxed compared to Molecular
    - glue compensates for particles (some)
    - glue compensates for roughness (all)
    - glue allows (some) contamination of surfaces

*While established technology for SOI, III-Vs often do not meet the requirements for molecular bonding*

Bonding Technology

Requirements for the adhesive for bonding

- Optically transparent
- High thermal stability (post-bonding thermal budget) 400°C
- Low curing temperature (low thermal stress) 250°C
- No outgassing upon curing (void formation) OK
- Resistant to all kinds of chemicals HCl, H2SO4, H2O2, ...

DVS-BCB satisfies these requirements

1,3-divinyl-1,1,3,3-tetramethyldisiloxane-bisbenzocyclobutene
Bonding Technology

Overview of the bonding process

- Die/wafer cleaning most critical step in processing
  - SOI wafer: standard clean – 1 (H2SO4:H2O2:H2O @70°C)
    - Lifts off particles from surface and prevents redeposition
  - InP/InGaAsP: removal of sacrificial InP/InGaAs layer pair

Cross-sectional image of III-V/Silicon substrate
Integrated laser diodes

- Fabry-Perot laser cavity by etching InP/InGaAsP laser facets
- Inverted adiabatic taper coupling approach

Integrated Devices: laser diode

- Only pulsed operation due to high thermal resistivity DVS-BCB
- Integration of a heat sink to improve heat dissipation
- Continuous wave operation achieved this way
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On-chip optical interconnect?

**IBM Cell processor**
- Multicore processor chip
- Now: ~ 1 TBit/s data bandwidth
- By 2015: 35-70 TBit/s expected!
- Note: 10 MBit/s km = 1 Tbit/s cm

**ITRS-roadmap** requests research in alternative interconnect options
- Optical one possible option
- Deployment expected around 2015

**On-chip optical interconnect?**

**Our goal:** build photonic interconnect layer on CMOS

- Using on-chip microsources and detectors
- Compatible with IC-production
- At reasonable price \( \rightarrow \) wafer-scale processes
- Between topmost metal layers
Integrated microdisk laser

Microdisk laser design

- Whispering-gallery modes
- Central top contact
- Bottom contact on thin lateral contact layer ($t_s$)
- Hole injection through a reverse-biased tunnel-junction

- Microdisk thickness $0.5 < t < 1 \mu m$
- Evanescent coupling to SOI wire waveguide ($500 \times 220 \text{nm}^2$)

→ European research programme PICMOS
(Photonic Interconnect Layer on CMOS by Waferscale Integration,
FP6-2002-IST-1-002131)


Integrated microdisk laser

25 µm

InP island  SOI waveguide microdisk

BCB InP - InGaAsP
SiO$_2$ Si wire
Si substrate

130-nm bonding layer

Measurement setup

Continuous-wave lasing

1-µm thick, 7.5-µm devices exhibit continuous-wave lasing

Threshold current $I_{th} = 0.5\, mA$, voltage $V_{th} = 1.5-1.7V$
slope efficiency $= 30\, \mu W/mA$, up to $10\, \mu W$
(Pulsed regime: up to $100\, \mu W$ peak power)

J. Van Campenhout et al., "Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit" Optics Express, May 2007
Temperature dependence

“Laser emission up to 70°C”
(pulsed operation)

Fit to experimental data

Model can be fitted to pulsed experimental data, assuming:

- uniform injection: injection efficiency = 0.36 x 0.7 = 0.25
- coupling loss = 3 cm⁻¹ (simulation)
- tunnel-junction p-doping $N_d = 2 \times 10^{18}$ cm⁻³
  (design target $N_d = 2 \times 10^{19}$ cm⁻³, SIMS analysis: $N_d \approx 8 \times 10^{18}$ cm⁻³)
- fitted scatter loss = 8 cm⁻¹ (passive ring resonators: 7-13 cm⁻¹)

Consistent fit, except for tunnel-junction p-doping and saturation effect
Sources vs. modulators

Source based approach
- Conceptually simple
- Direct modulation
- No wavelength matching needed
- High temperature operation?
- Integration process?

Off-chip source + modulators
- Simpler integration
- Resonator wavelength sensitive to temperature variations
- Power needed for modulators?
- Off-chip source needed + fibre coupling

Full Link
Demonstrator die (contains)
- 120 Microdisk lasers
- 120 DBR microlasers
- 264 Micro detectors (TU Eindhoven / Cobra)

**Pulsed operation of the link**

- Detector not biased (0V), negligible dark current
- Performance under pulsed operation:
  - Threshold current < 700 µA & Slope efficiency ~ 1.1 µW/mA
  - Detector efficiency of 0.23-0.29 A/W.
- Duty cycle = 8%  Period = 1 µs

**CW operation of the link**

- Detector not biased (0V), negligible dark current
- CW laser performance:
  - Threshold current ~ 600 µA & Slope efficiency ~ 1 µW/mA
  - Detector efficiency of 0.27-0.59 A/W.
- Unstable output power above 1.5mA
- Micro-disk is lasing in two directions
- Output direction varies in time + as function of applied voltage
On-Chip Optical Interconnect

Next step: integrate photonic interconnect on CMOS

- Through wafer-to-wafer bonding
- Or: Above IC processing using amorphous silicon

Outline

- Introduction & specifications
- The integration process
- Electrically pumped microsources
- Microdetectors
- Full optical point-to-point link

Conclusion and outlook
Outlook & conclusion

We demonstrated:

- Ultra-dense waveguiding
  - < 2um pitch (waveguide-to-waveguide)
- First electrically pumped micro-disk sources on silicon platform
  - 500uA threshold current
- Micro-detectors on silicon platform
  - 1.0A/W
- Full point-to-point link
- Fabrication using waferscale processes
  - In CMOS-pilot line
  - InP processing does not pose contamination problem

Outlook & conclusion

We still need to:

- Improve source performance
  - Towards 50uA threshold current – 10GHz modulation speed – 30% internal efficiency
  - Through improved processing
  - Through improved device design
  - Improved high temperature operation
- Full fabrication in CMOS pilot-line
- Integration with CMOS electronic driving circuit
- Implement WDM-functionality

WADIMOS
Wavelength division multiplexed photonic layer on CMOS
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See you in 2011 …
Acknowledgements

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- R. Notzel, X.J.M. Leijtens (TU/e) (epitaxy)

ePIXnet Silicon Photonics Platform (IMEC+LETI) for organizing MPW runs on a a cost-sharing basis
- Also for you ! See www.siliconphotonics.eu