III-V silicon heterogeneous integration

Dries Van Thourhout – IPRM ‘08, Paris
III-V silicon heterogeneous integration
Dries Van Thourhout – IPRM ‘08, Paris

1. Silicon photonics is great !!!
2. But we still need InP
3. III-V silicon integration
4. Devices
Acknowledgements

Photonics Research Group

- III-V silicon integration:
  - G. Roelkens, J. Van Campenhout, J. Brouckaert, L. Liu

- Silicon Processing
  - W. Bogaerts, P. Dumon, S. Selvarajan, R. Baets

EU IST-PICMOS team

- J.M. Fedeli, L. Di Cioccio (LETI) (molecular bonding, processing)
- C. Seassal, P. Rojo-Romeo, P. Regreny, P. Viktorovitch (INL) (processing, epitaxy)
- R. Notzel, X.J.M. Leijtens (TU/e) (epitaxy)
- C. Lagahe, B. Aspar (TRACIT) (planarization)
III-V silicon heterogeneous integration

1. Silicon photonics is great !!!
2. But we still need InP
3. III-V silicon integration
4. Devices
Silicon photonics: the solution to all our problems?

- Transparent at telecom wavelengths (1.3 µm, 1.55 µm)
- High refractive index contrast
- Ultra-compact circuits
- "Compatible" with CMOS-processing
- "Highest quality processes, high yield, high repeatability"
- Integration with electronics
- Pattern definition: DUV litho

Width (500nm) x Height (220nm)

Silicon

SiO$_2$ (1-2 µm)
Photonic wiring

Low loss bends

<0.3 dB excess loss for splitters

Excess bend loss [dB/90°]

Radius [μm]

97% transmission in crossings

Wavelength dependent devices

Increasing Index Contrast

Glass based devices
Bend Radius ~ 5 mm

Silicon photonic ICs
Bend Radius < 5 µm

InP/InGaAsP
(bend radius ~ 500um)
Silicon Photonics

Intel 40GHz Detector

Luxtera Ethernet Transceiver

IBM Modulator

Silicon Photonics

Silicon photonics comes in many flavors ...

- Large rib type waveguides
- Small core devices

- Easy coupling with fiber
- Optimized for nanophotonics
- Large device size
- Small device size
- This work and many others

- e.g. www.kotura.com
- e.g. www.luxtera.com

Full CMOS integration

- Fabricated in CMOS process
- Directly integrated with electronics
- e.g. www.luxtera.com
III-V on silicon?

Silicon photonics gives us:

- Excellent passives
- Fast modulators, fast photodetectors
- But: (almost) no light ...

➔ Need for integration with III-Vs

Requirements

- High density (~10-20um device pitch)
- High alignment accuracy (~100nm)
- Waferscale processes
1. Silicon photonics is great !!!

2. But we still need InP

3. III-V silicon integration

4. Devices
There are several ways to integrate III-V on SOI:

- **Flip-chip integration of opto-electronic components**
  - 😊 most rugged technology
  - 😊 testing of opto-electronic components in advance
  - 😞 slow sequential process (alignment accuracy)
  - 😞 low density of integration

- **Hetero-epitaxial growth of III-V on silicon**
  - 😊 collective process high density of integration
  - 😞 mismatch in lattice constant, CTE, polar/non-polar
  - 😞 contamination and temperature budget

- **Bonding of III-V epitaxial layers**
  - 😊 sequential but fast integration process
  - 😊 high density of integration, collective processing
  - 😊 high quality epitaxial III-V layers

See other talks at this conference
Proposed integration process

Starting point: Processed SOI-waveguide wafer

- 193nm or 248nm DUV lithography
  - Fabricated in pilot CMOS-line
Proposed integration process

Planarization

- Planarization
  - Using BCB (50nm to 2um) (UGent/IMEC)
  - Using SiO$_2$ (TRACIT - CEA-LETI)
Proposed integration process

Die-to-wafer bonding

- Bonding InP-dies on top of planarized SOI-wafer
  - Low alignment accuracy required
  → Fast pick-and-place
Proposed integration process

Substrate removal

- Remove InP-substrate down to etch stop layer
- Remove etch stop
- Thin membrane remains (200nm ~ 2 µm)
Proposed integration process

Hardmask deposition

- Decontamination and hardmask deposition
  - Alignment of waveguides and devices through lithographic methods
Proposed integration process

Processing of InP-optoelectronic devices

- Mesa etching and Metallization
  - “Waferscale” processing !!!
    - on 2cm² pieces (UGent, INL)
    - on 200mm wafers (CEA-LETI)

III-V/Silicon photonics

Bonding of III-V epitaxial layers

- **Molecular die-to-wafer bonding**
  - Based on van der Waals attraction between wafer surfaces
  - Requires “atomic contact” between both surfaces
    - very sensitive to **particles**
    - very sensitive to **roughness**
    - very sensitive to **contamination of surfaces**

- **Adhesive die-to-wafer bonding**
  - Uses an adhesive layer as a glue to stick both surfaces
  - Requirements are more relaxed compared to Molecular
    - glue **compensates** for particles (some)
    - glue **compensates** for roughness (all)
    - glue **allows** (some) contamination of surfaces

Bonding Technology

Requirements for the adhesive for bonding

- Optically transparent
- High thermal stability (post-bonding thermal budget) 400°C
- Low curing temperature (low thermal stress) 250°C
- No outgassing upon curing (void formation) OK
- Resistant to all kinds of chemicals HCl, H₂SO₄, H₂O₂,...

DVS-BCB satisfies these requirements

1,3-divinyl-1,1,3,3-tetramethyldisiloxane-bisbenzocyclobutene
Bonding Technology

Cross-sectional image of III-V/Silicon substrate

- 300nm bonding layer routinely and reliably obtained
Bonding Technology

Cross-sectional image of III-V/Silicon substrate

- 300nm bonding layer routinely and reliably obtained
- Recently also sub-100nm layers demonstrated

III-V silicon heterogeneous integration

1. Silicon photonics is great!!!
   2. But we still need InP
   3. III-V silicon integration
   4. Devices
Integrated Devices: laser diode

Integrated laser diodes

- First only pulsed operation due to high thermal resistivity
- Integration of a heat sink to improve heat dissipation
- Continuous wave operation achieved this way
Other groups

Intel / UCSB Hybrid laser

CEA-LETI / III-V lab

© intec 2007 - Photonics Research Group - http://photonics.intec.ugent.be (IPRM '08, paper MoA4.2)
MSM detectors

- Etching of detectors in III-V
- Spinning insulation layer of polyimide
- Opening contact window
- Metallization

25µm long detector

\[ R = 1.0\text{A/W (1550nm), IQE = 80\% (5V bias)} \]
\[ I_{\text{dark}} = 3\text{nA (5V bias)} \]

SOI waveguides (30µm pitch)

\[ L=30\mu m, d=400\text{nm} \]

No absorption

InGaAs absorption
Wavelength selective filter

1x4 demux, Δλ=20nm, 280µm x 150µm

V_{bias} = -10V
Integrated microdisk laser

Microdisk laser design

- **Whispering-gallery** modes
- Central top contact
- Bottom contact on thin lateral contact layer ($t_s$)
- Hole injection through a reverse-biased tunnel-junction

- Microdisk thickness $0.5 < t < 1 \mu m$
- **Evanescent coupling** to SOI wire waveguide ($500x220 nm^2$)

On-chip optical interconnect?

Integrate photonic interconnect on CMOS?

- Need integrated interconnect layer on top of CMOS
  - Silicon wiring for interconnect
  - III-V microdevices for sources and detectors
A collaborative project …

IMEC: SOI-wafer fabrication
TU/e: detector etching
IMEC: metallization
III-V processing
TRACIT: planarization
INL: substrate removal
INL: source etching

LETI: bonding
LETI: hard mask
Si substrate
130-nm bonding layer

BCB
InP - InGaAsP
SiO₂
Si wire

InP island
SOI waveguide
Microdisk

Six cleanrooms but still working devices …
Continuous-wave lasing

1-µm thick, 7.5-µm devices exhibit continuous-wave lasing

Threshold current $I_{\text{th}} = 0.5 \text{mA}$, voltage $V_{\text{th}} = 1.5-1.7\text{V}$

slope efficiency = $30\mu\text{W/mA}$, up to $10\mu\text{W}$

(Pulsed regime: up to $100\mu\text{W}$ peak power)

J. Van Campenhout et al., "Electrically pumped inp-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit" Optics Express, May 2007
Temperature dependence

“Laser emission up to 70°C”
(pulsed operation)

\[
\frac{d\lambda}{dT} \approx 86 \text{ pm K}^{-1}
\]

\[
\frac{dn}{dT} (\text{InP}) \approx 2 \times 10^{-4} \text{ K}^{-1}
\]

\[
\frac{dn}{dT} (\text{BCB}) \approx -7 \times 10^{-3} \text{ K}^{-1}
\]
Model can be fitted to pulsed experimental data, assuming:

- uniform injection: injection efficiency = 0.36 × 0.7 = 0.25
- coupling loss = 3 cm^{-1} (simulation)
- tunnel-junction p-doping $N_a = 2 \times 10^{18}$ cm^{-3} (design target $N_a = 2 \times 10^{19}$ cm^{-3}, SIMS analysis: $N_a \sim 8 \times 10^{18}$ cm^{-3})
- fitted scatter loss = 8 cm^{-1} (passive ring resonators: 7-13 cm^{-1})

Consistent fit, except for tunnel-junction p-doping and saturation effect.
Ultra-low-power Wavelength conversion

- No control power needed.
- Wavelength conversion with only 6.4uW control power.
- 5Gbps dynamic results.
Full Link

Demonstrator die (contains:

- 120 Microdisk lasers
- 120 DBR microlasers
- 264 Micro detectors (TU Eindhoven / Cobra)
- 120 Microdetectors
- 7mm
- 9mm
- 200mm SOI wafer

© intec 2007 - Photonics Research Group
Pulsed operation of the link

- Duty cycle = 8%  Period = 1 µs

- Detector not biased (0V), negligible dark current

- Performance under pulsed operation:
  - Threshold current < 700 µA
  - Detector efficiency of 0.23 - 0.29 A/W

© intec 2007 - Photonics Research Group
Outlook & conclusion

We demonstrated:

- Ultra-dense waveguiding
  - < 2 µm pitch (waveguide-to-waveguide)
- A powerful III-V on Silicon integration technology
- Several proof-of-principle demonstrators
  - Electrically pumped micro-disk sources on silicon platform
    - 500 µA threshold current
  - Micro-detectors on silicon platform
    - 1.0A/W
- Fabrication using wafer-scale processes
Outlook & conclusion

- Towards 50 µA threshold current
- 10GHz modulation speed – 30% internal efficiency

- Through improved processing:
  - Full fabrication in CMOS pilot line
  - Integration with CMOS electronic driving circuit
  - Implement WDM-functionality

- Through improved device design:
  - Improved high temperature operation

- Multi-wavelength sources
  - λ₁, λ₂ ... λ_N-1, λ_N
  - λ₁, λ₂ ... λ_N-1, λ_N

Single wavelength

Multi-wavelength Laser

4-wavelength laser

SM fiber

Biasing conditions:
- **10 µm diameter**
  - Biased at: 4 mA
  - FSR = 23 nm

- **7.5 µm diameter**
  - Biased at: 3 mA
  - FSR = 32 nm

Wavelengths:
- **10 µm diameter**
  - D1, D2, D3, D4

- **7.5 µm diameter**
  - D1, D2, D3, D4
Outlook & conclusion

We still need to:

- Improve source performance
  - Towards 50 µA threshold current – 10GHz modulation speed – 30% internal efficiency
  - Through improved processing
  - Through improved device design
  - Improved high temperature operation

- Full fabrication in CMOS pilot-line
- Integration with CMOS electronic driving circuit
- Implement WDM-functionality
- Simplify overall processing
Outlook & conclusion

Simplify processing

- Avoid critical patterning in the III-V layer

Silicon racetrack

III-V film

Acknowledgements

Photonics Research Group

- III-V silicon integration:
  - G. Roelkens, J. Van Campenhout, J. Brouckaert, L. Liu
- Silicon Processing
  - W. Bogaerts, P. Dumon, S. Selvarajan, R. Baets

PICMOS team

- J.M. Fedeli, L. Di Cioccio (LETI) (molecular bonding, processing)
- C. Lagahe, B. Aspar (TRACIT) (planarization)
- C. Seassal, P. Rojo-Romeo, P. Regreny, P. Viktorovitch (INL) (processing, epitaxy)
- R. Notzel, X.J.M. Leijtens (TU/e) (epitaxy)
Fiber-chip coupling

Important:
- Low loss coupling
- Large bandwidth
- Coupling tolerance
- Fabrication
  - Limited extra processing
  - Tolerant to fabrication
- Low reflection
- Polarization?
Coupling to fiber – Grating coupler

Alternative: Grating couplers

- Waferscale testing
- Waferscale packaging
- High alignment tolerance

From Fibre

Towards optical circuit

Increase efficiency?

Top view

Improving performance
- Add bottom mirror
- Apodize
- "Other"

FIB cross-section

With mirror

Without mirror

1dB bandwidth > 40nm

Main Challenges

1. Coupling of light between III-V and Silicon

- Option 1: evanescent
  - Guiding in silicon
  - Requires thin bonding layer
  - Requires III-V thinner than <250nm

- Option 2: other (adiabatic, grating coupler …)
  - Guiding in III-V
  - Thicker III-V layer
  - Sometimes thicker bonding
Main Challenges

1. Coupling of light between III-V and Silicon
   - Option 1: evanescent
     - Guiding in silicon
     - Requires thin bonding layer
     - Requires III-V thinner than 250nm
   - Option 2: other (adiabatic grating coupler...)
     - Guiding in III-V
     - Thicker III-V layer
     - Sometimes thicker bonding

Loss at metal contact

2. Electrical injection
   - Metal contact on membrane devices without inducing additional loss
Integrated Devices: laser diode

Integrated laser diodes

- Fabry-Perot laser cavity by etching InP/InGaAsP laser facets
- Inverted adiabatic taper coupling approach

![Polyimide waveguide](image1.png)

![SOI Inverted taper](image2.png)

![BCB spacer layer / bonding layer](image3.png)