# Photonic Crystal Waveguides in SOI fabricated with deep UV lithography

Wim Bogaerts (1), Vincent Wiaux (2), Dirk Taillaert (1), Stephan Beckx (2), Roel Baets (1)
1 : Ghent University-IMEC, Dept. of Information Technology, Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium,
e-mail: Wim.Bogaerts@intec.rug.ac.be
2 : IMEC vzw, Silicon Process Technology Division, Kapeldreef 75, B-3001 Leuven, Belgium

***Abstract*** *We demonstrate photonic crystals for 1550nm wavelengths fabricated with 248nm-excimer laser deep UV lithography in silicon-on-insulator, combining high resolution with mass-manufacturing. The structures are of high quality. Measurements show transmission through waveguides and sharp bends.*

**Introduction**

Photonic Crystals (PhC) are photonic structures with periodic variations of the refractive index with wavelength-scale periods [1]. The fabrication of 2-D photonic crystals for telecom wavelengths is therefore a challenging task. For research purposes, most PhCs are fabricated with e-beam lithography (EBL), which is very accurate, but also very slow. Therefore an alternative is needed if one is to consider mass-fabricated components based on photonic crystals.

Deep UV lithography (DUV) is an optical lithography technology for wavelengths of 248nm and shorter and is already widely used for the fabrication of advanced CMOS components. However, the requirements for the fabrication of CMOS components differ from those of photonic integrated circuits.

We have performed experiments for the fabrication of PhC-based structures in silicon-on-insulator with 248nm DUV lithography and measured transmission through waveguides and bends.

**Photonic Crystal Slabs**

Photonic crystals can be periodic in 1, 2 or 3 dimensions. 3-D photonic crystals control light in 3-D space, but they are hard to make at optical wavelengths. An alternative is the combination of a 2-D PhC with an index-guiding layer structure in the third dimension [2,3]. In these photonic crystal slabs light is controlled in plane by the PhC and confined by total internal reflection in the vertical direction. Moreover, existing fabrication techniques like high-definition lithography and dry etching techniques can be used.

**Silicon-on-Insulator for Photonic Crystals**

Photonic ICs come in a wide variety of materials: polymers, glass, III-V semiconductors, silicon, etc. As photonic crystals need a high refractive index contrast, semiconductor is the preferred candidate. For the experiments with deep UV lithography we chose silicon-on-insulator (SOI). This is a layer structure consisting of a silicon wafer with a layer of silica ($SiO_2$) buried under a thin layer of silicon. This material has multiple advantages. It is transparent at wavelengths around 1550nm, and the top Si layer acts as an optical waveguide because of the large index contrast between Si (n=3.5) and $SiO_2$ (n=1.45).

Another factor in our material choice was the availability of SOI as 200mm wafers compatible with the processing equipment at IMEC. We used standard Unibond wafers purchased from SOITEC, with a buried oxide of 400nm and a top silicon layer of 205nm.

**Deep UV Lithography**

SOI photonic crystals for 1550nm have typically periods of 400 to 500nm with hole sizes between 160nm and 300nm. Moreover, these structures need to be defined with an accuracy of tens of nanometres. For experimental purposes e-beam lithography (EBL) is best suited,because structures down to 50nm can be defined. However, the process is slow, taking hours for a not even very complex PIC.

For mass fabrication a parallel process is needed to print all patterns in a single lithography step. For larger structures, optical lithography at visible or near UV wavelengths has always been sufficient, but for photonic crystals the resolution falls short. The next generation of optical lithography uses excimer lasers with wavelengths of 248nm and 193nm. This makes it possible to fabricate certain isolated structures with dimensions below 100nm and and periodic structures, like photonic crystals, with periods down to 400nm [4].

For the experiments described further we used an ASML PAS 5500/300 deep UV stepper at 248nm. The stepper uses 200mm wafers and is attached to an automated wafer-processing track.

**Lithography of square lattices with overexposure**

PhCs for TE-polarisation generally consist of triangular lattices of holes, often with a large radius/pitch ratio (typically 0.3). Nevertheless, we did our first experiments with a CMOS process evaluation mask consisting of square lattices of holes of various size and pitch but with a radius/pitch ratio of 0.25 or smaller. To make superdense lattices similar to photonic crystals, we overexposed these structures to print the holes larger with the same pitch.

First tests with this mask showed promising results for lattices with pitches of 600nm down to 400nm, and we managed to make lattices with radius/pitch ratios of 0.25 to 0.35 with an adequate budget in lithography parameters like focus and exposure dose.

To transfer the resist patterns into the SOI we used a two-step dry etch technique, etching the top silicon and the oxide in separate reactors with different chemistry. The resulting holes have straight, smooth sidewalls in both the top silicon layer and the oxide layer, with no discernible discontinuities between the different layers.

**Lithography of triangular photonic crystals**

For further tests, a process evaluation mask for photonic crystal like structures was designed. This mask contains triangular lattices with various pitch and hole size, as well as photonic crystal designs taken from literature, where necessary adapted to the SOI layer structure [4,5]. We included waveguides of different lengths and widths, as well as waveguides with bends and coupled cavity waveguides.
Figure 1 shows a single line defect waveguide in a triangular photonic crystal waveguide with a pitch of 460nm and hole diameter of 290nm after etch.

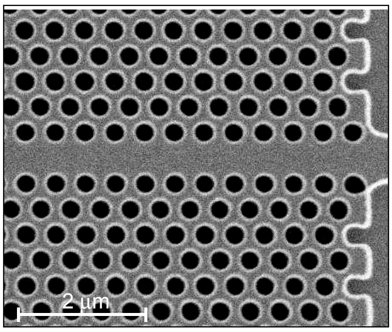


*Figure 1: Photonic crystal waveguide in SOI. Pitch is 460nm, hole-size is 290nm.*

To characterise the fabrication process, we have measured the hole diameter for a number of different photonic crystal lattices as a function of the exposure energy during lithography. Figure 2 shows the hole size for 5 different lattice parameters for exposure energies between 10 and 40mJ. The curves show that a wide variety of hole sizes can be fabricated by changing the lithography conditions. Also, an adequate energy budget is available to print the holes correctly within a 5% margin.

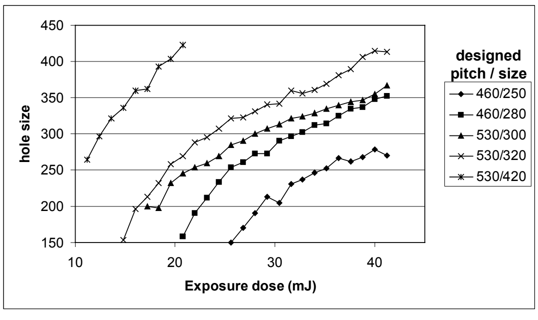


*Figure 2: Photonic crystal hole size after lithography and etch for different triangular lattice designs.*

**Further processing and measurements**

After lithography, the resist is baked and developed. The resist patterns are then transferred into the SOI with a two-stage dry etch process; the first stage for the top silicon layer, the second stage for the oxide.
Afterward the resist is stripped and the wafer is cut up into parts of about 3 by 3 cm$^2$. The substrate of these parts is then grinded back from 725µm to about 200µm. This allows us to cleave these parts into samples with two parallel cleaved facets.
Light is coupled in at the facet with a lensed fibre and the transmitted light is collected with an objective. The first measurements show transmission through the photonic crystal waveguides, as well as through waveguides with two 60° bends.

**Conclusions**

Our first experiments show that deep UV lithography definitely has the potential for the mass fabrication of ultra-compact photonic ICs based on photonic crystals. Lithography and etching experiments with photonic crystals in silicon-on-insulator showed well-defined holes with very little edge roughness. However, because of the differences between these structures and CMOS structures, existing fabrication techniques cannot be transferred directly. For lithography, different structures (like holes and lines) need different illumination conditions, and optical proximity effects for densely packed structures should be compensated at the mask design stage.
At the time of writing, the first few measurements showed transmission through photonic crystal waveguides and double 60° bends.

**Acknowledgements**

Part of this work was carried out in the context of the IST-PICCO project supported by the European Union.
Part of this work was carried out in the context of the Belgian IAP PHOTON network
Wim Bogaerts thanks the Flemish Institute for the industrial advancement of scientific and technological Research (IWT) for a specialisation grant.
The authors would like to thank Diziana Vangoidsenhoven for the wafer exposures, and Rudi de Ruyter and Johan Mees for their work on the mask design.

**References**

1 E. Yablonovitch, Phys. Rev. Lett. 58 (1987), 2059
2 T.F. Krauss et al., Nature 383(1996), 699
3 S.G. Johnson et al., Phys. Rev. B 60 (1999), 5751
4 M. Loncar et al., J. Lightw. Techn. 18(2000), 1402
5 S. Lin, et al., Opt. Lett. 25 (2000), 129