

Recent Progress in SOI Nanophotonic Waveguides

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Abstract Submicron Silicon wire waveguides allow realising extremely compact photonic ICs and can be fabricated in a cost-effective and reliable manner. We demonstrate basic waveguide functions and results for more complex WDM-devices.

Introduction

While state-of-the-art electronic circuits have unit dimensions between a few tens of nanometers to a few micrometers for their basic functional blocs, the dimensions of photonic devices are typically much larger, varying from a few micrometer (e.g. for the core of a single mode fiber) to several centimeter (e.g. for PLC-type AWGs). This huge size difference makes it in most cases not interesting to integrate electronics and photonics on a single substrate. To make optoelectronic integration more attractive there is a need for considerably more compact passive optical interconnect structures (waveguides, bends, splitters, combiners ...), more compact wavelength selective devices (high Q-resonators, highly dispersive elements) and more compact non-linear functions. Realizing this requires the use of ultra-high optical index contrast waveguides. In the past, so-called super-high- Δ planar lightwave circuits (PLC) have been presented, with a 1.5% index contrast between the silica cladding and the Germanium doped waveguide core [1]. However, the minimum acceptable bending radius in this material system is still 2 mm and therefore incompatible with tight optoelectronic integration. III-V based waveguides allow a bending radius from 500 μ m to a few tens of μ m and very compact devices have been presented for so called "deeply etched" waveguides, which were defined by etching completely through the high-index guiding layer and therefore show a very high lateral index contrast. However, when using a very small bending radius, light leaks out of the bend through the substrate because of the low vertical index contrast. To avoid this, also the vertical index contrast has to be increased. Such a high index contrast has been demonstrated in InP-based membrane type devices, GaAs/AlOx based devices and SOI-based devices, all of which consist of a thin high refractive index semiconductor core layer between low index cladding layers (dielectric or air) and allow for the realization of ultra-compact waveguide elements.

An additional problem of photonic devices however is the fact that they, for several reasons, often suffer from a low yield compared to their electronic counterparts, which makes optoelectronic integration not very appealing. Therefore it is important to adopt

as much as possible fabrication methods and tools used in the Silicon-based electronics industry. From this point of view, SOI-based devices show the most potential for integration with electronic devices and therefore form one of the most promising solutions for dense on-chip optical interconnects. These waveguides are typically fabricated starting from an SOI wafer, consisting of a Silicon substrate, a SiO₂ box layer (thickness t_{box}) and a Silicon guiding layer (thickness h). The waveguides are formed in this guiding layer. In some cases a SiO₂ cladding layer is deposited following the etch process. Figure 1 shows the basic waveguide structure. The most relevant parameters are the waveguide width w and the height h . Due to the extremely high index contrast, these will typically be limited to a few hundreds of nanometer for single mode waveguides.

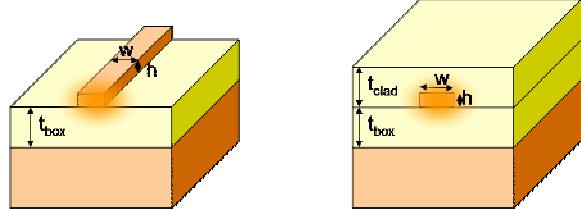


Figure 1 Basic waveguide structure

Basic properties

Basic structure and fabrication

Table 1 gives a review of publications discussing sub-micron Silicon strip waveguides, showing a strongly enhanced activity in this domain during the last few years. Two main categories of waveguide structures can be distinguished. Some groups are aiming to reach polarization independence by choosing the waveguide width equal to its height [9][13][15]. Most groups however opt for an asymmetric guide with a core height varying between 200nm and 340nm and a width varying from 400nm to 600nm. The latter is in most cases determined by the single mode condition. Fabrication in general starts from an SOI-wafer with the desired top-layer thickness. In most cases (see Table 1) the structures are defined using ebeam lithography, which allows for a fast turn-a-round but may not be compatible with mass-fabrication. We developed a technology based on 248nm DUV-illumination used also for the fabrication of advanced electronic ICs.

Aff.	Date	h [nm]	W [nm]	loss [dB/cm]	BOX [um]	top clad	Fab.	Ref.
IMEC/UGent	Apr. '04	220	500	2.4	1	no	DUV	[3][2][6][16]
IBM	Apr. '04	220	445	3.6	2	no	EBeam	[7]
Cornell	Aug. '03	270	470	5.0	3	no	EBeam	[8]
NTT	Feb. '05	300 200	300 400	7.8 2.8	3	yes	EBeam	[9]
Yokohama	Dec. '02	320	400	105.0	1	no	EBeam	[10][17][4]
MIT	Dec. '01	200	500	32.0	1	yes	G-line	[11]
LETI / LPM	Apr. '05	300 200	300 500	15.0 5.0	1	yes	DUV	[12][13]
Columbia	Oct. 03	260	600	110.0	1	Yes	EBeam	[14]
NEC	Oct. '04	300	300	19	1	Yes	EBeam	[15]

Table 1 Recent results on nano-photonic wire waveguides

Following illumination, the patterns are transferred directly into the Silicon using the resist as a mask. A detailed review of the processing steps can be found in [3]. Recently we started the development of a hard mask process, in which case the resist pattern is first transferred in a SiO₂ layer, which is subsequently used for etching the Silicon. Preliminary results are discussed below.

Losses

Reported losses for single mode waveguides vary from +100dB/cm to less than 3dB/cm (see Table 1). In [11] a 0.8dB/cm loss was reported. However, the dimensions of this waveguide were too small to strongly confine the light and this wire can no longer be considered as a high contrast waveguide.

The most relevant loss factors are fundamental material absorption (e.g. due to free carrier absorption), substrate leakage and scattering at interface roughness. The first two factors can be reduced to negligible values by respectively choosing sufficiently high resistivity wafers and a sufficiently high box layer thickness (see below). Reducing scattering losses requires careful process optimization to reduce sidewall roughness.

In literature, values varying from 11nm [10] to 2nm [7] have been reported for the roughness standard deviation resulting in a corresponding reduction in losses from over 100dB/cm to below 4dB/cm for single mode waveguides. Figure 2 shows the measured waveguide loss as function of waveguide width. The circles indicate the loss for the waveguides fabricated using the original process based on a resist mask, showing a 2.4 dB/cm loss for 500nm wide waveguides, which are single mode. The losses increase faster than expected with decreasing width however, suggesting that the magnitude of the roughness increases for smaller waveguides. The crosses show preliminary results for the hard mask based process. For wider waveguides the losses are higher than for the original process but they increase more slowly with decreasing width, indicating a different behavior for

the roughness. We believe an important part of the loss (1dB for 500nm width, >6dB for 400nm width [16]) is caused by leakage to the substrate due to the limited thickness t_{box} of the SiO₂ box layer in our devices (1μm). The other data points indicate some results published by several groups (box layer thickness for these results is shown in Table 1).

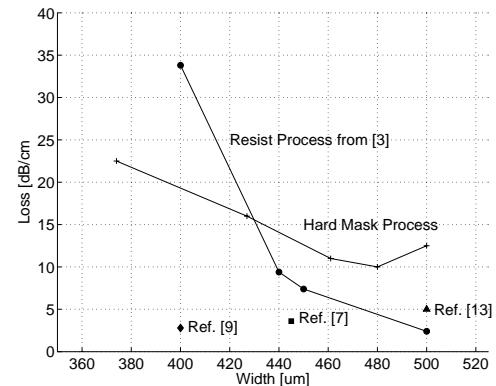


Figure 2 Measured waveguide losses as function of width

Bends

Obviously, one of the most attractive features offered by Silicon wire waveguides is the possibility for realizing an extremely short bending radius. In order to measure straight and bend losses accurately, we fabricated spiral-like structures with different total lengths and different number of 90 degree bends [2]. With a good choice of the samples in this parameter space, a reasonable fit of the propagation losses in straight wires and excess bend losses can be made. For 1, 2 and 3 μm radius, structures with a total length up to 25mm and up to 550 90 degree bends have been fabricated. For 5 μm radius, total length varied up to 50mm. The fitted excess bend loss includes the mode mismatch at the interfaces between straight and bent waveguides. The effect of this mode mismatch was separately characterized. Another possible source of bend loss is coupling to the TM mode, which is very lossy due to the limited thickness of the oxide undercladding. However, this effect is difficult to

quantify both experimentally and by simulation. Measurements show that for 5 μm radius, losses are completely dominated by the normal propagation losses. For 1 μm radius, excess bend losses dominate. Results for a 540nm wide wire are plotted in Figure 3 ($\lambda=1540\text{nm}$). Excess bend losses for 5 μm radius are smaller than 0.004 dB. These results agree well with experimental results reported in [7] and FDTD-simulations [17].

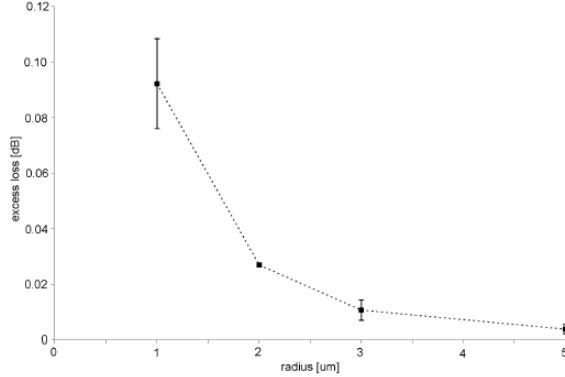


Figure 3 Measured bend losses for 540nm Silicon wire

Several authors have proposed and/or demonstrated corner-mirror and resonator based bend structures with the goal of further decreasing the bend loss and size. However, in view of the excellent results reported above for standard bend structures and taking into account the increased sensitivity to wavelength, polarization and side wall angle for the resonant structures, it is very unlikely that they will have any practical use.

Crossings

Low loss crossings showing negligible crosstalk form an important element in more complex PICs such as ROADM and crossconnects. However, since SOI-wires confine the optical mode to a very small cross-section we can expect large crosstalk and reflections due to diffraction at intersections. From 3D-FDTD simulations [4] the insertion loss and crosstalk were estimated to be 1.4dB and -9.2dB respectively, totally unacceptable for practical applications. To overcome this problem, we fabricated expanded mode crossings (inset Figure 4), which reduces the angular spectrum and therefore the diffraction angle. Figure 4 shows the measured loss for 2, 4 and 6 intersections and the crosstalk as function of wavelength. Loss was reduced to 0.65dB per intersection and the crosstalk to -30dB [2].

Fiber-chip couplers

Coupling light between fiber and chip is one of the most essential parts of the device and determines a huge fraction of the cost of the packaged device. Because of the extremely large mismatch, external mode adaptation is almost impossible for Silicon

wires and a solution with on-chip mode adapters has to be used. A good solution has to fulfill several requirements including broadband operation, low loss, low reflection, large alignment tolerance, good fabrication tolerance, compactness and should require only a limited number of extra processing steps and be compatible with "CMOS"-fabrication methods.

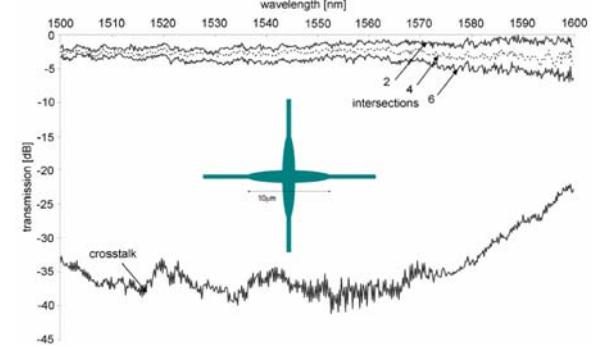


Figure 4 Normalised transmission spectrum of 2, 4 and 6 tapered intersections and crosstalk

The inverse taper approach has been demonstrated by several groups [7][8][9]. Over a length of a few tens to a few hundreds of micrometers the Silicon waveguide is narrowed down to a width below 100nm and the optical field is pushed upwards to a low index overlay. In most cases this overlay is patterned to form a single mode waveguide, which then is used to bring the optical mode to the edge of the chip. Using this approach low-loss broad band operation was demonstrated (<0.5dB per connection over range 1250nm to 1750nm in [7][9]). The loss is mainly determined by the taper tip width and its length and a compromise between acceptable loss and size has to be found.

All reported results thus far used ebeam-lithography to define the narrow taper tips. To demonstrate the compatibility of this approach with the DUV-illumination process, we defined narrow taper tips using an adapted process, which included a resist trimming step (Figure 5). Preliminary results show low loss coupling between the tapered waveguide and the polymer overlay.

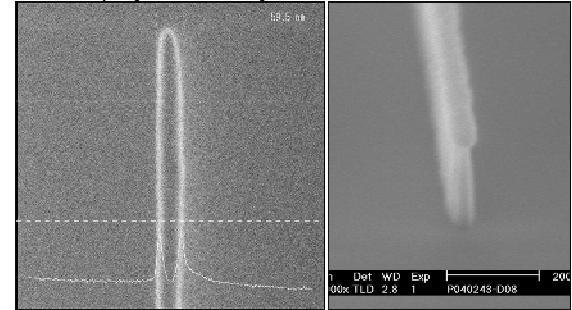


Figure 5 Sub 100nm wide taper tip for fibre-chip coupler defined using 248nm deep-UV litho

An alternative approach uses grating couplers for coupling the light between fiber and chip. Traditional

grating couplers use long, low index contrast gratings, resulting in narrow band operation. To overcome this we developed high-contrast fiber couplers, mode-matched to butt-coupled single mode fibers. The short interaction length increases the 3dB-bandwidth of the couplers to 60nm. A coupling efficiency of 33% has been demonstrated. Theoretically, the efficiency can be increased to 60% by using a non-uniform grating. By further adding a bottom reflector we simulated a coupling efficiency of 90% ([5], Figure 6). Compared to the inverse taper approach described above, the grating couplers show a reduced bandwidth. However, the alignment tolerances are better and the grating couplers allow for waferscale testing.

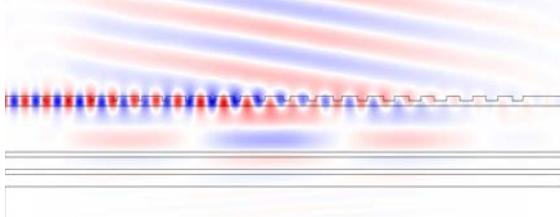


Figure 6 Simulated grating-coupler performance (90% to SMF)

Devices for WDM

Silica-on-Silicon AWGs (Arrayed Waveguide Grating) are currently the most popular integrated devices for multiplexing and demultiplexing multiple wavelength channels. We demonstrated an 8-channel AWG (Figure 7) with a footprint of 380 μ m x 290 μ m or about 0.1mm² [6]. The channel spacing was 3nm, the free spectral range 24nm. The measured on-chip insertion loss was approximately 8dB. We believe the loss was mainly caused by reflections in the star coupler and can be reduced by adapting the transition zone between the grating arms and the star coupler. The main problem is the high crosstalk level, limited to values around -7dB, which is clearly not sufficient for practical applications. Using an improved, low-loss star coupler design, we recently showed a reduction of the device insertion loss to values below 2dB and a considerable improvement of the crosstalk level.

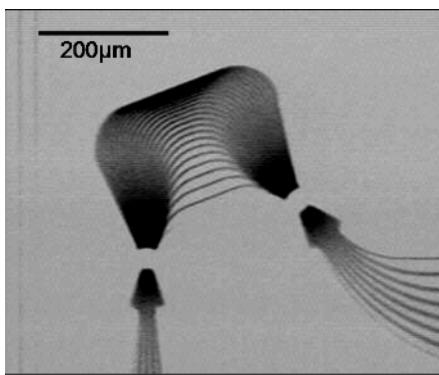


Figure 7 SOI-based AWG

Conclusion

As explained above, process optimization has led to a propagation loss reduction from over 100dB/cm to <3dB/cm for single mode Silicon strip waveguides. Despite this spectacular improvement, such losses are still much higher than those reported for silica-based waveguides [1]. However, while the dimensions of typical PLC-based devices are in the order of centimeters, dimensions of Silicon wire based devices have dimensions below 100 μ m, leading to total insertion losses per device that are comparable for both optical waveguide platforms. Some issues remain to be solved however. This includes the high sensitivity to processing deviations and phase noise induced crosstalk in WDM-devices.

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