NEW TECHNOLOGIES & DEVICE STRUCTURES

Silicon Nanophotonics

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Abstract

Silicon photonics builds on the momentum of silicon electronics to deliver to photonic integration what was lacking: a generic integration platform. Silicon-based nanophotonic ICs tremendously increase the integration scale, and the functionality per chip, compared with their counterparts in other material systems (glass, III-V semiconductor, etc.). This will drive adoption of photonic integration by a wide range of volume applications with increasing requirements in size, weight and power consumption.

Photonic ICs in Silicon-on-Insulator

Today photonic integration suffers from an extreme diversity in materials, processes and integration approaches. Convergence on a generic platform with a select set of processes and industry-standard tools can overcome this bottleneck.[1] As silicon is an excellent material for passive optics in the infrared, the use of CMOS processes for photonic ICs is obviously attractive.

Industrial "off-the-shelf" CMOS processes can be used for a variety of photonic devices, as young companies such as Luxtera and Lightwire have been demonstrating in the U.S. Their multi-channel transceivers for optical interconnect and datacom are made with CMOS foundry processes applied in a clever way. Meanwhile, IMEC and CEA-LETI have been developing processes to support a wider range of photonic circuits: To meet the stringent alignment requirements of photonic circuits, both the isolated and very dense structures in nanophotonic circuits have to be patterned simultaneously.[2]

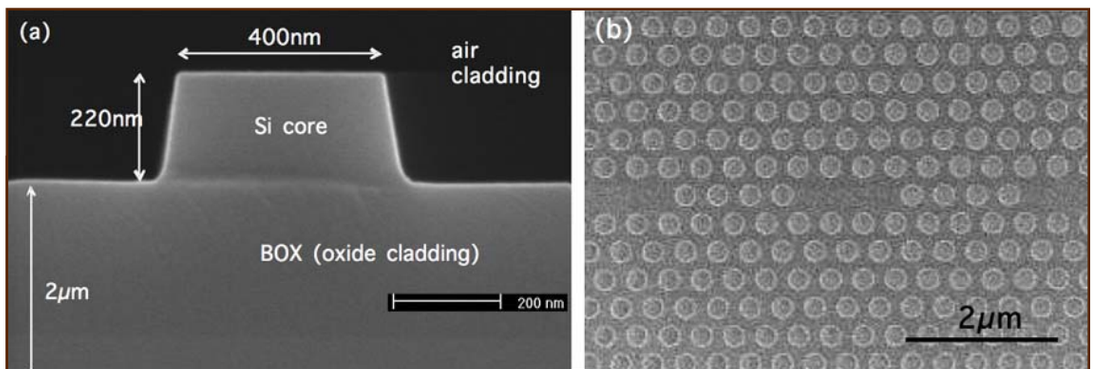

Figure 1. (a) high-index contrast strip waveguide in SOI
(b) photonic crystal (pitch 440nm) with cavity confining the optical mode in a 2 x 0.5µm² area.

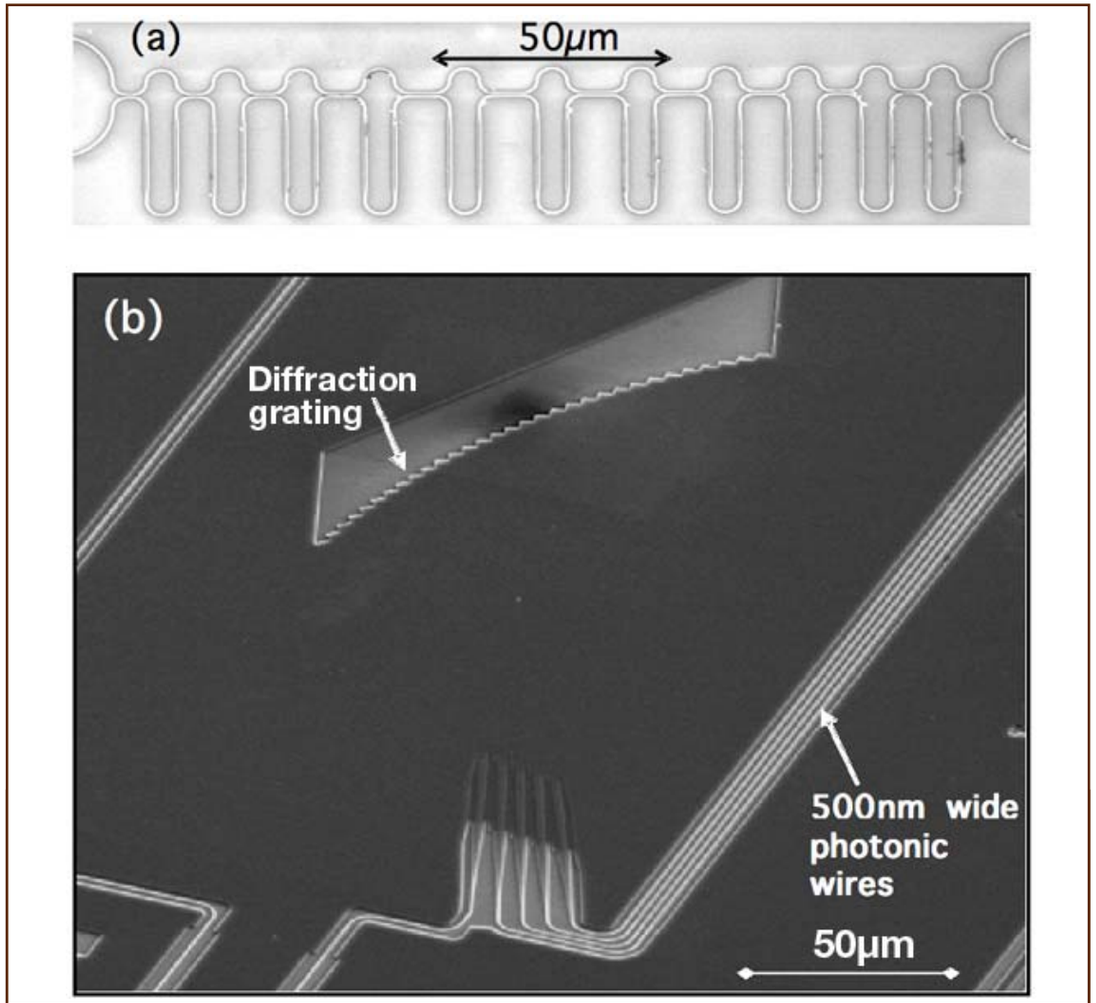

Figure 2. Compact wavelength-selective devices in SOI
(a) WDM channel selector based on a lattice filter with a 0.02 mm² footprint [3]
(b) WDM demux based on a diffraction grating [4]

Strong Light Confinement

To create a dielectric waveguide for light, a core is defined in a high refractive index material surrounded by cladding with a lower index. With semiconductor for the core (n≈3.5) and an oxide or air (n≈1-1.5) as the cladding, light can be bound to a submicron strip waveguide, as shown in Figure 1. The optical mode is strongly confined in a cross section comparable to the light's wavelength in the material. Because of this, the optical path can be steered on a much smaller footprint compared with other material systems. Bends of just a few micron radius, compact splitters, wavelength-scale cavities with high-quality resonances (Figure 1) and strong nonlinear effects enable very compact circuits. The integration scale can be up to six orders larger than that of glass-based components. As an example, a WDM channel selector with a 0.01mm^2 footprint is shown in Figure 2, together with a wavelength demultiplexer smaller than 0.02mm^2.

The Need for Extreme Accuracy

The typical critical dimensions (CD) of the silicon waveguides are in the 100–500nm range. However, nanometer-scale deviations can limit the device performance due to losses, reflections and crosstalk. The alignment tolerance between waveguide elements is of the order of a few nanometers at best, so most patterns within a single circuit layer need to be printed in the same lithographic step. To complicate matters, waveguide circuits consist of diverse features, from (semi-)isolated lines all the way to ultradense arrays of holes. The generic processes needed to support this wide range of features have been developed on CMOS tools at institutes like IMEC over the last decade. As the layer-to-layer alignment accuracy of scanners is improving towards the 5nm-level, double exposure techniques now start to reach the tolerance requirement of a number of photonic devices, opening opportunities to further optimize the fabrication processes.

One of the most striking requirements of silicon photonics is the extreme accuracy on the critical dimensions: While 100–500nm feature sizes are fairly large for today's high-end CMOS tools, an accuracy of 1 percent or better is needed. In fact, within a single wavelength-selective device, CD control of even 1nm or better is needed. While CD variations can be compensated for by thermo-optic or electro-optic tuning, an accurate base technology is needed to keep the power consumption low and the compensation algorithms simple. IMEC is now at a stage where wafer-level uniformity is controlled within less than 1 percent (1σ) for 450nm-wide waveguides, with even better uniformity within a single die. This accuracy requirement also poses significant metrology challenges. Still, sub-nm deviations which are impossible to measure with SEM can be assessed accurately through optical device characterization.

Recycling Old Fabs and Processes?

The accuracy requirements show that silicon photonics cannot just "recycle an old fab," but need cutting-edge technology. Additionally, the smaller the allowed minimum CD, the wider the range of possible devices and applications. Still, technology from the 0.18µm or 0.13µm CMOS nodes already deliver many possibilities for silicon photonic circuit designers, with standard 193nm DUV lithography being the key necessity. While existing tools and fabs can be used, novel processes are needed to support the diversity of features, and to ensure a sufficient scalability both in technology and in applications.

Applications

First products are entering the market now with waveguide mode sizes smaller than 1µm^2. For the data communication market, Luxtera has developed multichannel transceivers, in the process setting up a complete tool chain from CMOS-compatible design libraries all the way to packaging and testing. They integrate photonic circuits with electronics for control, tuning and drivers, and run the processing through a fab from Freescale. Elsewhere, basic and applied research is targeting communication applications such as fiber-to-the-home, short-range interconnects/datacom and all-optical signal processing. Within two years, other companies can be expected to develop prototypes and enter the market with products based on even smaller mode sizes, with corresponding larger-scale integration. Key in driving these developments is the integration of silicon photonic ICs with SiGe for detection and modulation, and with III-Vs for light generation and signal processing.

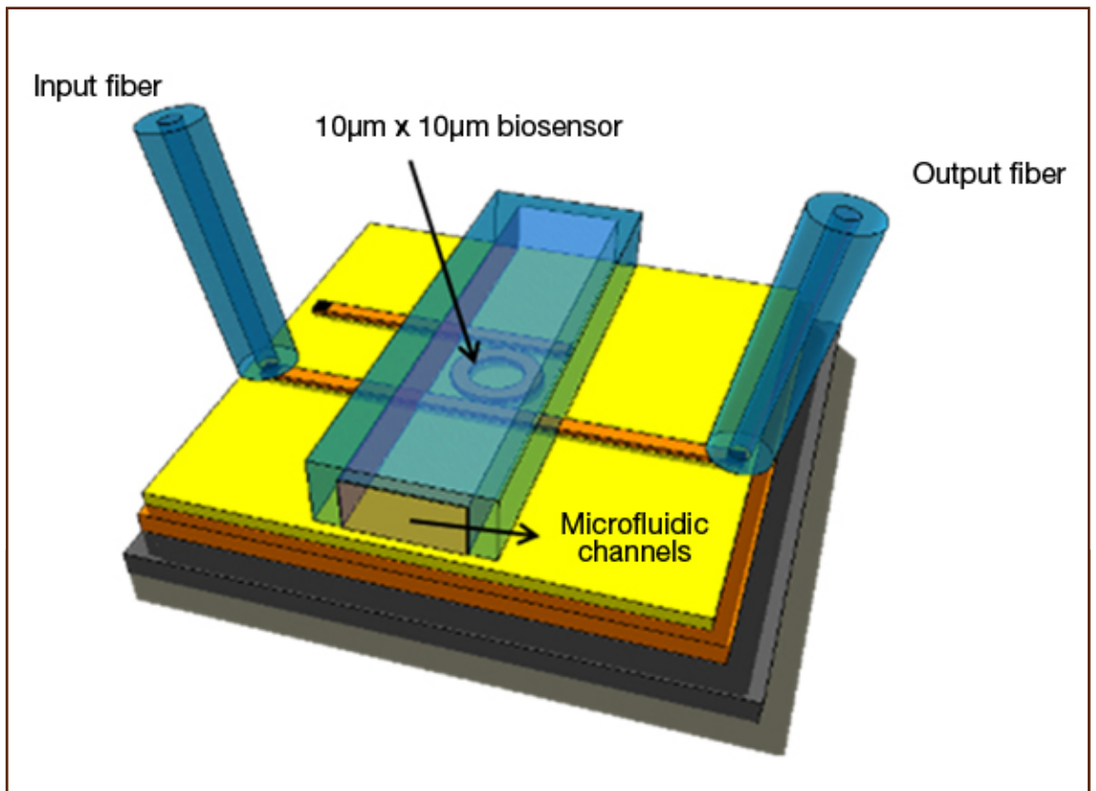

Figure 3. Label-free biosensor concept based on optical resonators. Thousands of functionalized biosensors can be integrated on a single chip.

Light can also be used as a sensing instrument, either directly or indirectly, and waveguide circuits for this purpose are the focus of many research teams. For instance, a highly integrated silicon photonic IC could serve as a multiparameter sensor for infrastructure monitoring, even equipped with on-chip logic for data processing. Ultracompact label-free biosensor chips, as illustrated in Figure 3, can easily contain hundreds of sensors for different substances or sensitivity ranges. Throw in on-chip communication capabilities and data processing logic and you have a very powerful mix.

Active-Passive Integration

As in electronics, silicon is not the holy grail of materials, but it offers an immensely attractive integration platform. For light detection at telecom wavelengths, SiGe or III-V materials need to be integrated,[6,7] either monolithically or heterogeneously. Similar integration efforts are needed for light amplification and generation. Die-to-wafer bonding approaches for heterogeneous integration of III-V sources and detectors with silicon circuits have been extensively studied over the last years, and significant research efforts are directed towards wafer-scale processing of III-V bonded material in CMOS lines. Pioneering work of IMEC and CEA-LETI has already shown that these can be viable technologies.[5,6]

Hundreds of multi-Gbit/s transceivers can be integrated on a single chip, e.g., for use in access networks and high-performance computing. Integration with active and nonlinear materials enables complex all-optical signal processing, such as wavelength conversion, switching and optical buffering. A possible route towards this is the sandwiched waveguide technology developed by CEA-LETI. Dramatically improved high-speed interconnect solutions will be needed in the next decade for box-to-box down to on-chip data communication, to address the ever-growing memory and processor bandwidth requirements. Both Intel and IBM have projects on multicore processors with terabit/s on-chip bandwidth requirements, which can be powered by silicon photonics. An example of such on-chip optical interconnects from the PICMOS project [5] is shown in Figure 4.

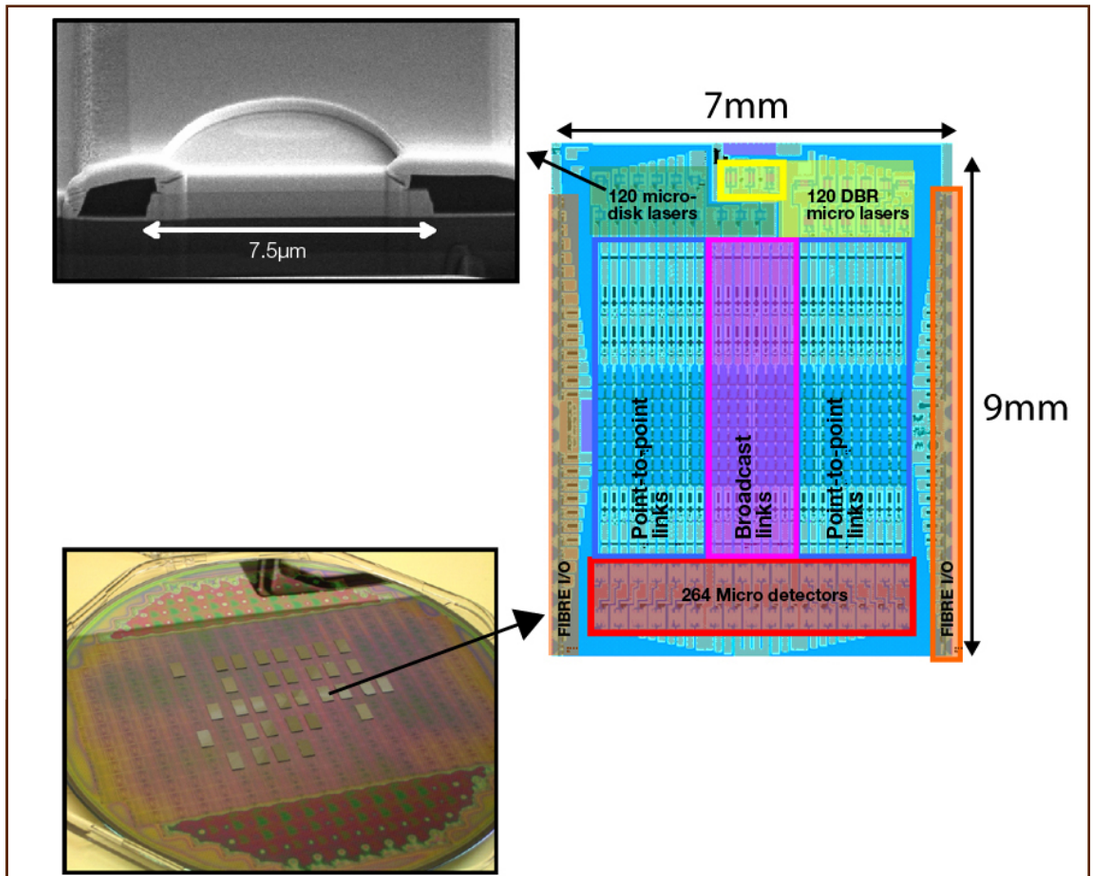

Figure 4. On-chip optical interconnects with Si photonic circuits form the EC-funded FP6 PICMOS project [5] III-V microsources and microdetectors. Sources and detectors are integrated by die-to-wafer bonding. The demonstrator contains point-to-point as well as broadcast links. Microdisk lasers, DBR microlasers and microdetectors are processed in the thin-film III-V after bonding and III-V substrate removal.

Integration With CMOS

As silicon photonics is working on the same platform as CMOS, why not integrate with CMOS? Transmitters and detectors can then be directly integrated with their driver circuits and logic. Or labs-on-a-chip can have the optical sensors, ADC, logic and external connectivity all on board. Of course, the most direct application of integration with CMOS is for optical interconnects as previously described.

However, it is currently unclear which of the many integration approaches is best for each application. The impact of manufacturability, yield, thermal properties and raw device performance is either unknown today or depends very much on the application. The possible approaches can mainly be classified in front-end, back-end and 3D integration (separate electronic and photonic ICs). In the industrial examples, Luxtera integrates photonics and electronics on the same chip in the front end, while Lightwire keeps them on separate chips, though both make clever use of CMOS technology. In contrast, both IMEC and CEA-LETI have developed low-loss amorphous silicon films deposited with (low-temperature) PECVD, compatible with back-end integration.[8,9] Interesting times are ahead.

Part II: From Research to the Market

The first start-ups in silicon are delivering their first products. However, a tremendous amount of research is bringing in new applications and better-performing devices. In the next issue, we will discuss how the gap between the research and the market can be bridged, as well as how the ePIXnet silicon photonics platform organizes affordable prototyping for this purpose.

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Pieter Dumon obtained his Master in Electrical Engineering degree from Ghent University in 2002. He obtained his Doctorate in Electrical Engineering degree in 2007, also from Ghent University. Pieter now coordinates the ePIXnet silicon photonics platform at IMEC, Dept. of Information Technology, in the Photonics Research Group, which gives access to the CMOS facilities at IMEC (B) and CEA-LETI (F) for wafer-scale research and prototyping of silicon photonic components. He is a member of the IEEE and the OSA.

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Wim Bogaerts started in silicon photonics at Ghent University-IMEC in 1999. He developed CMOS-compatible processes for nanophotonic circuits, with a Ph.D. in 2004. He is currently a postdoctoral fellow of the Flemish Research Foundation, and member of IEEE-LEOS and OSA.

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Jean-Marc Fedeli

Jean-Marc Fedeli acts at CEA-LETI since 2002 as coordinator of silicon photonic projects with a focus on 200 mm fabrication technology. He has been working on different European projects (PICMOS, PHOLOGIC, MNTE, ePIXnet) for the development of photonic layer on top of an electronic integrated circuit.

Roel Baets

Roel Baets received the degree in electrical engineering from Ghent University, Belgium (1980), M.Sc. in electrical engineering from Stanford University (1981) and his Ph.D. degree from Ghent University in 1984. He leads the Photonics Research Group at Ghent University-INTEC (associated lab of IMEC), which focuses on new concepts for photonic components and circuits. Currently he coordinates the European Network of Excellence ePIXnet. Roel is a Fellow of the IEEE and from 2003 to 2005 was an elected member of the Board of Governors of IEEE-LEOS.