Compact Demultiplexer Using Cascaded Planar Concave Grating and Ring Resonators on SOI

Gunay Yurtsever, Joost Brouckaert, Wim Bogaerts, Pieter Dumon, Dries Van Thourhout and Roel Baets

Ghent University – IMEC, Photonics Research Group, Department of Information Technology (INTEC) , Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium
gunay@intec.ugent.be

Abstract

We present a compact demultiplexer based on cascaded planar concave grating and ring resonators. The demultiplexer has 28 channels, with 1 nm channel spacing. The device was fabricated on a silicon-on-insulator (SOI) platform using CMOS compatible deep UV lithography. The size of the structure is 1.5 x 3 mm. Insertion loss is 15 dB, channel to channel variation is 5 dB

I. INTRODUCTION

High resolution multichannel demultiplexers are crucial for telecom and spectroscopic applications. Integrated optical demultiplexers are advantageous for mass production, dense output channels and integration with other optical components. Such demultiplexers have been implemented mainly as array waveguide gratings (AWGs) and planar concave gratings (PCGs). Using silica on silicon a planar concave grating with 256 channel, 0.2 nm channel spacing has been demonstrated [1]. AWG with similar properties on silica has also been fabricated by NTT Electronics (personal communication). Such devices can also be designed for high index contrast material systems such as silicon on insulator, reducing the size of the device almost by two decades. However, the dramatic decrease in the size makes the components sensitive to fabrication related random errors. With the current technology and processes for SOI, AWGs are limited to free spectral range of 50 nm with 1.6nm channel spacing, while PCGs can have more than 100 nm free spectral range but performance degrades for channel spacing less than 3.2 nm. Narrow spectral filters with 0.2 nm 3dB bandwidth can be implemented on SOI using ring resonators if sufficiently small FSR is chosen. In this article, we demonstrate for the first time on SOI, that using cascaded PCG and ring resonators high resolution demultiplexer with large FSR is feasible.

II. DESIGN AND FABRICATION

The demultiplexers consists of a PCG with 5 channels separated by 7 nm. The output of each channel has 11 ring resonators in series. The design of the PCG is based on the Rowland geometry, where the 7 μm input waveguide and the 2 μm output waveguides are located on a circle with a radius of 1.3mm. Both input and output waveguides are etched shallower (70nm) and tapered adiabatically to 450nm deep etched (220 nm) waveguides. The grating facets are second order distributed Bragg reflectors, individually blazed for 10^{th} order diffraction [2]. The ring resonators have 3dB bandwidth of 0.3 nm. FSRs are ranging from 10.8 – 10.9 nm, with radii changing from 7.6-7.7 μm and 2 μm long straight sections separated from the waveguides by 200 nm gap. The free spectral ranges are sufficiently large to obtain -35dB isolation between the adjacent peaks of the rings. Only the rings that have peaks within -4dB bandwidth of the lobes are utilized, and almost haft of the channels are not used. As result effective channel spacing is

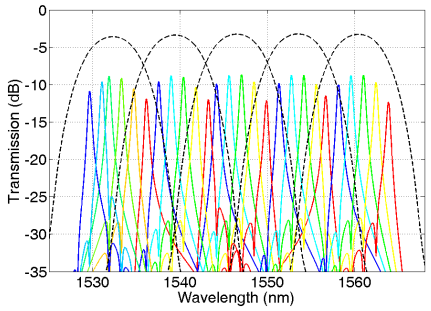

Figure 1. Simulated spectral response of the of the PCG (dashed lines) and the demultiplexer (solid lines).

978-1-4244-3681-1/09/$25.00 ©2009 IEEE

1.4 nm. Simulation of the demultiplexer response is shown in Figure 1.

The devices are fabricated on a 200 mm SOI wafer with 220 nm thick Si top layer on top of 2 µm thick SiO_2 using 193nm deep-UV lithography in combination with ICP-RIE etching [2]. The fabrication was done through ePIXfab silicon photonics platform (www.epixfab.eu) The fabricated demultiplexer is shown in Figure 2.

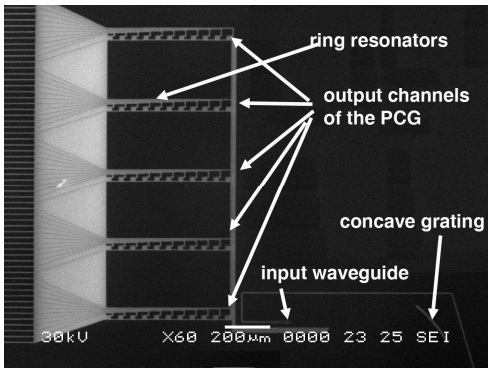

Figure 2. Scanning electron microscope image the demultiplexer.

III. MEASUREMENT RESULTS

The response of each channel has been measured with a broadband source which was coupled in and out of the chip using grating couplers. The spectral response of the device is given in Figure 3. The insertion loss varies between -10 dB and -17.5 dB, which is in accordance with the simulation results. The non-uniformity of the channels can be attributed to sensitivity of the coupling coefficient of the ring resonators to small deviation in gap and waveguide thicknesses of the rings [3].

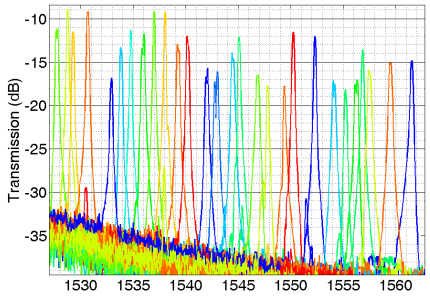

Figure 3. Measured spectral response of the demultiplexer.

The channel spacing is quite uniform around 1 nm. The 3dB bandwidths of the peaks range between 0.2 – 0.4 nm. Rings with smaller 3dB bandwidths are also feasible , however splitting of the resonance peak should be taken into account. 28 out of the 55 channels has been used, discarding the ones with high insertion loss, overlapping peak, and high side lobes. The device can be potentially used in spectrum analysis, and variation in the channels can be compensated from the apriori characterization or active tuning.

IV. CONCLUSIONS

We have demonstrated a very compact high resolution demultiplexer fabricated using CMOS process compatible deep UV lithography. Despite of sensitivity to fabrication errors, cascaded PCG and microring resonators bring advantages of both sides and offer a small size, low cost demultiplexer solution.

ACKNOWLEDGMENTS

Part of this work has been supported by Methusalem Program, funded by the Flemish Government

REFERENCES

[1] S. Janz et al., “Planar waveguide echelle gratings in silica-on-silicon,” *IEEE Photon. Technol. Lett.*, vol. 16, no. 2, pp. 503–505, Feb. 2004

[2] J. Brouckaert *et al*., "Planar Concave Grating Demultiplexer with High Reflective Bragg Reflector Facets," *Photonics Technology Letters,* vol. 20, pp. 309-311, 2008.

[3]JM Lee et al., “Multichannel silicon WDM ring filters fabricated with DUV lithography”, Optics Communications, vol. 281:17, pp 4302-4306, 2008.