SOI thickness uniformity improvement using corrective etching for silicon nano-photonic device

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Abstract: We present our recent results on Si thickness uniformity improvement in a SOI wafer. We improved the thickness uniformity by 50%. The effect of the correction process on the propagation loss and device uniformity is also presented.

I. Introduction

High-index contrast silicon nano-photonic devices are very sensitive to small dimensional variations. The change in device dimension results in the shift of the spectral response, which is not acceptable in most applications. The change in the device dimension is mainly caused by two physical factors, firstly, the thickness or the height of the device and secondly the width of the device. The later is related to patterning process, optical lithography and dry etching process, while the former is directly related to the thickness control of the wafer fabrication process. In our previous work [1], we have shown that good device uniformity can be achieved by using high resolution patterning process uniform. The effect of thickness variation, however, by and large, depends on the wafer manufacturing process. It has been shown by many that thickness variation is one of the dominant effects compared to width variation [2]. Hence addressing this issue is ever more important than now, as silicon photonic is moving toward a mass manufacturing environment.

In this paper, we present our recent work on Si-thickness uniformity improvement of SOI wafer. We use Gas Cluster Ion Beam location specific process [3] to correct the existing non-uniformity of a virgin wafer to achieved highly uniform thickness over a 200 mm wafer. Furthermore, we studied the effect of the correction process on the propagation loss and uniformity of the wavelength selective device.

II. Corrective etch process

Gas Cluster Ion Beam (GCIB) process generates highly concentrated reactive ion beam, which can accurately process a specific location on the surface. The localized process can be deposition, etching or doping. This localized process mechanism provides GCIB an unique opportunities in many applications. Figure 1 shows the schematic of a simple GCIB generation system. Firstly, atom and molecule clusters are formed by forcing the gas through a nozzle. Then the accelerated beam is formed to desired shape and focused on to the wafer surface. The energy and acceleration of the ions are controlled during the acceleration and beam forming process. When a cluster of ions reaches the surface they instantaneously react with a smaller volume of target material on the surface, which may either form volatile produce or non-volatile produce resulting in a sputtering or deposition process respectively.

In this work, we use fluorine based ion beam generation from CHF_3 gas to etch a predetermined thickness of Si from a SOI wafer. In the following section, we elaborate the procedure adopted to reduce non-uniformity of Si thickness in a 200 mm SOI wafer.

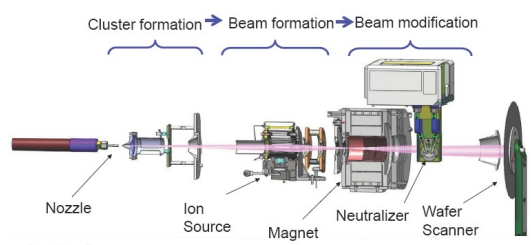

Fig. 1.Schematic of a GCIB system.

III. Experiment

A. Thickness uniformity improvement

A typical Si thickness non-uniformity over a 200 mm SOI wafer is ~10%. For example, in a 220nm thick Si device layer one can expect a thickness variation of ±22nm. This variation is mainly due to wafer manufacturing process technology. Even though the non-uniformity is improving over time as a result of improved manufacturing process the specifications are far for the strict requirement of integrated Si photonic devices.

The corrective etch process is done in the following sequence,

1. Firstly, the thickness map of the top silicon layer of the virgin wafer is generated by using spectroscopic ellipsometry. In our case,

we used 361 points over a 200 mm to capture a detailed map.

2. Based on the thickness map a corrective etch map is generated based on the target thickness.
3. Based on the correction map the etch process is applied on the wafer.
4. Finally, a dense 361 point corrected thickness map is collected again to access the uniformity after the correction process.

Figure 2a&b shows the thickness map of Si before and after a corrective etch process. And Table I show the measurement statistics. Based on the uncorrected thickness data we chose a target Si thickness of 200 nm. Since the correction process can only remove the material the target thickness has to be less than the minimum thickness (<218.95 nm) on the wafers. We used TEL Epion Ultra-Trimmer® system for the corrective etch process. The corrective etch was done using CHF_3 gas targeting a final thickness of 200 nm. The etch process was optimized to reduce physical and chemical damage to the Si surface.

The effect of corrective etch can be clearly seen from the wafer map in Fig. 2b and Table I. The mean thickness shows the accuracy of the optimized correction process used. We also clearly observe a substantial improvement in the thickness uniformity. The thickness non-uniformity (3σ) over a 200mm wafer has been improved from 6.08 % to 2.13 %. Similarly, we observed 53 % reduction in the wafer range.

TABLE I
WITHIN WAFER THICKNESS STATISTICS
361 POINT MEASUREMENT OVER A 200 MM SOI WAFER

	Before trimming	After trimming
Mean (nm)	219.45	199.82
Max(nm)	235.66	205.21
Min (nm)	214.98	194.23
Range (nm)	20.68	10.93
3σ (%)	5.7	2.7

B. *Optical test devices and fabrication process*

In order to evaluate the material damage and uniformity of the devices, we used two types of test devices. Firstly, we used 450 nm wide single mode spiral waveguides with varying length (1, 2, 4 and 7 cm) to assess the damage created through propagation loss. In the same layer, we implemented two identical racetrack ring notch filter to study device uniformity. The resonators were formed by a racetrack ring with a bend radius of 5 µm and a straight section of 4 µm separated by a gap of 180 nm from the bus waveguide. Both the ring and bus waveguide width was kept at 450 nm. The filter was place 25 µm apart, which can be used to study the short range uniformity.

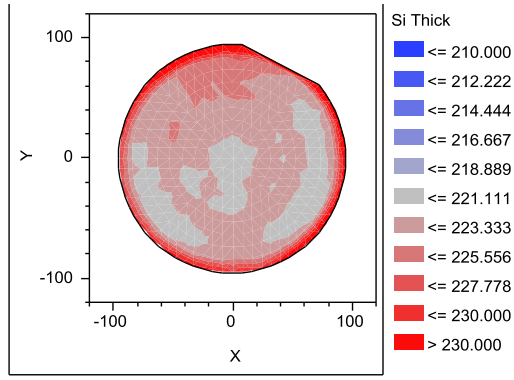

Fig. 2a. Thickness map before corrective etch.

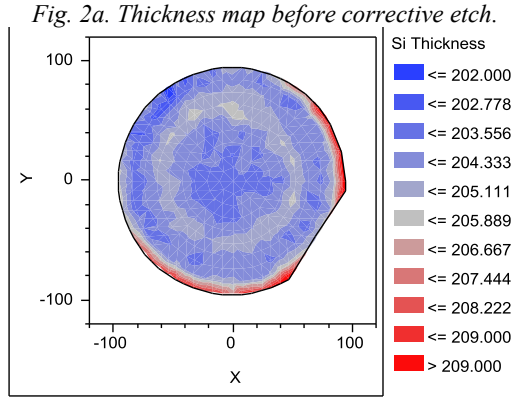

Fig. 2b. Thickness map after corrective etch.

The devices were fabricated in the SOI wafer which went through the corrective etch process where the top Si thickness was 200 nm on top of 2000 nm buried oxide layer. The fabrication was done in a CMOS pilot line at *imec*, Leuven, Belgium. We used an optimized 193nm optical lithography and dry etch process as described in [4] to obtain highly uniform devices within a die and over the wafer. Multiple dies were printed over the wafer with identical optical lithography process yielding nominally identical dies/chips.

IV. OPTICAL CHARACTERIZATION AND DISCUSSION

The fabricated devices were optically characterized by coupling in TE polarized light from a broadband light source and measuring the output from the device through an optical spectrum analyzer. For in- and out-coupling we used shallow etch grating coupler [5].

The propagation loss of the photonic wire was measured by cutback method, where the transmission spectrum of the wires with varying length was collected and the propagation loss was extracted by linear regression. We measured a propagation loss of ~50dB/cm for TE polarized light (Fig. 3). This

exceptionally high loss can be attributed to surface absorption and scattering loss. It is well known that ion beam process such as the one used here damages the surface both physically and chemically. As the ion beam is scanned over the wafer the top surface is amorphousized initially, and then volatile product is removed from the surface. This amorphousized layer can be as deep as 10 nm and rich in dangling bonds which absorbs light. Even though the process was carefully designed to reduce such damage optical loss was still high.

Since the correction process is done at the very beginning of the fabrication process the wafers enjoy process temperature freedom. Hence the defects can be cured at high temperatures. We annealed some of the dies at 900°C in nitrogen atmosphere for 30 minutes. After annealing the waveguides showed a substantial reduction in the propagation loss (Fig.3). The loss has come down to 5 dB/cm, which is an order of magnitude reduction. This reduction in the propagation loss can be attributed to curing of surface defects created during the corrective etch process. The main form of the defect curing process is recrystallization of the amorphousized Si surface.

Figure 4 shows our preliminary inter and intra die device uniformity. Three nominally identical dies were chosen from the wafer each containing two ring resonators. The dies were picked from location sufficiently far apart (~100 mm) in order to capture the non-uniformity over long distance range. The transmission spectrum of the rings shows good uniformity. We measured an inter-die non-uniformity range (λ_{resMax}-λ_{resMin}) of 1.8±0.12 nm and an average intra-die non-uniformity of 0.2 nm, which shows that the device uniformity within a short distance scale is better than the global variation attributing to global variation such as the thickness and dry etch process.

Even though the data points are limited the statistics clearly indicated that the long range non uniformity has shown improvement compared to our previous uncorrected uniformity presented in [1].

However, this promising result requires further extensive full wafer characterization to extract and correlate device and dimensional non-uniformity, which is our focus of study at the moment. Furthermore, in addition of thermal annealing in N_2 atmosphere other annealed atmospheres are also being investigated.

V. Summary

We have demonstrated Si thickness uniformity improvement using GCIB corrective etch process. The uniformity of a virgin 200 mm SOI wafer was improved by 50 %. The damage created during the corrective etch is cured by thermal annealing by which the loss was reduced from 50 dB/cm to 5 dB/cm. We have achieved a short range (intra die) non-uniformity of ~0.2 nm and long range (inter die) non-uniformity of ~1.8 nm.

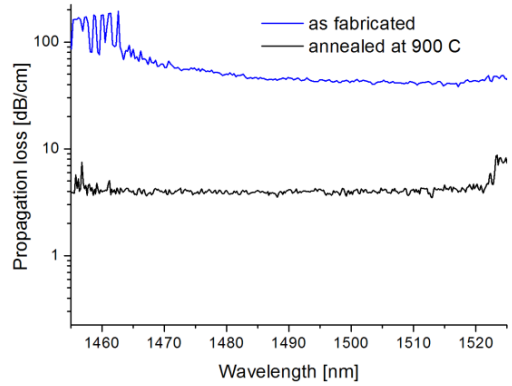

Fig. 3.Propagation loss spectrum of a 450 nm photonic wire.

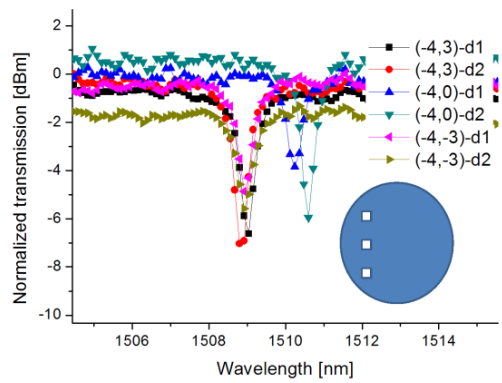

Fig. 4. Spectral response of ring filter from 3 nominally identical dies. Inset shows the location of dies in the 200mm wafer..

References

[1] S. K. Selvaraja, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Subnanometer Linewidth Uniformity in Silicon Nanophotonic Waveguide Devices Using CMOS Fabrication Technology," *IEEE J. Sel. Top. Quantum Electron.,* vol. 16, pp. 316-324, 2010.

[2] W. A. Zortman, D. C. Trotter, and M. R. Watts, "Silicon photonics manufacturing," *Opt. Express,* vol. 18, pp. 23598-23607, Nov 8 2010.

[3] I. Yamada, J. Matsuo, N. Toyoda, and C. R. C. C. Ion, "Cluster ion beam process technology," *Nucl. Instrum. Methods Phys. Res., Sect. B,* vol. 206, pp. 820-829, May 2003.

[4] S. K. Selvaraja, P. Jaenen, W. Bogaerts, D. Van Thourhout, P. Dumon, and R. G. Baets, "Fabrication of Photonic Wire and Crystal Circuits in Silicon-on-Insulator Using 193-nm Optical Lithography," *J. Lightwave Technol,* vol. 27, pp. 4076-4083, 2009.

[5] D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, and R. Baets, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," *Jpn. J. Appl. Phys., Part 1,* vol. 45, pp. 6071-6077, Aug 2006.