A highly efficient electrically pumped optical amplifier integrated on a SOI waveguide circuit

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Abstract— **A heterogeneously integrated III-V-on-silicon optical amplifier utilizing an ultra-thin DVS-BCB die-to-wafer bonding process is reported. A novel design exploiting high confinement in the active waveguide is demonstrated showing low power consumption operation. 13dB on-chip gain is achieved for 40mA drive current at room temperature.**

Keywords-component; III-V-on-silicon amplifier; heterogeneous integration; adhesive bonding

I. INTRODUCTION

Silicon-On-Insulator (SOI) is gaining interest as a novel platform for integrated optical circuits, since its large refractive index contrast allows for ultra-compact devices. The interest in this technology stems however mostly from the expectation that the maturity and low cost of CMOS-technology can be applied for advanced photonics products. However, the integration of a silicon amplifier and laser is hampered by silicon's indirect bandgap. Building light sources, and in particular optical amplifiers and laser sources, on integrated silicon circuits is a big challenge. In that sense the heterogeneous integration of III-V/silicon amplifiers takes the best of two worlds. In order to densely integrate the III–V semiconductors with the silicon waveguide circuits, mainly DVS-BCB adhesive wafer bonding and molecular bonding techniques are used and are actively reported in state-of-the-art hybrid amplifiers [1] and lasers [2]. In these approaches, unstructured InP dies are bonded, epitaxial layers down, on a SOI waveguide circuit wafer, after which the InP growth substrate is removed and the III–V epitaxial film is processed. The design space for hybrid InP/SOI devices is large and in particular the coupling between the optical mode in the top active III–V waveguide and that in the bottom passive SOI waveguide plays an important role. In literature, two main solutions are reported. In the first one, based on evanescent coupling, the bulk of the optical mode (~70%) in the III-V/silicon amplifier waveguide is confined within the Si waveguide [1-2]. Typically, the silicon waveguide thickness is larger than 500nm and the III–V effective waveguide width is large (> 4μm). Such thick silicon waveguides are difficult to integrate with most high-performance modulator designs, which have usually a thickness of less than 400nm [3]. In the second type of devices, the optical mode is mostly confined in the III-V material. In this case, coupling between the III–V and silicon waveguide is realized by adiabatically tapering the silicon and III-V waveguide [4]. This requires that the thickness of the bonding layer is thin enough (<100nm) to have high coupling efficiency. Achieving such thin bonding layers that are uniform over the full bonding area presents a great technological challenge.

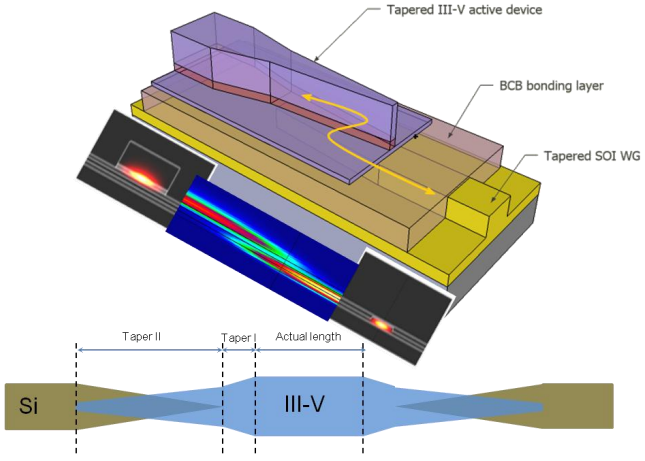

Figure 1. (a) Three-dimensional view of the coupling structure of the hybrid amplifier with representative mode profiles in two cross-sections; (b) the detailed top view of the the hybrid amplifier.

This paper reports on a hybrid amplifier fabricated using DVS-BCB bonding presenting several new features: narrow III–V waveguides in the range from 2 to 3μm, thin silicon

waveguide thickness (400nm/220nm) and an adiabatic taper in both the III–V and silicon waveguide. These new features lead to 13dB on-chip gain for 40mA drive current at room temperature.

II. Device Configuration

A bonded structure of an InGaAsP quantum well p-i-n diode layer stack and a silicon waveguide forms the heterogeneously integrated amplifier. The III–V region consists of a p-InGaAs contact layer, a p-InP cladding layer, 6 InGaAsP quantum wells (6nm) surrounded by two InGaAsP separate confinement heterostructure (SCH) layers (100nm), and an n-InP layer (200nm). The SOI substrate (200 mm wafer manufactured by SOITEC) is composed of a 400 nm mono-crystalline silicon layer on top of a 2µm thick buried oxide layer on a silicon substrate. The silicon rib waveguides have a height of 400nm and an etch depth of 180nm. The III-V membrane layer is bonded onto the silicon waveguide circuit using an adhesive BCB die-to-wafer bonding approach [5]. The bonding layer thickness is around 40nm. The device structure is schematically outlined in figure 1. The structure can be divided into three parts. In the center of the device there is a III-V waveguide that provides optical gain, at both sides of this section there is an adiabatic inverted taper coupler for high efficiency and large optical bandwidth coupling between the silicon waveguide layer and the III-V membrane layer. After the coupling region the light is guided by a silicon waveguide to a fiber-to-chip grating coupler defined in a 220nm thick silicon waveguide using a low-loss 400nm to 220nm waveguide transition. In the adiabatic taper section, the width of the III-V mesa is tapered from 900nm to 500nm, while the silicon rib waveguide underneath is tapered from 300nm to 1µm over a length of 100µm. The III-V mesa width is tapered more abruptly from 2µm (3µm) to 900nm over 20µm (30µm).

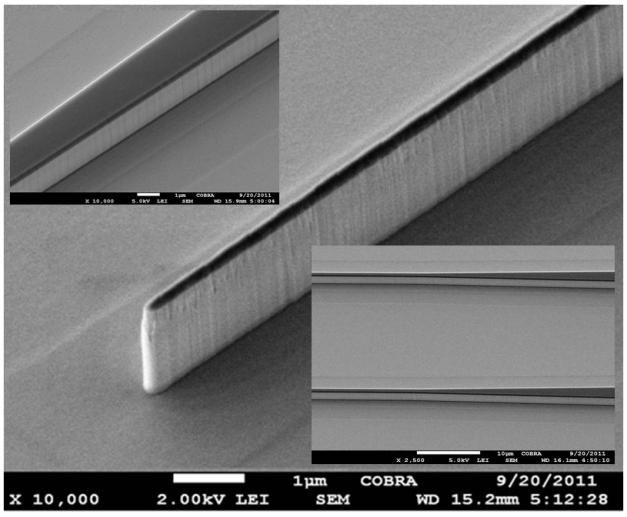

Figure 2. SEM picture of a III–V waveguide and taper tip.

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III. Device Fabrication

After bonding and removing the InP substrate, the masking layers for the III-V waveguides, 600nm SiNx deposited by plasma-enhanced chemical vapor deposition (PECVD) and then a 50nm Cr layer, are evaporated. The Cr layer allows to do e-beam lithography (EBL) patterning required for the III-V waveguides and narrow taper structures. A 320nm thick ZEP e-beam resist is applied and the III-V waveguide patterns are written with a Raith 150-Two, using predefined markers on the SOI waveguide circuit. The waveguide pattern is transferred into the Cr layer by Cl_2:O_2 inductively coupled plasma (ICP) etching. The Cr layer serves then as an etching mask to open the 600nm thick SiNx layer in a CHF_3 RIE process. ICP etching by CH_4:H_2 was used to etch through the InGaAs layer and etch the InP p-doped layer. The MQW layer was etched by chemical selective etching to stop on n-InP. Fig. 3 shows a scanning electron microscope (SEM) picture of the III–V taper. The active waveguide is then encapsulated with DVS-BCB. A Ti/Pt/Au alloy was used for metallization on both p and n sides.

IV. Experiments and Results

The device gain is measured by launching and collecting the signal through tilted vertical fibers at both the input and output grating couplers. Polarization control is used to excite the TE mode in the silicon waveguide circuit. The gain for different bias currents was measured by changing the input wavelength with 2nm step, keeping 1mW power. The output signal was filtered by a bandpass filter for amplified spontaneous emission (ASE) suppression. By comparing the signal transmission through the device with the transmission through a reference silicon waveguide, the gain (Si waveguide to Si waveguide) in the III–V amplifier can be extracted. Fig. 3 shows the measured TE small-signal fiber-to-fiber transmission for an optical amplifier with a 3µm wide mesa, 200µm length and two times 100µm taper length as a function of drive current, together with the transmission through a reference waveguide. Fig. 4 shows the extracted gain spectra for the amplifier. The maximum gain occurs at 1560nm with a spectral full width at half maximum of 70nm at 40mA.

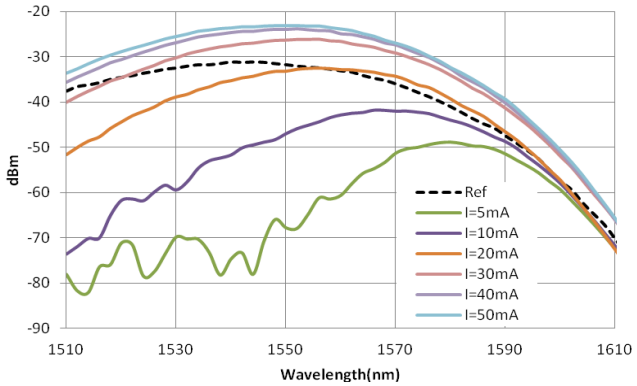


Figure 3. Fiber-to-fiber transmission versus drive current and a reference transmission spectrum.

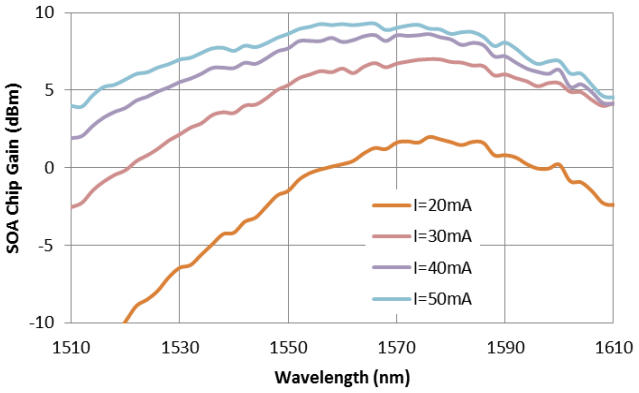


Figure 4. Amplifier gain versus wavelength for different current levels for a 200µm long amplifier with a width of 3µm and 100µm taper length.

Fig. 5 shows the gain spectra for an amplifier with a 2µm wide mesa, 400µm length and two times 100µm taper length. A maximum chip gain of 13dB is obtained at 1560nm for 40mA drivecurrent.

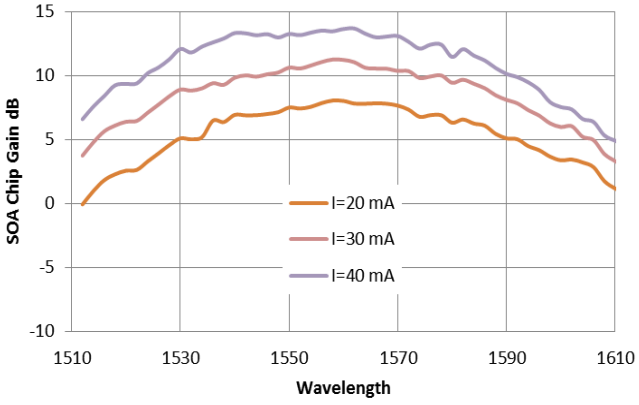
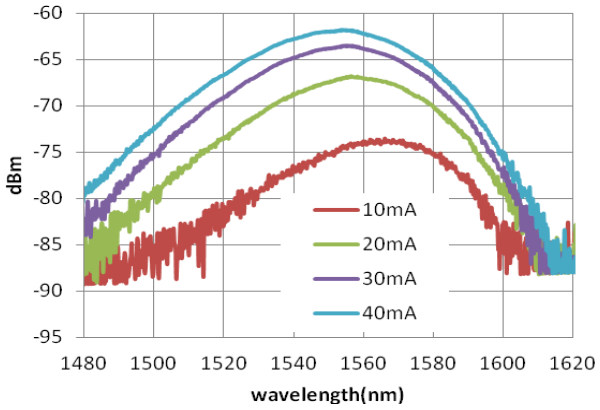


Figure 5. Amplifier gain versus wavelength for different current levels for an amplifier with 400µm length, 2µm width and 100µm taper length

The ASE spectra from the amplifier are shown for four different drive currents in Fig. 6 for both devices (recorded with 50pm resolution). No ripples (<0.05dB at 40mA) in the ASE spectrum can be observed, implying that the parasitic reflections at the III-V tip/SOI waveguide interface is very low, which is attributed to the narrow III-V tip defined by e-beam lithography.

V. CONCLUSIONS

A new concept was proposed for the realization of III-V-on-silicon hybrid amplifiers, providing high optical confinement in the III-V waveguide layer, while the passive photonics elements are implemented in the silicon on a 220nm/400nm platform. High optical gain at low drive currents was obtained. This is an important step towards a CMOS-compatible optical amplifier for optical interconnects. This gain section can now also be implemented to realize more complex laser geometries with gain provided by the III-V mesa while the wavelength selective feedback is implemented in the silicon waveguide layer.



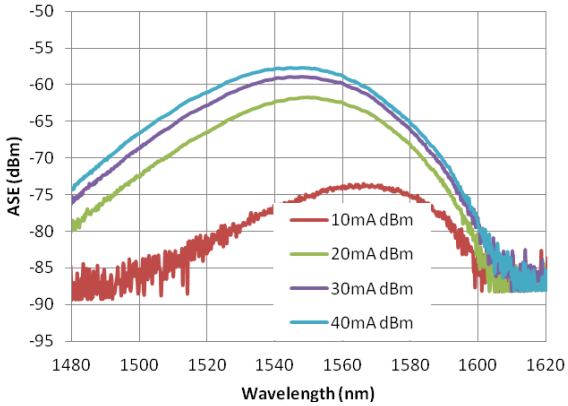


Figure 6. ASE spectra of the amplifier for different applied currents (a) amplifier with 200µm length, 3µm width and 100µm taper length (b) amplifier with 400µm length, 2µm width and 100µm taper length

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