Photonics Design with an EDA approach: Validation of Layout Waveguide Interconnects

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***Abstract*—This work demonstrates the use of commercial EDA toolsets for the measurement and validation of the layout of waveguide interconnects and the integration into a dedicated silicon photonics physical design flow.**

Tremendous progress has been made on development of silicon photonics building blocks, but the next challenge will be the realization of more complex systems that include many devices and are integrated within complex CMOS mixed electro-optical circuits [1] [2]. Seamless integration of photonic integrated circuit (PIC) technology into existing silicon platforms requires a design flow that is compatible with current electronic design automation (EDA) tool suites. However, due to differences in the physics between photonic and electronic circuits, a dedicated methodology for PIC design automation must be developed to enable technology integration. At the physical verification stage, design rule checking (DRC) and layout versus schematic (LVS) comparisons are the two required assessments that must be passed to obtain permission from the foundry for fabrication. Designs that are non-compliant with DRC and LVS will not meet manufacturing and performance targets. As such, foundries prohibit the shipping of these designs for production.

In this paper, we address a key missing feature in PIC functional verification – the validation of layout waveguide interconnect designs. If we compare the photonic components that perform the manipulation of light (coupling, splitting, amplification, modulation, etc.) to devices in electronic design, then the waveguide that connects these components is the equivalent of metal wires. It is well-established in the EDA flow that LVS performs connectivity checks on those wires for potential shorts or open circuit, by comparing the layout-extracted netlist to the original design netlist (known as the source netlist). Unlike electronic ICs, where connectivity is defined by the touch/overlap of the wire design geometries, the optical signal integrity in waveguide interconnects is dependent on more geometrical factors, such as path length, width, and bend curvature [3]. Photonic designers must meticulously design their waveguide routes, carefully considering the proper propagation of optical modes along the waveguide, to avoid optical open circuits, or rather scatter points or reflection points. There is a similar stage in the IC verification flow where layout measurements of wire path length and width are performed on wire geometry for the purpose of parasitic resistance and capacitance extraction. However, waveguide interconnect validation differs in two respects: 1)earlier flow integration is required, because the geometrical parameters of a waveguide interconnect must be considered to be not only simulation parameters for the post-layout analysis of parasitic side effects, but must also be validated to avoid fatal circuit failure, 2) a different extraction methodology must be employed, due to the lack of existing algorithms for curvilinear parameter computation.

I. Methodology

A. Waveguide Interconnect Parameter Validation

As layout waveguide interconnect geometry must be validated for human errors that easily lead to optical signal discontinuity, design reference values such as interconnect width, path length, and minimum curvature value must be specified for comparison to the layout geometry parameters. The validation process has several essential requirements: 1) waveguide interconnect recognition, 2) a programmable engine to apply customized computation algorithms, 3) validation of the waveguide with extracted layout parameters against reference values.

To fulfill these requirements, we adapted the Calibre® PERC™ tool process flow to this PIC-specific validation. It is a reliability verification and analysis platform for physical layout and logical netlist information. It was used to implement programmable electrical rule checking (ERC), electrostatic discharge (ESD) and latchup checking, as well as more general geometry measurements based on topology selection and logical circuit analysis [4]. It is Tcl-based that allows user-programmable topological analysis and algorithm insertion. Based on these features, we implement the flow for waveguide interconnect verification and it is depicted in Fig. 1(a).

Within this flow, a source netlist analysis is first performed and waveguide interconnect objects are exported, which are then mapped to layout geometries and measured for critical parameters such as width, path length, and minimum radius of curvature (RoC). Those values are verified against the references with user-defined criteria – ie. width must be close to a certain value for proper mode propagation, minimum RoC and path length must be above threshold values to ensure acceptable bend loss and propagation, etc. In addition to those checks, the extracted values can also be annotated back into the

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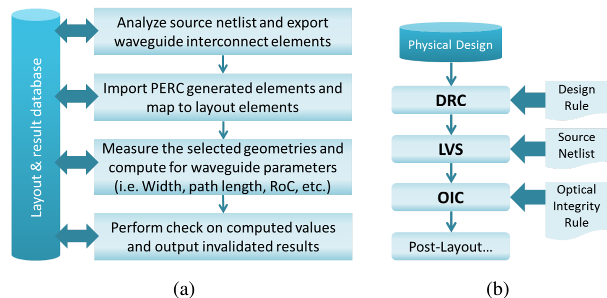


(a) (b)

Fig. 1: (a) Waveguide parameter validation realized using Calibre® PERC™. (b) The proposed physical verification flow.

netlist for further simulation purposes. In this way, waveguide interconnect quality is secured by correct geometrical design.

B. Flow Integration

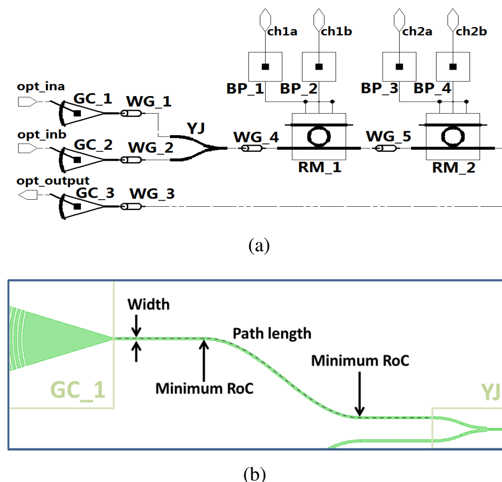
We propose a physical verification flow that integrates the verification methodology classified as the optical integrity checking (OIC) (Fig. 1(b)). The physical design is first validated for manufacturability using DRC. LVS is then performed to verify device placement and parameters, as well as basic connectivity, by comparison with the reference schematic design. OIC performs checks that further verify geometrical parameters of the layout waveguide interconnect to prevent optical signal discontinuity. It includes rule for topology analysis and selection, algorithms for geometrical measurement, and error output criteria, which are Tcl-scripted. Design errors at any one of these steps must be corrected and looped back to the beginning of the process before sending the design to post-layout simulations and further layout correction steps.

II. Experiments & Results

We demonstrate the methodology based on a generic process design kit (PDK) [1]. A schematic design of a PIC is shown in Fig. 2(a), containing device building blocks of grating couplers (GC), Y-junctions (YJ), ring modulators (RM), bond pads (BP), and waveguide interconnects (WG) (which are inserted into the source design as redundant devices only for property attachment). Layout design is then conducted accordingly.

The proposed physical verification flow is applied to the design. In addition to DRC for fabrication rule compliance, and device placement and connectivity accordance guaranteed by LVS, OIC is performed to check for signal discontinuity due to a bad geometrical design of a waveguide interconnect. Connectivity failure can happen even after LVS-clean, where the interconnect is simply defined as a touch in design geometry. With the proposed methodology, we flexibly cross-reference the netlist scan to the design geometries of the waveguide interconnect, and perform specific geometrical measurement checks. In our example, we measure the width using existing DRC functions, as well as path length and minimum RoC using the programmable engine that allows integration of user-defined computation algorithms (Fig. 2(b)). Then they are compared with reference values, and a threshold for the value

[1]The technology kit is provided through the SiEPIC program and is publicly available at http://siepic.ubc.ca/GSiP



(a)

(b)

Fig. 2: (a) Schematic design of a photonic integrated circuit. (b) Layout waveguide interconnect on which key parameters as width, path length, and minimum RoC are extracted.

deviation is specified to control error reporting. In this way, we are able to accept/refuse each layout waveguide interconnect according to our specification.

III. Conclusion & Future Work

OIC is proposed as an essential step for optical signal integrity checking for layout waveguide interconnects. By using a programmable ERC framework, we can recognize interconnect geometry based on topology selection, and integrate user-programmable measurements and checks. Such a framework complements traditional LVS with tailored checks on waveguide interconnects, in which the design geometry parameter can determine circuit yield. The complementary work to this study is to clearly define the signal integrity criteria (technology-dependent), as well as explore other potential factors affecting optical signal integrity.

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References

[1] L. Vivien, Ed., *Handbook of silicon photonics*, ser. Series in optics and optoelectronics. CRC Press, Taylor & Francis Group, 2013.

[2] J. Buckwalter, X. Zheng, G. Li, K. Raj, and A. Krishnamoorthy, "A monolithic 25-gb/s transceiver with photonic ring modulators and ge detectors in a 130-nm cmos soi process," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 6, pp. 1309–1322, June 2012.

[3] Y. A. Vlasov and S. J. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," *Optics Express*, vol. 12, no. 8, pp. 1622–1631, Apr. 2004.

[4] K. Kollu, T. Jackson, F. Kharas, and A. Adke, "Unifying design data during verification: Implementing logic-driven layout analysis and debug," in *IC Design Technology (ICICDT), 2012 IEEE International Conference on*, May 2012, pp. 1–5.

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