Expanding the Silicon Photonics Portfolio With Silicon Nitride Photonic Integrated Circuits

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***Abstract*—The high index contrast silicon-on-insulator platform is the dominant CMOS compatible platform for photonic integration. The successful use of silicon photonic chips in optical communication applications has now paved the way for new areas where photonic chips can be applied. It is already emerging as a competing technology for sensing and spectroscopic applications. This increasing range of applications for silicon photonics instigates an interest in exploring new materials, as silicon-on-insulator has some drawbacks for these emerging applications, e.g., silicon is not transparent in the visible wavelength range. Silicon nitride is an alternate material platform. It has moderately high index contrast, and like silicon-on-insulator, it uses CMOS processes to manufacture photonic integrated circuits. In this paper, the advantages and challenges associated with these two material platforms are discussed. The case of dispersive spectrometers, which are widely used in various silicon photonic applications, is presented for these two material platforms.**

***Index Terms*—Photonic integration, silicon nitride, silicon-on-insulator, silicon photonics.**

I. Introduction

PHOTONIC integration has made tremendous progress in the last few years. Large-scale monolithic integration of complex photonic functions is a reality now [1]–[5]. The range of applications has broadened from long-haul telecommunication [6], [7] to short-reach data communication [8], [9] and from optical coherence tomography [7], [10] to lab-on-a-chip systems [11], [12]. Unlike electronic integration, photonic integrated circuits have been based on a plethora of material platforms [4], [5], [13]–[15], each platform having its own advantages and challenges.

In the last 15 years, silicon photonics has established itself as an important photonic integration platform [16]. It has made its way from research labs to manufacturing foundries [2]–[4] and ultimately to the market. It may be described as a technology that uses a high index contrast material platform for wafer-scale fabrication of high-density and low-cost Photonic Integrated Circuits (PICs) in a CMOS[1] fab delivering high yield.

The success of silicon photonics can be attributed to two main features. First, leveraging existing CMOS infrastructure [17] for the fabrication of silicon photonic chips has turned out to be the major driver for the growth of this field. It allows the fabrication of high, moderate and low volumes of silicon photonic chips in existing CMOS fabs that are primarily loaded with the fabrication of electronic ICs. For prototyping, typically executed by means of Multi-Project Wafer (MPW) services to deliver a small number of chips, the cost per chip is of the order of 100 to 1000 US Dollars [18]. But for manufacturing this cost will rapidly drive down by a factor of 100 or so even for moderate volume. Such a scenario circumvents huge financial investment and risk involved in building a dedicated fab for photonic integration only. Second, a paramount attribute to the success of silicon photonics is the use of a high index contrast material platform for the implementation of PICs. This feature ensures the implementation of complex optical functions while keeping the chip form factor small, resulting in more chips per wafer. Furthermore, the high index contrast allows the implementation of functions such as photonic crystal cavities [19]–[21] and high-efficiency grating couplers [22], [23] that are difficult or simply not possible to implement in a low-index contrast material platform.

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[1]CMOS compatibility has many meanings. For the sake of this paper CMOS compatibility means that the process flow for the fabrication of photonic integrated circuits can be executed with the typical technology toolbox found in a CMOS fab or pilot line, without major modifications. Hence it is not meant to imply compatibility with CMOS electronic circuitry.

In [24] a comparison of Silicon-on-Insulator (SOI) and Silicon Nitride (SiN) platforms is provided. This paper provides a more detailed discussion on the aspects already published in [24]. In section II, a description of the two silicon photonic platforms is provided. Section III provides a comparison of SOI and SiN-based silicon photonics by highlighting their strengths and challenges. In section IV, the two material platforms are compared qualitatively by looking at the specific case of dispersive optical spectrometers realized in the two platforms.

II. Silicon Photonics Platforms

SOI is currently the mainstream and predominantly used material platform for silicon photonic devices. Its layer stack comprises a thin layer of crystalline silicon, which is separated from the silicon substrate by a buried oxide (BOX) layer. SOI wafers with a 0.22 μm silicon guiding layer and 2 μm BOX is the pseudo standard used for SOI-based silicon photonics. However recently thicker silicon layers of 0.31 μm [25] and 0.4 μm [26] are also getting prominence due to the ease of heterogeneous III-V laser integration on these waveguide circuits. The high index contrast of about 2 between the guiding silicon layer (n $\sim$ 3.5) and the BOX (n $\sim$ 1.45) allows for a tight bending radius of 5 μm (for 0.45 μm wide strip waveguides operating at 1.55 μm). This enables flexibility in the layout of complex and highly integrated photonic circuits. In its basic form SOI-based silicon photonics provides passive components such as waveguides, splitters, wavelength filters, interferometers, resonators, polarization management devices and couplers to guide light in and out of the silicon chip [22], [27]–[29]. In its more advanced form, it provides advanced photonic functions such as high speed (40 Gb/s and beyond) modulators and monolithically integrated detectors [2]–[4]. Moreover, the high thermo-optic coefficient of silicon is exploited for realizing tunable filters [30], tuning of fabrication-induced errors [31] for interferometric devices and for low-speed switching operations [32]. Low-cost access to SOI-based silicon photonics is commercially available through the MPW services offered by various CMOS pilot lines [18] and foundries [2], [3].

SOI has undoubtedly shown impressive performance for passive and active functions on a photonic integrated chip in the last few years. Some of the test bed demonstrations using SOI-based silicon photonics in research labs have made their way to products, which is a very promising sign for SOI-based silicon photonics. The high index contrast of SOI not only makes it superior, due to the reasons mentioned above, to other photonic integrated material platforms, but also makes it a challenging material platform. It demands nm-scale precision in fabrication to achieve high performance components. Moreover, the success of silicon photonics has opened new avenues for applications, e.g. in wavelength regimes where silicon or the buried oxide of SOI is no longer transparent. The above mentioned reasons cause an increasing interest to explore alternate material platforms which still possess relatively high index contrast and are CMOS compatible to enable high-density photonic integration. SiN is emerging as an important candidate in this context [33]–[37].

SiN is a commonly used material in CMOS foundries for masking, passivation, and strain engineering [38]. The material stack used for SiN-based silicon photonics is similar to SOI-based silicon photonics. The only difference is that the guiding silicon layer is replaced by a layer of SiN, which can either be deposited by Low Pressure Chemical Vapour Deposition (LPCVD) at high temperature ($>700\,^{\circ}$C) or by Plasma Enhanced Chemical Vapour Deposition (PECVD) at low temperature ($<400\,^{\circ}$C). LPCVD-based SiN is typically close to stoichiometric Si_3N_4. However, it has large internal tensile stress [39]. For integrated non-linear optics using SiN, thicker SiN layers are desired to enhance the confinement of optical mode in the waveguide and tune the waveguide dispersion. Thick SiN LPCVD layers can be deposited by increasing the silicon content in SiN (the so called Silicon rich SiN) [40], by using the thermal cycling process [39] or by using the Damascene process [41]. These types of waveguides are beyond the scope of this paper.

LPCVD SiN provides an excellent control over the homogeneity of material index and thickness. It has a refractive index of $\sim$2 at a wavelength of 1.55 μm. PECVD-based nitride has a composition that depends strongly on the deposition conditions and can be silicon-rich (higher refractive index) or nitrogen-rich (lower refractive index). Both types of nitride have been used for photonic ICs. In the telecom band around 1.55 μm it is common to use LPCVD nitride to avoid the absorption due to N-H and Si-H bonds around 1.52 μm [42]. To this end the LPCVD nitride is annealed at high temperature to drive out the hydrogen. This high temperature annealing process makes the co-integration of LPCVD SiN with CMOS electronics challenging. Fig. 1(a) and (b) show the refractive index and absorption coefficient of typical LPCVD and PECVD silicon nitride for wavelengths ranging 0.4 μm to 1.68 μm [43].

SiN-based silicon photonics provides a valuable alternative to mitigate the challenges associated with SOI-based silicon photonics by providing a compromise between footprint and performance of the photonic integrated devices. Currently the MPW access to SiN-based silicon photonics is provided by LioniX using their trademark material platform called TriPleX [44]. It uses LPCVD SiN to provide passive photonic integrated components and very low loss waveguides. Due to the growing interest in this new material platform, CMOS pilot lines now also envision to offer MPW services for SiN-based silicon photonics [45].

III. Silicon Nitride vs SOI-Based Silicon Photonics

A material platform needs to have a range of characteristics to be effective for photonic integration. This includes a wide transparency range, the ability to provide low loss components, allowing for high integration density, the realization of high-performance active and passive components and unique material properties to implement novel devices. In the next sub-sections a comparison is provided on the basis of the above mentioned attributes for the SOI and SiN material platforms.

A. Transparency Range

The transparency range determines the potential application domains of a material platform. The SOI platform is transparent between 1.1 μm and 4 μm [46]. The lower limit of this range results from the band gap of silicon. Below 1.1 μm silicon can

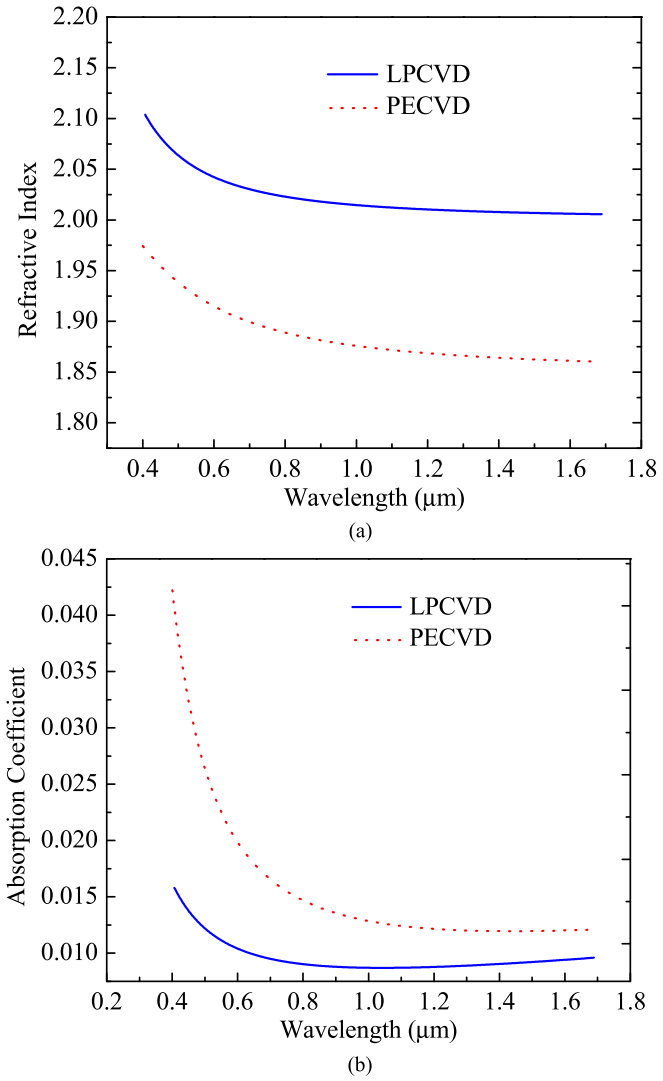

Fig. 1. Refractive index (top) [43] and absorption coefficient (bottom) of typical LPCVD (blue) and PECVD (dotted red) SiN for the visible and IR wavelength regime.

be used for photodetection, but is no longer useful for guiding and manipulation of light. Silicon itself is transparent up to 8 μm [46] but the upper limit of the transparency window of the SOI platform is dictated by the absorption of the silica BOX layer. Beyond $\sim$4 μm there is a sharp onset of mid-IR absorption [47] in silica. By under-etching the BOX to make free-standing silicon structures, the transparency range of SOI may be stretched to the transparency range of silicon [48].

In the wavelength range of $\sim$1.26 μm to $\sim$1.63 μm, SOI has predominantly been used to demonstrate components for short and long haul communication systems. Amongst others these include wavelength filters for WDM systems [49], [50] and high-speed transceivers [6], [8]. However, spectroscopic and sensing applications [12] have also been targeted. For wavelengths in the short-wave IR and mid-IR (>2 μm), silicon-based components have been demonstrated for gas and liquid spectroscopy, which have strong and characteristic absorption peaks in this band [51]. Non-linear photonic functions such as parametric amplification [52] and wavelength conversion [53] have also been demonstrated in the mid-IR and short-wave IR, because of the reduced nonlinear absorption here.

The transparency window of the SiN platform is extended to the visible wavelength range (0.4 μm). Similar to the SOI platform, the upper limit of the transparency window is determined by the BOX absorption, picking up at $\sim$4 μm. The visible and near IR transparency of the SiN platform enables many applications in life sciences. Here, the advantages are minimal photo damage to living cells and negligible water absorption. Moreover, the availability of low-cost sources and detectors makes the SiN platform a viable platform for on-chip spectroscopic analysis of biological media. This has led to demonstrations of spectroscopic functions [48], [54], Raman spectroscopy-on-chip functions [55]–[57] and integration with colloidal quantum dots emitting in the visible [58]. On top of that, the SiN platform has also demonstrated high-performance passive components for optical telecommunication, microwave photonics and biomedical applications [59]–[61].

B. Index Contrast

The index contrast between the guiding and cladding layer influences the waveguide guiding properties [62]. The index contrast in silica-cladded SOI is $\sim 140\%$. This index contrast does not change significantly with wavelength. In silica cladded LPCVD (PECVD) SiN platform the index contrast is 38% (28%) in the telecommunication window. This index contrast changes by only 2% to 3% for visible wavelengths for PECVD and LPCVD SiN as compared to telecom wavelengths. The higher index contrast of SOI allows for a bend radius of $\sim$5 μm for a 0.45 μm wide strip waveguide as compared to a $\sim$75 μm bend radius for a 1.2 μm wide SiN waveguide operating at 1.55 μm. The tighter bend radius available on the SOI platform allows for the implementation of optical functions on a smaller footprint as compared to SiN. It also enables implementation of high-efficiency grating couplers for out-of-plane optical input/output coupling. This is a very useful feature that allows for wafer-level testing and alignment-tolerant fiber coupling [63]. Nevertheless grating coupler efficiencies better than -3 dB have been reported on the PECVD SiN platform for a wavelength of 0.66 μm using metal reflectors [64].

The advantages provided by the higher index contrast of the SOI platform as compared to the SiN platform come at the price of enhanced sensitivity of SOI devices to nm-scale geometrical variations. These can come from the thickness variation of the silicon device layer or process-induced variations in width and etch depth of the waveguides. All of this results in effective index deviations from the designed value, which is a critical design parameter for interferometric devices such as Mach-Zehnder Interferometers (MZI), ring resonators and Arrayed Waveguide Gratings (AWGs). It is well known that $\sim$1 nm width (thickness) variation produces 1 nm (1.4 nm) spectral shift for such interferometric components [66]. This subject is discussed in more detail in section IV for the case of dispersive spectrometers.

Moreover, high-index contrast SOI waveguides are more prone to spurious reflections. These reflections can be caused by an abrupt index variation in the design of the device or due to surface roughness on the waveguides. In [67], it has been

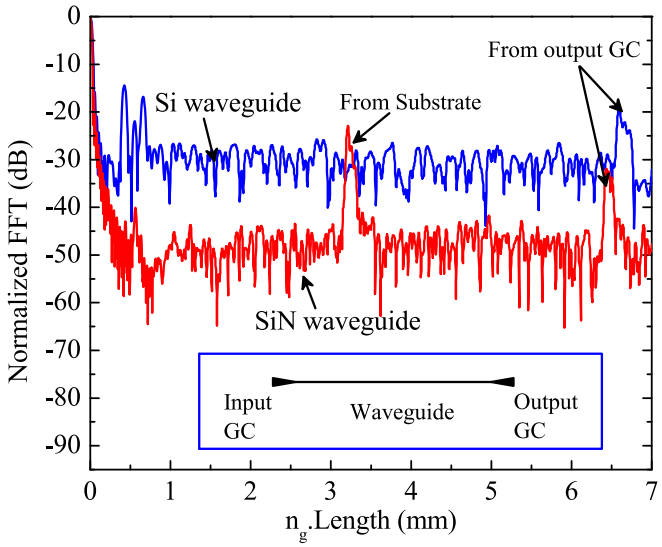

Fig. 2. Spurious reflections in SOI (blue line) and SiN (red line) single mode oxide cladded strip waveguides for TE polarized light. The inset shows the schematic of the test waveguides for spurious reflections. GC stands for Grating Coupler and n_g stands for the group index of the waveguide.

shown that LPCVD based SiN waveguides have 5 to 15 dB weaker distributed reflections due to the surface roughness of the waveguides as compared to SOI waveguides. Fig. 2 shows an indicative plot for spurious reflections in a single mode oxide cladded SOI and oxide cladded LPCVD SiN strip waveguide fabricated using the same fabrication technology at imec. Such spurious reflections degrade the performance of devices such as ring resonators for bio-sensing applications [68] and are also problematic for PICs involving lasers and amplifiers. Smart design strategies [28], [49] have been developed to minimize the effect of back reflections in SOI waveguides.

C. Waveguide Loss

A high index contrast leads to high guided mode field intensity at the sidewalls of Si or SiN waveguides. This increased interaction with the surface enhances scattering when surface roughness is present. If the BOX is thick enough to prevent substrate leakage then the imperfect waveguide sidewalls are a major source of waveguides loss and this is typically proportional to Δn^2 where [69], [70],

$$\Delta n^2 = n_{\text{core}}^2 - n_{\text{cladding}}^2. \quad (1)$$

Fully etched SOI photonic wires - silicon strip waveguides - that are completely surrounded by a silica cladding - have a typical waveguide loss of $\sim$1.5 dB/cm for TE polarized light in the C-band [27]. Loss values of $\sim$0.7 dB/cm have been reported for partially etched rib waveguides.

In SiN LPCVD (PECVD) photonic wires these losses can be $\sim$5 ($\sim$7) times lower, as can be estimated from the Δn^2 of the SOI and SiN waveguides. The losses can be reduced further by using shallow rib waveguides or by using very thin strip waveguides, but this is obviously at the expense of lateral and/or vertical confinement. At IR wavelengths, losses down to 1 dB/m have been reported by the latter approach [71] in which 0.08 μm to 0.1 μm thick LPCVD SiN layers were used. In [39] a waveguide loss of 0.5 dB/cm has been demonstrated using a thicker LPCVD SiN layer of 0.7 μm at 1.55 μm wavelength in strip waveguides with a trapezoidal cross-sections. Using PECVD SiN, losses of $\sim$1.5 dB/cm have been demonstrated for the visible and the very near IR wavelength range for strip waveguides [35]. For 1.55 μm, in [72] strip waveguide loss of 4 dB/cm has been reported on 0.5 μm thick PECVD SiN.

D. Manufacturing Flexibility

SiN is deposited by an LPCVD or PECVD deposition technique which implies that there is a lot more flexibility to combine the SiN waveguides with other photonic structures than is the case for SOI waveguides. As an example, one can deposit the waveguide layer on top of a DBR-mirror or metal mirror and thereby boost the efficiency of standard grating couplers [64], [73]. In [64], this approach has led to the demonstration of coupling efficiencies of $\sim$60% for focusing grating couplers operating at 0.66 μm wavelength. Also, one can deposit the waveguide layer in two steps and add luminescent quantum dots in the waveguide core in between both steps [58].

Moreover the manufacturing flexibility of SiN has been used to either stack multiple layers of SiN [74], [75] or combine SiN and SOI on a single platform [36], [76], [77]. This approach pavesthe way for low loss and high integration density PICs. Combining SOI and SiN on a single platform provides the unique features of both platforms in a single chip. In such a multilayer platform, passive components demanding low loss and high fabrication tolerance are defined on the SiN layer. Functions such as modulators and photodiodes are defined on the Si layer. This scheme has been deployed for the demonstration of broadband coherent receivers [7] and high-speed transceivers [76].

The main challenge in realizing such multilayer platforms is to have fabrication tolerant low loss transitions from one layer to the other and low crosstalk for crossings between the two layers. Approaches using directional couplers [74], grating couplers [77], inverted tapers [78] and reflector mirrors [79] are used to implement interlayer coupling in multilayer platforms. Typically the multiple layers in multilayer platforms are separated by an oxide layer. Depending on the thickness of this oxide layer, a compromise exists between the transition loss and crossing loss. In [80], this compromise is mitigated by using an intermediate SiN layer between the Si and SiN layer. The transition loss of $<$0.003 dB and crosstalk of $-$52 dB are reported using this approach.

In terms of electronic-photonic integration, there are cases where it is desirable to be able to co-integrate electronic circuitry with photonic circuitry by wafer-scale methods on the same wafer. With the SiN platform, this integration can be much more flexible and efficient than is the case of SOI. This is simply due to the fact that SiN is prepared by a deposition process.

E. Third-Order Non-linearity

Silicon has a large third-order non-linearity. Its Kerr index is roughly 20 times higher than that of SiN in the

telecommunication band. The large Kerr index in combination with small mode effective area due to strong confinement provided by the high index contrast of silicon waveguides result in a non-linear parameter that is $\sim$200 times stronger than SiN waveguides [15]. Despite that, crystalline silicon is not sufficiently efficient for nonlinear processes in telecommunications bands because of two-photon absorption (TPA) [81] resulting from its small bandgap of 1.1 eV. For wavelengths beyond $\sim$2.2 μm, the problem of TPA is drastically reduced. This makes silicon waveguide structures ideal for implementing non-linear optical devices in the mid-IR [52], [53], [82].

TPA induces extra waveguide losses at high power, but at the same time excess loss is also induced by free carrier absorption of the generated carriers. The latter also induces free carrier induced index change. Already at a continuous wave power of a few tens of mW the TPA-induced penalty sets in. This limits the maximum intensity level before non-linear processes such as Self-Phase Modulation (SPM), Cross-Phase Modulation (XPM), Four Wave Mixing (FWM) and Stimulated Raman Scattering (SRS) take place. In order to exploit silicon waveguides for non-linear signal processing functions in the telecommunication band, the free carriers from the waveguide can be removed by using a reverse-biased PIN diode across the silicon waveguide [83]. This approach reduces the carrier life time in a silicon waveguide by several orders of magnitude. Using this approach a FWM conversion efficiency of -1 dB has been demonstrated [84] for CW pumping but at the cost of extra processing steps. Applications such as signal regeneration [85], [86], wavelength conversion [87], optical parametric gain [88], [89], supercontinuum generation [90] and third harmonic generation in SOI [91] have been reported.

SiN has a weaker Kerr non-linearity of $\sim 0.26 \times 10^{-18}$ m^2/W in the telecommunication band. The TPA is virtually zero due to a much larger bandgap (5.3 eV). Despite a weaker Kerr non-linearity in SiN, the possibility to have very low loss waveguides with no TPA enables efficient non-linear processes in SiN, especially when resonant structures are used to enhance the pump power. It has therefore been possible to demonstrate impressive frequency comb generation, supercontinuum generation and wavelength conversion in SiN photonic wires [15], [92]–[96].

F. Pockels Effect and High-Speed Functions

The two key high-speed functions desired for telecom/datacom PICs are modulators and detectors. To implement a linear modulator, typically the Pockels effect or the linear electro-optic effect is to be used.

Both silicon and silicon nitride have a negligible Pockels effect in view of the centro-symmetry of both materials. Therefore electro-optic modulation is not possible using the Pockels effect. In the case of the SOI platform, one can resort to the plasma dispersion effect. It is a weak electro-optic effect by which the refractive index of the waveguide is modulated by injection, accumulation or depletion of free carriers [97]. For high-speed operation, depletion-type modulators using reverse-biased PN junction are preferred and speeds of up to 50 Gb/s have been demonstrated [98]. Such modulators have a large footprint (a few mm long) and they consume a substantial power at high modulation speeds. Moreover, these modulators have a relatively high insertion loss, a limited linearity and chirp.

The hunt is open for a more compact high-speed modulator by using the Pockels effect, which can overcome the above mentioned problems associated with the plasma dispersion effect based modulators. In recent years, a strong Pockels effect has been reported in SOI waveguides. These results were achieved by a strain gradient that was induced by means of a strained silicon nitride overlayer [99]. The precise mechanism for this phenomenon is still a matter of debate, but one recent report attributes the effect to a strain gradient in the silicon nitride rather than that in the silicon [100]. This may open the door to strained SiN-based Pockels modulators. An alternative route applicable to both SOI and SiN is to overlay the waveguide with a strong electro-refractive or electro-absorptive cladding layer. Results have been reported for graphene [101], for poled polymers [102], for ferro-electric materials [103] and for ABC-metamaterials [104], [105].

An integrated photodiode is another key high-speed function required for PICs. In the telecommunication band, Germanium has a high absorption coefficient. In SOI-based silicon photonics, germanium is epitaxially grown on top of silicon for photodetection. Demonstrations of monolithically integrated germanium p-i-n [2], [3], [106] and Avalanche Photo Diodes (APD) [107] have been reported. Low dark currents of 4 nA and bandwidths of 67 GHz have been reported with a 0.74 A/W responsivity for C-band operation in monolithically integrated Germanium p-i-n photodiodes [108]. For SiN-based PICs, silicon can potentially be used for integrated photodiodes for visible/near-IR wavelengths. At telecom wavelengths, a first graphene-based photo-detector has been reported for SiN-based PICs [109]. To overcome this lack of high speed photodiode in SiN, it can be combined with SOI whereby there is access to high speed germanium photodiodes [80].

G. Temperature Sensitivity

Silicon has a thermo-optic coefficient of $\simeq 1.86 \times 10^{-4}$ K^{-1} at 1.55 μm. This large thermo-optic coefficient makes SOI-based devices sensitive to temperature variations. Typically 1°C change in temperature shifts the spectrum of SOI wavelength filters by 70 pm. To circumvent this, either active tuning is deployed or temperature insensitive SOI-based devices are designed [65], [66], [110]–[112] to ensure fixed wavelength operation. The large thermo-optic effect is used to good effect for implementing low-speed thermo-optic switches [113], couplers with arbitrary coupling ratios [114], tunable filters [30] and to compensate fabrication-induced phase errors on delay lines or ring resonator based interferometric filters. Typically metallic micro-heaters are embedded on top or beside the waveguides to induce phase shifts by the thermo-optic effect. Apart from that, n-doped waveguides have also been demonstrated as heaters [115]. The amount of electrical power needed to induce a certain phase shift and the speed of operation of the micro-heater define the figures of merit for the micro-heaters. Stoichiometric

TABLE I
CHARACTERISTICS OF SILICON PHOTONICS USING SILICON AND SILICON NITRIDE PLATFORMS. APART FROM THE TRANSPARENCY RANGE, TYPICAL VALUES IN THE C-BAND ARE QUOTED. THE WAVEGUIDE LOSS AND THE NON-LINEAR COEFFICIENTS ARE QUOTED FOR A STRIP WAVEGUIDE GEOMETRY. THE VALUES IN PARENTHESES ARE FOR PECVD SiN

	Silicon	Silicon Nitride
Transparency: Shortest λ (μm)	1.1	0.4
Transparency: Longest λ (μm)	$\sim$4	$\sim$4
Guiding layer thickness (μm)	0.05 to 0.5	0.05 to 0.7
Index Contrast (%)	140	38 (28)
Waveguide Loss (dB/cm)	1 to 1.5	0.001 to 0.5 [71], [39] (4.0) [72]
Kerr Index (m^2/W)	$\sim 4.5 \times 10^{-18}$ [116], [81]	$\sim 0.26 \times 10^{-18}$ [15]
TPA Coefficient (m/W)	$\sim 9 \times 10^{-12}$	0
Distributed Backscatter (dB/mm)	-25	-30 to -40 [67]
n_{eff} sensitivity (strip width) nm^{-1}	$\sim 10^{-3}$	$\sim 10^{-4}$
Temperature Sensitivity K^{-1}	$\sim 1.86 \times 10^{-4}$	$\sim 2.45 \times 10^{-5}$
High speed Modulators Gb/s	>40	Not available
Integrated Photodetector GHz	>60	Not available
Layer Stack Flexibility	Limited	Excellent

silicon nitride deposited using the low-pressure chemical vapor deposition (LPCVD) technique has a thermo-optic coefficient of $\simeq 2.45 \times 10^{-5}$ K^{-1} at 1.55 μm. In [44] a filter spectral shift of 11 pm/K has been quoted. This leads to a larger power dissipation for micro-heaters in SiN. On the other hand, for temperature-sensitive applications the lower thermo-optic coefficient of SiN is advantageous.

Table I summarizes the important properties of the SOI-based and SiN-based material platforms used for silicon photonics.

IV. THE CASE OF DISPERSIVE SPECTROMETERS IN SOI AND SILICON NITRIDE

A spectrometer is a wavelength selective filter. It can separate different wavelengths propagating in a waveguide. Due to reciprocity, the same filter can be used to combine multiple wavelengths propagating through different waveguides into a single waveguide. Traditionally wavelength-selective devices have been used in optical communication at 1.3 μm and 1.55 μm. More recently such filters are sought for optical spectroscopy and sensing applications in mid-IR and visible, where the light from a broadband source is resolved spectrally after interaction with the material under investigation using a wavelength-selective device.

Arrayed Waveguide Gratings (AWGs) and Planar Concave Gratings (PCGs)-also called planar waveguide echelle gratings-are the two most used configurations for wavelength selective filters. PCGs are reflective spectrometers comprising a slab region and a curved grating. AWGs exist both in transmission and reflection-based versions and dispersion is introduced by an array of waveguides with fixed path length difference between them. More detailed principles of both devices are discussed in [117] and [119] respectively. AWGs are commercially deployed in optical networks, while PCGs are to our knowledge not commercially deployed but have shown promising performance in research labs. Both AWGs and PCGs are complex to design, requiring multiple simulation strategies and involve different fabrication challenges. Therefore, they are considered as perfect candidates to gauge the performance of the two silicon photonic material platforms discussed here. This comparison is done at a wavelength of 1.55 μm. At shorter wavelengths ($<$1.1 μm) SiN is the only option and at mid-IR wavelength ($>$2 μm) the better index contrast of silicon makes it superior in terms of its performance and form factor [126]. In the scope of the discussion in this section, 0.22 μm SOI with 2 μm BOX and 0.3 μm LPCVD SiN with 2 μm BOX are considered. However there have been demonstrations of cm-scale footprint SiN AWGs on much thinner SiN layers of 50 nm with a 15 μm BOX layers [121]. In another implementation a 12 channel AWG with 100 GHz channels spacing is demonstrated with a crosstalk of $\sim$20 dB and 5 dB of insertion loss [76].

The important figures of merit of an AWG are the accuracy of the center wavelength of the channels, crosstalk between adjacent and non-adjacent channels, insertion loss and the return loss. SiN waveguides have lower waveguide losses, but the delay length for a given FSR is $\sim$2 times longer than for SOI waveguides. Therefore, the insertion loss for both types of AWGs is expected to be comparable. SiN AWGs with very low insertion loss of $\sim$0.2–0.5 dB are reported [121], but that is at the expense of large footprint due to the mm-scale bending radius required for waveguides with weak lateral and vertical confinement. The return loss of silicon AWGs is bound to be larger due its larger index contrast, although values have not been reported for the two platforms. The major source of the return loss are the reflections at the star couplers of the AWG and the roughness on the waveguides. The former effect is normally solved by implementing a two etch-step adiabatic transition at the interface between waveguides and the star couplers [49]. The latter effect is mitigated by using wider waveguides in the grating arms.

The center frequency of a channel of the spectrometer is influenced by the local effective index of the waveguide grating arms. This is influenced strongly by the thickness variation of the guiding layer of the material platform. Commercially available 300 mm SOI wafers have 2 nm intra-wafer variation in the thickness of guiding silicon layer when measured by 50 point mapping on the wafer. For partially etched silicon on such wafers the thickness variation is $\sim$6.5 nm [123] with a standard deviation of 2.2 nm when wafer-to-wafer and lot-to-lot variations are considered. Moreover the width of the waveguide core also impacts the local effective index. For standard silicon strip waveguides, the waveguide width is $\sim$2 times larger than the thickness of the guiding silicon layer at 1.55 μm. This makes the effective index variations more sensitive to thickness variations than to the width variation. It is evident from Fig. 3(a) and (b) that for silicon strip waveguides (0.45 μm $\times$ 0.22 μm), the local effective index variation induced by variation in the thickness is $\sim$2 times stronger than due to variation in the width of the waveguide. Using a commercial mode solver, it has been calculated that a thickness variation of 1 nm induces an effective index variation of the order of 10^{-3}.

On the other hand, for a 0.3 μm thick SiN guiding layer and using 1.2 μm wide waveguides for operation at 1.55 μm, the effect of a 1 nm thickness change is 8 times stronger than the waveguide width change as shown in Fig. 4(a) and (b).

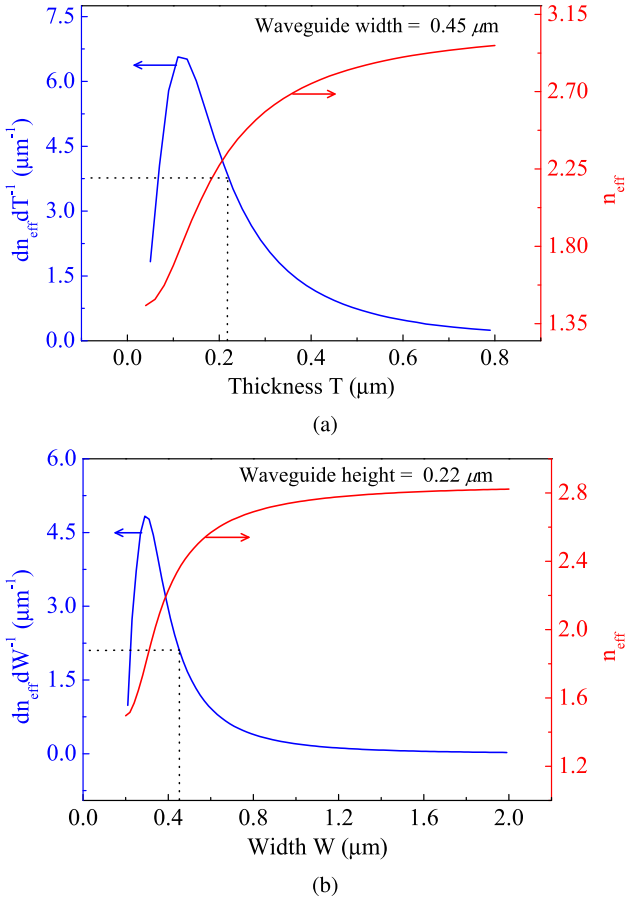

Fig. 3. Effective index (red) and its variation (blue) for the fundamental TE mode of silica cladded SOI strip waveguide (a) with thickness T for 0.45 μm wide waveguide and (b) with width W for 0.22 μm thick silicon guiding layer.

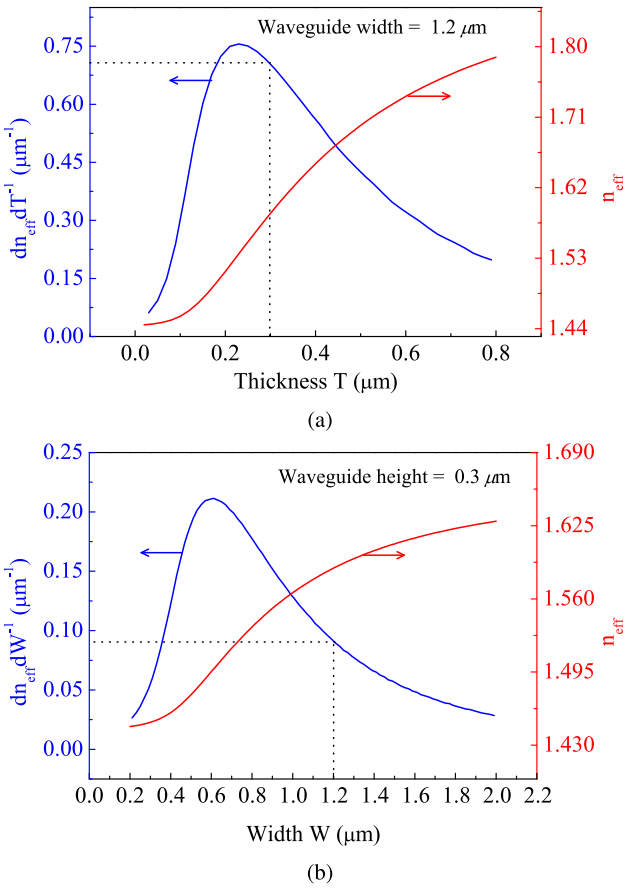

Fig. 4. Effective index (red) and its variation (blue) for the fundamental TE mode of silica cladded SiN strip waveguide (a) with thickness T for 1.2 μm wide waveguide and (b) with width W for 0.3 μm thick SiN guiding layer.

Calculations using commercial mode solver has shown that a thickness change of 1 nm introduces local effective index change of the order of 10^{-4}.

The spectral shift $\Delta\lambda$ is related to the local effective index variation Δn_c and the group index of the waveguide n_g by Eq. 2 [124]:

$$|\Delta\lambda| = \lambda_0.\Delta n_c/n_g. \tag{2}$$

The effective index variation Δn_c in SOI waveguide due to changes in thickness is ~5.5 times larger than for the SiN waveguides (see Figs. 3(a) and 4(a)). Moreover the group index n_g of SOI waveguide is ~2.2 times larger than the SiN waveguide. This leads to a ~2.5 times larger spectral shift for SOI-based AWGs as compared to SiN-based AWGs. This shift in the center wavelength of a channel are acceptable for applications such as wavelength metering [125], [126], spectroscopy of liquid and solid analytes [127] and coarse WDM by using flat top filters [122]. For applications requiring a better channel wavelength accuracy, the temperature of operation of the AWG can be changed to shift the overall spectrum of the AWG. The order of magnitude weaker thermo-optic effect means that roughly the same amount of electrical power will be required to align the center frequency of a channel of the silicon and SiN-based AWGs to a grid.

Another consequence of the variations in the waveguide geometry or the thickness of the material stack is the different average effective index for each of the waveguide grating arms. This results in phase errors on the grating arms. Since an AWG is an interferometric device, these phase errors result in a degraded crosstalk, as described by the empirical formula [124];

$$\text{Crosstalk}_{\text{AWG}} \simeq 20 \cdot \log \frac{\delta n_c L_{\text{ctr}}}{\lambda_0} \tag{3}$$

where δn_c is half of the peak-to-peak variation in the average effective index of a grating arm, L_{ctr} is the length of the middle waveguide of the arrayed waveguide grating and λ_0 is the central wavelength. Using Eq. 3, the cross-talk of the silicon and SiN AWGs of similar specifications can be compared. It is considered that the peak-to-peak variation in the average effective index of a delay line is 10 times smaller than the local effective index variation [124]. Considering this, an AWG with an FSR of 3200 GHz and 16 channels with 200 GHz channel spacing in silicon platform has a crosstalk of ~ -18 dB, which is in good agreement with the measured results shown in [49]. An AWG with the same specifications in SiN will deliver a crosstalk of ~ -30 dB. The above discussion implies that for a given number of channels in an FSR, an order of magnitude lower δn_c makes SiN-based AWGs superior to SOI-based AWGs despite 2 times longer L_{ctr}. AWGs with large FSR and large channel

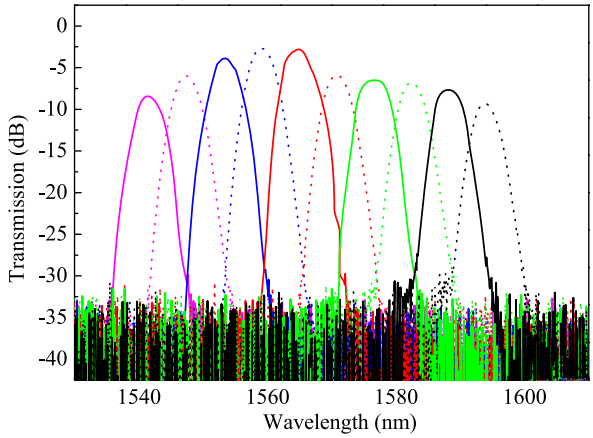

Fig. 5. Measured transmission of a 10 channel PCG fabricated on LPCVD SiN with 0.3 μm guiding and 3.3 μm BOX layers respectively [43].

spacing result in shorter L_{ctr}. This results in improved crosstalk for SOI-based AWGs and makes them a viable option for applications requiring large channel spacing as demonstrated in [49], where a 16 channel SOI-based AWG with 200 GHz channel spacing has shown a crosstalk of ~ -20 dB at a wavelength of 1.55 μm. In SiN-based AWGs a similar performance has been demonstrated even for 100 GHz of channel spacing [76] by a 12-channel AWG operating at 1.55 μm.

In PCGs, the major source of insertion loss comes from the limited reflection of the grating teeth. Factors such as rounded corners of grating teeth and roughness of the grating teeth introduce excess loss. Moreover, for thicker guiding layers, the non-verticality of the grating teeth also results in reduced reflection. It is expected that the insertion loss for silicon or SiN PCGs is comparable. To have a large reflectivity (90%), Distributed Bragg Reflector (DBR) mirrors are used [118]. Such high reflectivity is highly desirable to limit the insertion loss of the PCGs. Typically SOI uses DBR mirrors with $\sim 25\%$ fill factor with reference to the unetched part and with a grating period of 0.6 μm. In SiN, a DBR with comparable performance has more relaxed values for fabrication, hence making it more tolerant to fabrication errors. The crosstalk in PCGs is influenced by the thickness variation in the free-propagating slab region and the position of the grating teeth [119]. The crosstalk of a PCG in a high index contrast platform is related to the slab effective index n_s, the position fluctuation of the reflective facets of the PCG $\delta\zeta$, the variation in effective index of the slab induced by thickness variation of the guiding layer δn_s and the slab length from the input to the middle reflective facet L_{ctr} by [124],

$$\mathrm{Crosstalk_{PCG}} \simeq 20 \cdot \log\left(\frac{2\delta\zeta n_s}{\lambda_0} + \frac{2L_{\mathrm{ctr}}\delta n_s}{\lambda_0}\right). \quad (4)$$

In [128] and [43], PCGs on SOI and SiN are demonstrated. Using Eq. 4, PCGs in silicon [128] with 4 $\times$ 20 nm channels are compared (crosstalk ~ -23 dB) with PCGs in SiN [43] with 10 $\times$ 6 nm channels. Using their measured crosstalk and considering that $\delta\zeta$ is comparable for the two PCGs as they are fabricated using the same technology, the effective index variation due to thickness variation of the slab δn_s is found to be of the order of 10^{-4} for silicon PCGs, which is an order of magnitude stronger as compared to SiN-based PCGs. Fig. 5 shows the transmission of the SiN PCG considered for the comparison with a silicon PCG. The SiN PCG is fabricated using 0.3 μm LPCVD SiN on 3.3 μm BOX layer and 1 μm top oxide cladding. The nearest-neighbor crosstalk and insertion loss at the central channel was measured to be -34 dB and 1.5 dB respectively. Non-optimum grating couplers for channels 6 to 10 have resulted in larger insertion loss for these channels. All the channels are normalized by using the optimum grating coupler used for channel 5.

The examples mentioned above indicate that dispersive spectrometers in SOI and SiN have shown promising performance.

V. Conclusion

SOI-based silicon photonics has evolved to become a mature technology platform for photonic integration. The last few years we have already seen the emergence of commercial silicon photonic products in the market. This success has opened new avenues of applications next to the traditional communication-geared applications. Silicon Nitride, being a moderately high index and well-known material in CMOS fabrication, provides an equally valuable option for the manufacturing of densely integrated photonic circuits in a CMOS-fab. The two platforms nicely complement each other's deficiencies. While the focus of SiN PICs is still largely with passive functions, one can expect in the future the emergence of approaches for the integration of high speed modulators and detectors and even light sources by means of wafer-scale technologies in the CMOS-fab.

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