Layout-Aware Yield Prediction of Photonic Circuits

Wim Bogaerts, Umar Khan and Yufei Xing
Ghent University - imec, Photonic Research Group, Department of Information Technology, Gent, Belgium.
Center of Nano and Biophotonics, Ghent University, Belgium.
Email: wim.bogaerts@ugent.be

***Abstract*—We demonstrate yield prediction of silicon wavelength filters using layout-aware Monte-Carlo circuit simulations. Maps of wafer and die-level variability of width and thickness are projected onto circuit layout and translated into circuit model parameters. We apply this onto Mach-Zehnder lattice filters with different filter orders.**

I. Introduction

Silicon photonics enables large-scale integration of photonic circuits thanks to high index contrast submicrometer waveguides. But this high contrast also all components sensitive to nanometer-scale geometry variations. This in turn affects the circuit performance, especially as circuits become larger. Efficient yield prediction in the design stage is an essential requirement for scaling up silicon photonic circuits [1].

This is especially needed for wavelength filters, as these are very sensitive to phase variations and coupling variations . Design processes for wavelength filters are well known, but an accurate prediction of their yield in the presence of fabrication variations is not trivial. Monte-Carlo methods with random variations give an idea of the sensitivity of the circuit, but this is not a realistic representation of actual fabrication variation. For instance, a silicon wire waveguide is most sensitive to the line width and the waveguide thickness, and these are affected by very different processes during the fabrication, with a different distribution over the wafer. Also, variations within the circuit are correlated: elements closer together are more likely to be matched than elements further apart. A good yield prediction therefore depends on the correct mapping of the various sources of variability at die or wafer level caused by the fabrication as well as the design (e.g. pattern density) [3], [4]. Random Monte-Carlo methods, but also faster methods based on Polynomial Chaos expansion [2] can not easily take these different mappings into account.

The Monte-Carlo method can be enhanced by incorporating the spatial information in the form of wafer maps [3], [4]. We have built such a circuit-level variability analysis tool for yield analysis with variable fabrication processes. We separate the concerns of the compact model building and the mapping with the process statistics. When component designers (or fabs) build a compact circuit model for a building block, they are not aware of the larger circuit context which a designer will encounter in his specific design. However, a component designer can still simulate or measure the sensitivity of the component to a number of fabrication effects, such as linewidth or thickness variation. This sensitivity or correlation can be embedded in the model of the component, or supplied as an additional lookup table. In parallel, fabrication conditions are generally monitored through statistical process control based on in-line measurement of test structures (e.g. SEM measurements, ellipsometry) or extracted from measurements on devices. This results in different wafer maps for all important parameters that affect a component's behavior.

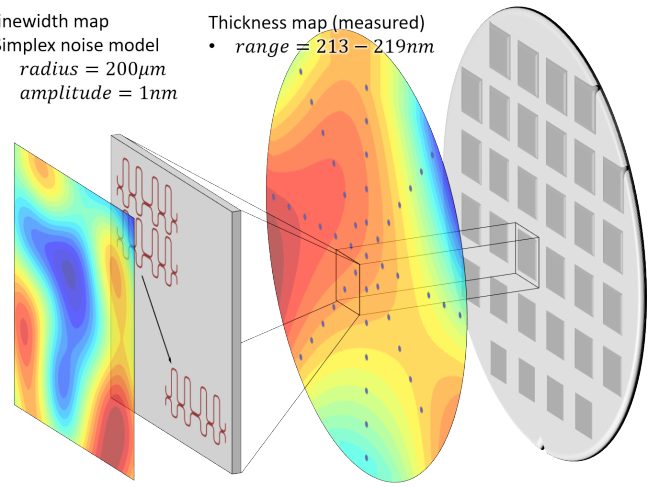

Fig. 1. Maps of processing-related parameters such as deviations in linewidth and thickness are projected onto the circuits in the actual layout.

The models with sensitivity and the wafer maps are combined into a Monte-Carlo simulation using different locations on a wafer (different dies and within the same die) or on different wafers. This results in a yield prediction that takes into account the actual layout and distribution of the circuit on the chip.

II. Implementation

We implemented the *variability engine* (VE) onto the commercial circuit simulator *Caphe* by Luceda Photonics [5], which is integrated in the design framework IPKISS with access to the circuit's parametric layout. Caphe allows the implementation of efficient full-custom models in Python, both in time domain and frequency-domain. We extended the circuit models with sensitivity data that can be supplied by the user or the fab, expressing how every model parameter is sensitive to fabrication variables. There is no need for expensive interpolated models: only the sensitivity is needed.

Wafer maps for variables such as thickness and line width can be generated from measurements or from models. Such