



# 27 dB gain III-V-on-silicon semiconductor optical amplifier with > 17 dBm output power

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**Abstract:** Hybrid III-V-on-silicon semiconductor optical amplifiers with high-gain and high-output-power are important in many applications such as transceivers, integrated microwave photonics and photonic beamforming. In this work we present the design, fabrication and characterization of high-gain, high-output-power III-V-on-silicon semiconductor optical amplifiers. The amplifiers support a hybrid III-V/Si optical mode to reduce confinement in the active region and increase the saturation power. A small-signal gain of 27 dB, a saturation power of 17.24 dBm and an on-chip output power of 17.5 dBm is measured for a current density of 4.9 kA/cm<sup>2</sup> (power consumption of 540 mW) at room temperature for an amplifier with a total length of 1.45 mm. The amplifiers were realized using a 6 quantum well InGaAsP active region, which was previously used to fabricate high-speed directly modulated DFB lasers, enabling their co-integration.

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## 1. Introduction

Silicon photonics is a key technology in the field of integrated optics. Passive photonic integrated circuits (PICs) have been designed for many applications such as integrated microwave photonic filters [1] and optical beam steering [2]. However, many essential photonic circuits, such as transceivers, require the integration of active components (light sources, amplifiers, modulators and photodetectors). An appealing method to create active PICs is the heterogeneous integration of InP-based materials on the silicon-on-insulator platform. This approach allows to combine the scalability of silicon photonics with the high performance of InP-based opto-electronic components. This technology has been used for example to demonstrate integrated high-speed directly modulated lasers (DMLs) [3] and high-speed Mach-Zehnder modulators [4]. Apart from its use for optical transceivers, III-V-on-silicon is also a very promising platform for the realization of integrated microwave photonic ICs [5] [6]. Many of the systems that are being implemented in silicon and III-V-on-silicon photonic integrated circuits could however be greatly improved by higher on-chip optical power. Examples include the realization of long-range chip-scale LIDAR systems [7] and the implementation of microwave photonic links, as the link gain depends quadratically on the optical power received at the opto-electronic conversion stage [8].

Although several semiconductor optical amplifiers (SOAs) have been developed, both on the InP platform and the hybrid III-V-on-silicon platform, achieving high-gain and high-output-power remains challenging. The highest output power from a C-band InP discrete SOA was achieved using a slab coupled optical waveguide (SCOW) design [9]. Although this design provides watt-level output power, this type of amplifier demands a dedicated layer stack and an amplifier length of 1 cm, making the co-integration with other photonic components not straightforward. A chip saturation output power of 19.6 dBm and a gain of >15 dB was reported for a discrete InP/InGaAsP SOA with 3 quantum wells [10]. Again, in monolithic integration many different components have to be integrated together and specific integration for high-power SOAs is not

trivial [11] [12]. SOAs have also been developed on the III-V-on-silicon platform, both using direct die-to-wafer bonding and divinylsiloxane-bis-benzocyclobutene (DVS-BCB) adhesive die-to-wafer bonding. In the latter approach the bonding is facilitated by spin-coating a thin layer (40-100 nm) of DVS-BCB, a planarizing spin-on polymer, on the silicon PIC. In [13] III-V/Si SOA designs are presented where the wall-plug efficiency is optimized for 10 dB gain SOAs with 13 dBm of on-chip output power. A packaged III-V-on-silicon amplifier with 28 dB gain is demonstrated in [14], but the saturation power is not discussed and the highest mentioned on-chip output power is 12 dBm. More recently III-V-on-silicon SOAs using direct die-to-wafer bonding were fabricated with 14 dB gain and 16.8 dBm saturation power [15]. This was achieved with a 2 mm long amplifier, using a 3 quantum well material with a power consumption of approximately 640 mW.

In this paper we present the design, fabrication and characterization of an array of hybrid III-V-on-silicon SOAs. The array consists of 5 SOAs with identical cross-section but with different lengths, ranging from 0.95 to 1.85 mm. This enables to assess the impact of the device length on the amplifier performance, as well as to enable loss measurements (internal loss of the amplifier and the loss of the III-V/silicon transition sections). A 1.45 mm long SOA was measured to have an unsaturated gain of 27 dB and an on-chip amplified output signal of 17.5 dBm. This result was achieved at a current density of 4.9 kA/cm<sup>2</sup> and a power consumption of 540 mW. The 1.2 mm long SOA provides 24.7 dB of gain and a maximum on-chip output power of 17.2 dBm at the same current density (power consumption of 410 mW). The remainder of this manuscript is structured as follows: in the first part we discuss the design and fabrication of the amplifier. In the second part we discuss the characterization of the device and in the final section we summarize the results and present a conclusion.

## 2. Design and fabrication

As discussed in the previous section, there are several approaches to achieve an integrated high-output-power amplifier. However, the two main strategies are to either have low confinement in the active region or having a large cross-section active region. This is illustrated by the formula for the saturation power  $P_s$  [15], which is defined as the optical power for which the gain coefficient  $g$  is halved:

$$P_s = \frac{hc}{\lambda} \cdot \frac{\sigma_{xy}}{a\tau\Gamma_{xy}}, \quad g = \frac{g_0}{1 + P/P_s}. \quad (1)$$

Where  $h$  is the Planck constant,  $c$  is the speed of light,  $\lambda$  is the wavelength in vacuum,  $\sigma_{xy}$  is the cross-sectional area of the active material,  $a$  is the differential gain,  $\tau$  is the carrier lifetime,  $\Gamma_{xy}$  is the confinement factor of the optical mode in the active region,  $g_0$  is the maximum gain and  $P$  is the optical power. Using a hybrid III-V-on-silicon mode is an appealing strategy to lower the confinement factor, similar to the slab coupled SOA [9]. Furthermore, it is beneficial to realize the amplifier using the same fabrication process and material that can also be used for other active devices to form complex photonic integrated circuits. While other high-output power amplifiers had few quantum wells to optimize output power, it is appealing to implement a high saturation power amplifier using III-V epitaxial material that can also be used for the realization of advanced laser sources on the same circuit, such as directly modulated lasers for example, which typically require more quantum wells [3].

Therefore, the epitaxial layer stack used in this work consists of a 6 quantum well active region, consisting of InGaAsP quantum wells (1.55  $\mu\text{m}$  wavelength, 7 nm thick) and InGaAsP barriers (bandgap wavelength of 1.17  $\mu\text{m}$ , 9 nm thick). A 100 nm thick separate confinement heterostructure above and below the active region is realized using InGaAsP (bandgap wavelength of 1.17  $\mu\text{m}$ ). The top p-contact consists of a highly doped InGaAs layer (300 nm thick) and the p-type cladding consists of a gradient p-doped InP layer (1500 nm thick). A 200 nm thick

n-doped InP layer is used for the n-contact. A cross-section of the III-V waveguide with the different layers indicated is shown in Fig. 1(a).

The silicon rib waveguide underneath the III-V is realized in a 400 nm thick silicon device layer on a 2  $\mu\text{m}$  thick buried oxide layer, by a 180 nm partial etch. The silicon rib waveguide is 4  $\mu\text{m}$  wide, while the III-V mesa is 5  $\mu\text{m}$  wide. The mode is laterally confined by the mesa and the silicon waveguide. The active region is 0.5  $\mu\text{m}$  wider than the p-InP mesa to reduce the interaction between the guided mode and the sidewalls. A simulated hybrid mode-profile is shown in Fig. 1(b). The mode-profile was simulated using FIMMwave and an optical confinement of 0.7 % per well is found for this waveguide design.

Since the amplifier is meant to be used in a photonic circuit, tapering to a single-mode 650 nm wide silicon rib waveguide is implemented. As shown in Fig. 1(c) the transition from the single mode waveguide to the amplifier happens in two steps: first the silicon waveguide is adiabatically tapered from 650 nm to 4  $\mu\text{m}$  over a length of 150  $\mu\text{m}$ , then the III-V waveguide structure is tapered, which is shown in detail in Fig. 1(d). The III-V waveguide tapers in two parts from 0.6  $\mu\text{m}$  to 5  $\mu\text{m}$ , the first part tapers from 0.6  $\mu\text{m}$  to 1  $\mu\text{m}$  over a length of 80  $\mu\text{m}$ . The narrow III-V waveguide width is achieved using an anisotropic etch of the p-type InP cladding, creating a V-shaped waveguide as described in [16]. In the second part of the taper the III-V waveguide widens from 1 to 5  $\mu\text{m}$  over a distance of 100  $\mu\text{m}$ . However, the active region is kept wider than the cladding layer to minimize interaction between the confined optical mode and the sidewalls. Due to the large confinement in the silicon waveguide, the mode-mismatch between the silicon waveguide and the hybrid III-V-on-silicon amplifier is small. The coupling efficiency of the taper and back-reflections of the taper-tip were simulated using FIMMWave and FIMMprop software. It was found that the reflections at the III-V taper tip are below -40 dB and coupling losses are < 0.5 dB per taper.

The fabrication of the amplifiers was achieved using DVS-BCB bonding of the above discussed III-V material, as described with more detail in [16]. A bonding layer thickness of 40 nm was used. First a SiN hard mask is defined to etch the InP mesa. Then the heavily p-doped InGaAs contact layer is dry-etched, after which the p-InP cladding layer is wet etched in diluted HCl. This anisotropic wet-etch creates the V-shape of the cladding layer. A second nitride hard-mask was then deposited to perform a wet-etch of the active region using a  $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$  solution. Then 30-20-50 nm of Ni-Ge-Au is deposited on the n-InP to create metallic n-contacts. Finally the n-InP is etched again using diluted HCl. Once the III-V waveguides are formed the structures are passivated and planarized using DVS-BCB. To electrically contact the III-V waveguide the DVS-BCB is etched back to reveal the top InGaAs contact and vias are etched in the DVS-BCB such that the metallic n-contacts are exposed. In a final step 40-800 nm Ti-Au is deposited using a lift-off process to form the final contact layer and to define contact pads, which allow for easy electrical probing.

The array of 5 SOAs with different lengths was fabricated on a PIC together with several test-structures and other devices. A microscope image of the fabricated sample is shown in Fig. 2(a). The amplifiers length are varied from 0.95 mm to 1.85 mm, including two 0.18 mm long tapers. A cross-section of the III-V-on-silicon amplifier structure is shown in Fig. 2(b).

### 3. Characterization

To characterize the SOAs, the III-V-on-silicon PIC was placed on a temperature-controlled stage and kept at a constant 20°C for all measurements. The device under test is optically probed using cleaved standard single mode fibers on a fiber stage. Reflectionless grating couplers with a simulated back-reflection below -40 dB were used [17]. The amplifiers were electrically contacted using probe needles. The SOAs have a differential resistance ranging from 3.4  $\Omega$  (3630  $\mu\text{m}^2$  surface area) to 1.7  $\Omega$  (8630  $\mu\text{m}^2$  surface area), for the 0.95 mm to 1.85 mm long SOAs respectively. This is similar to the differential resistance found for a full InP SOA (6300  $\mu\text{m}^2$

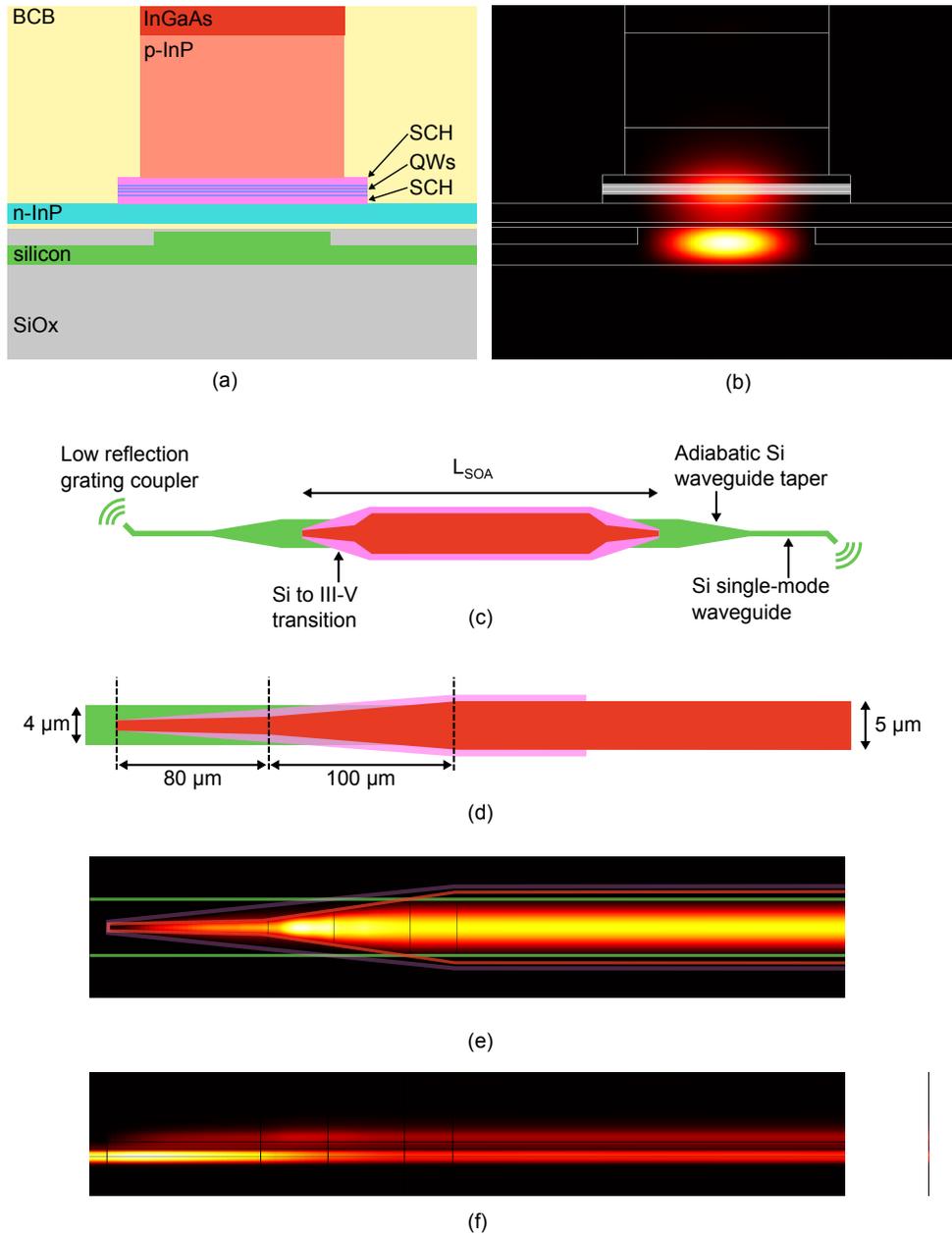


Fig. 1. (a) Cross-section of the amplifier waveguide. (not to scale) (b) Hybrid optical mode in the amplifier, simulated using FIMMwave. (c) Top-view of the silicon waveguide, p-InP mesa and active region. (d) Detailed schematic of the silicon to hybrid III-V-on-silicon waveguide taper. (e) Simulated propagation of the optical coupling from the silicon waveguide to the gain waveguide (top view). Only the intensity in the active layer is shown. The silicon waveguide, p-InP mesa and active area are indicated with colored lines. (f) Side-view of the simulated coupling from the silicon waveguide to the gain waveguide.

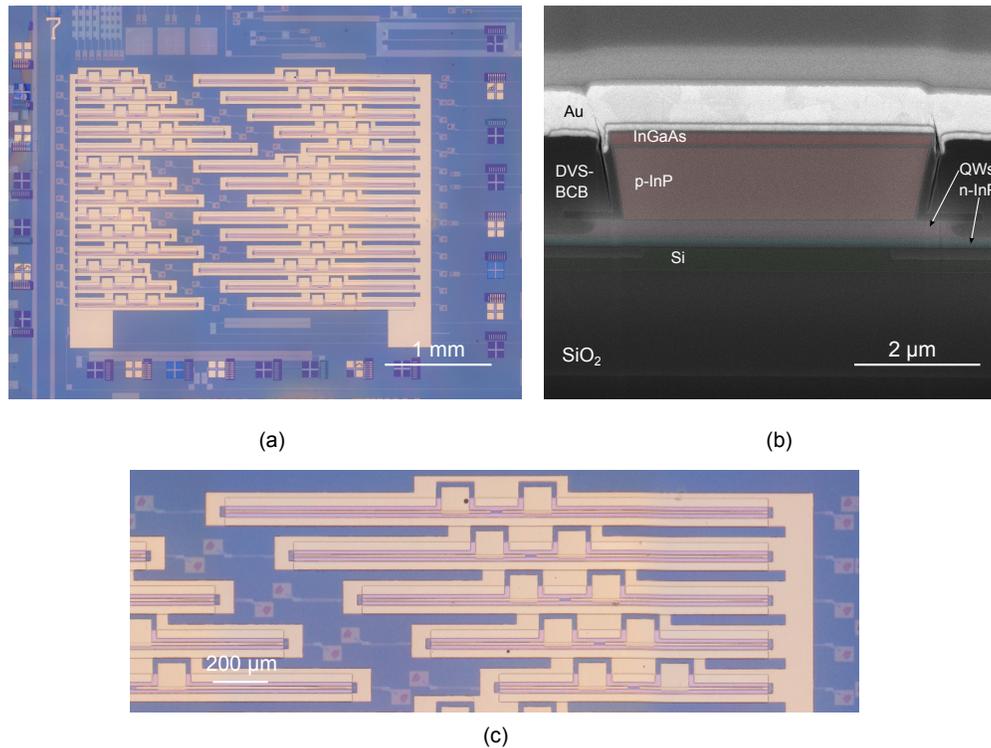


Fig. 2. (a) Microscope image of the fabricated III-V-on-silicon PIC, the SOA array consists of the five devices in the top right corner. Two reference silicon waveguides without III-V material are included in the array. (b) SEM image with colorization of a focused ion beam cross-section of the III-V-on-silicon amplifier. (c) Detailed view of the five SOAs.

surface area) [10]. The differential resistance was determined for an injection current density of  $4.9 \text{ kA/cm}^2$  for all amplifiers. The three shortest amplifiers were biased at 175 mA (1.57 V), 237 mA (1.74 V) and 300 mA (1.8 V) for a length of 0.95 mm, 1.2 mm and 1.45 mm respectively. The two longest amplifiers were biased at 362 mA (1.97 V) and 425 mA (1.79 V) for a length of 1.6 mm and 1.85 mm respectively. The good electrical characteristics of the amplifier allows for high current injection with low self-heating, which is essential for high power operation.

To characterize the on-chip gain of the amplifier, the grating coupler losses must be accurately known as function of wavelength. Therefore, reference passive silicon waveguides were placed on the chip, in between the amplifiers, such that the reference waveguides undergo the same processing as the passive waveguides and couplers of the SOAs. The losses of the grating couplers were determined using a tunable laser (Santec TSL-510) and an optical spectrum analyzer (Anritsu OSA MS9740A), as shown in Fig. 3. As the gain peak of the III-V material is approximately 1575 nm, the angle of the fiber holders was optimized so that the wavelength of maximum transmission coincides with the gain peak. At this optimum angle the grating couplers have a loss of 9.5 dB per coupler at a wavelength of 1575 nm. The grating couplers were optimized for low reflection and in future applications could be replaced by high-efficiency edge-couplers [18]. To determine the gain of the amplifiers, the same measurement set-up was used. The output power of the SOA was measured with the OSA, in a 1 nm band centered at the input laser wavelength. This ensures that the measured output power is not distorted by the amplified spontaneous emission (ASE).

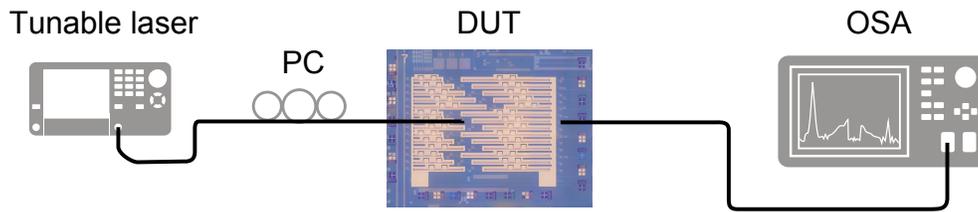


Fig. 3. Schematic overview of the measurement set-up. PC: polarization controller; DUT: device under test; OSA: optical spectrum analyzer.

It was found that all amplifiers, except for the shortest, could generate an on-chip output power exceeding 17 dBm, for an on-chip optical input power of 3 dBm. However, the 1.6 and 1.85 mm long amplifier didn't achieve higher output power or gain than the 1.45 mm. Furthermore, for the two longest amplifiers parasitic lasing occurred for on-chip optical input powers smaller than -10 dBm. From the free spectral range of the lasing modes it was deduced that the lasing is due to parasitic reflections of the cleaved single mode fibers. Optimum gain and output power characteristics were found for the amplifiers with a length of 1.2 and 1.45 mm. Furthermore, a current density of 4.9 kA/cm<sup>2</sup> was chosen, as further increasing the gain current did not improve the output power at high input powers. The on-chip output power as function of the on-chip input power for the three shortest SOAs is shown in Fig. 4(a). The shortest amplifier, 0.95 mm long, provides 20 dB of small-signal gain and 16 dBm of maximum output power. This performance can be practical for some applications but does not show beyond state-of-the-art performance. The two amplifiers with length 1.2 mm and 1.45 mm show over 17 dBm of maximum output power and 14 dB of gain for 3 dBm on-chip input power. To accurately determine the small-signal gain  $G_0$  and gain saturation power  $P_s$  of the 1.2 mm and 1.45 mm SOA, we use the same method as described in [15]. This is implemented by varying the input power of the tunable laser between -15 and +13 dBm while monitoring the SOA output power on the OSA. Both amplifiers were biased at an injection current density of 4.9 kA/cm<sup>2</sup> corresponding to 300 mA for the 1.45 mm SOA and 237 mA for the 1.2 mm long SOA. For this injection current the power consumption of the 1.45 mm SOA is 540 mW and that of the 1.2 mm SOA is 410 mW. The corresponding gain as a function of input power is shown in Fig. 4(b), for a wavelength of 1575 nm, corresponding with the material gain peak in this experiment. This result is fitted with a formula relating the gain  $G$  to the input power  $P_{in}$ , gain saturation power  $P_s$  and small-signal gain  $G_0$ :

$$G(P_{in}) = G_0 \frac{1 + P_{in}/P_s}{1 + G_0 P_{in}/P_s} \quad (2)$$

The small signal gain is found to be 27 dB for the 1.45 mm SOA and 25 dB for the 1.2 mm SOA. The saturation power  $P_s$  was determined from the fit procedure and was found to be 17.24 dBm for the 1.45 mm SOA and 16.72 dBm for the 1.2 mm SOA. In principle the saturation power should be identical for both amplifiers, since it only depends on the waveguide cross-section. However, since the discrepancy is small it can be explained by measurement accuracy and fabrication tolerances. To assess the optical bandwidth of the amplifiers we measured the small-signal gain as function of wavelength of the 1.2 mm long SOA. This was achieved by sweeping the wavelength of the tunable laser from 1550 to 1610 nm with a constant output power of -10 dBm. The output power at the signal wavelength was measured with the OSA, and the transmission spectrum of the grating couplers was de-embedded to calculate the on-chip gain. As described in [19], the gain  $G$  as function of wavelength  $\lambda$  can be described with the following formula:

$$G(\lambda) = G_p \exp \left[ -A(\lambda - \lambda_p)^2 \right]. \quad (3)$$

Where  $G_p$  is the peak value of the gain,  $\lambda_p$  is the wavelength at which the maximum gain occurs

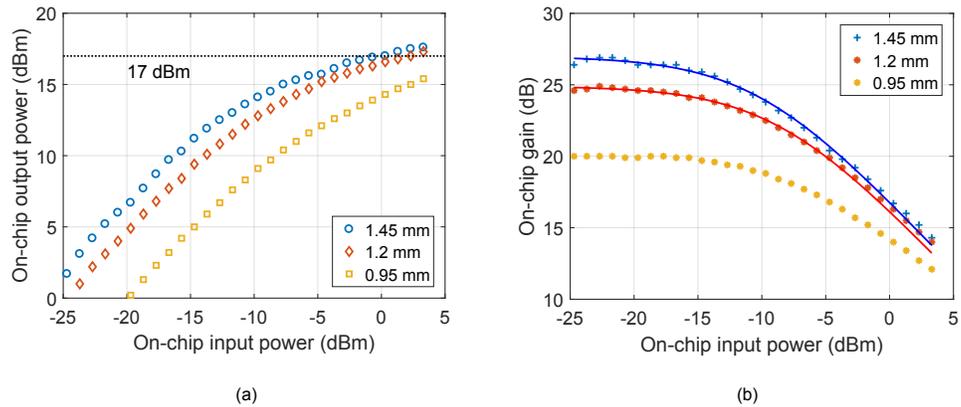


Fig. 4. (a) The on-chip output power as function of the input power for three different SOA lengths. (b) The gain as function of on-chip optical input power for three SOAs with different lengths. The points are measured values, the line is a fit.

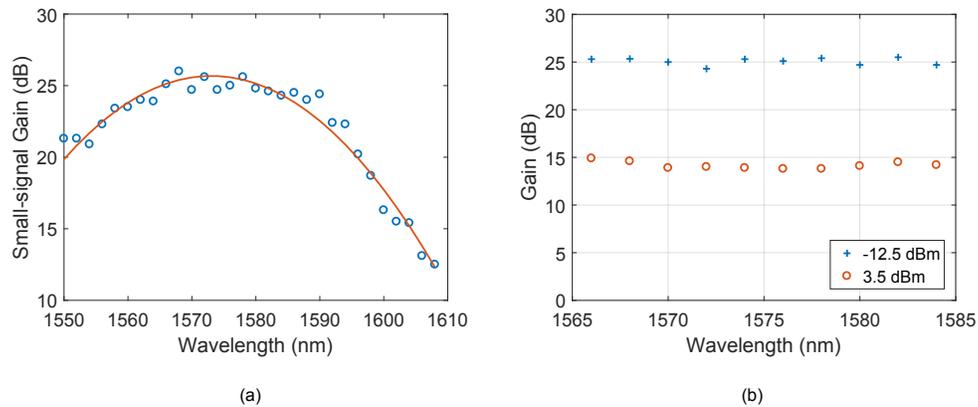


Fig. 5. (a) Small-signal gain as function of the wavelength of the 1.2 mm long SOA, for a current density of  $4.9 \text{ kA/cm}^2$ . The circles represent the measured values, the full line is a fitted curve. (b) The on-chip gain as function of the wavelength for an injection current of  $4.9 \text{ kA/cm}^2$  for the 1.45 mm long SOA. The gain was measured for both 3.5 dBm on-chip input power and -12.5 dBm on-chip optical input power.

and  $A$  is a factor which determines the gain bandwidth. The gain as function of wavelength is shown in Fig. 5(a) for a current density of  $4.9 \text{ kA/cm}^2$ . The fit gives a 1 dB small-signal gain bandwidth of 20 nm. It is of course also essential to investigate the gain at very high output powers. Therefore we analyzed the gain of the 1.45 mm amplifier in a 20 nm band centered at 1575 nm. The gain as function of wavelength for the 1.45 mm SOA is shown in Fig. 5(b). We see that for an input power of 3 dBm, corresponding to an output power of  $> 17 \text{ dBm}$ , the gain ripple is less than 1 dB over a 20 nm span. Furthermore the gain ripple is similar for an input power of -12.5 dBm.

The passive losses of the optical mode shown in Fig. 1(b) and the tapers shown in Fig. 1(d) can be determined by performing a cutback measurement while the amplifiers are biased at transparency current density. At transparency current the quantum wells neither absorb or amplify, therefore any measured losses are caused by the passive waveguide layers (including

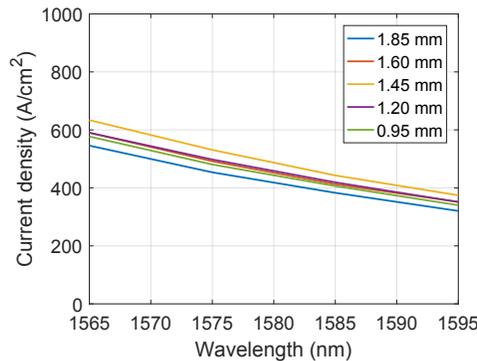


Fig. 6. Transparency current density measurement as function of wavelength for all 5 SOAs of different lengths.

free carrier losses). To measure the transparency current density of the amplifiers the method described in [20] was used. This method relies on measuring the voltage drop over the amplifier when it is being operated at constant current. If we inject the amplifier with the modulated output of a tunable laser, the voltage drop across the amplifier will also be modulated. If the modulation of the voltage drop across the amplifier is detected using a lock-in amplifier the phase can also be measured. If either the wavelength or the injection current is swept, the modulation will change sign for a given wavelength and current. This occurs at transparency because at that point the modulated laser output does not affect the carrier density or the voltage drop over the amplifier.

The transparency current density was determined for all 5 SOAs. The result is plotted as function of wavelength in Fig. 6. As can be seen in the plot, the transparency current density varies slightly but is not correlated to the length of the amplifier. In previous SOA designs we found that the taper introduced substantial surface recombination and the transparency current density depended on the amplifier to taper length ratio. From this we conclude that the taper design with wider quantum wells reduces this problem.

Using the measured transparency current of the amplifiers shown in Fig. 6, the passive losses of the amplifiers can be determined with a cut-back measurement. We find a III-V-on-silicon waveguide loss of  $18 \text{ cm}^{-1}$  and a taper loss of approximately 0.5 dB per taper at a wavelength of 1575 nm.

Finally we estimate the on-chip noise figure (NF) using the optical method detailed in [21] [22]. We chose to evaluate the on-chip NF instead of the external NF, as the amplifier was designed for implementation in a photonic circuit and not as a separate packaged device. However, if low-loss edge couplers would be used the amplifier could be envisioned to be used in a similar fashion as demonstrated in [14]. To determine the NF we use the OSA to measure the ASE for a given input power. Once the on-chip ASE power  $P_{ASE}$  in a band  $B_0$  is determined together with the on-chip gain  $G$ , the on-chip NF can be determined using the following formula:

$$NF = 10 \cdot \log_{10} \left( \frac{1}{G} + 2 \frac{P_{ASE}}{G h \nu B_0} \right) \quad (4)$$

where  $h$  is the Planck constant and  $\nu$  is the photon frequency. We find that the noise figure of both the 1.45 mm and 1.2 mm SOA is approximately 9 dB for high input powers ( $> 0 \text{ dBm}$  on-chip). This was measured using a injection current of  $4.9 \text{ kA/cm}^2$  corresponding to 237 mA for the 1.45 mm SOA and 175 mA for the 1.2 mm SOA. For input powers lower than -15 dBm (on-chip) the noise figure becomes smaller than 8 dB for both devices. Both noise figures were determined for an input wavelength of 1575 nm. This NF is comparable to, but lower than, the

on-chip noise figure ( $>10$  dB) reported for a high-gain III-V-on-silicon amplifier [14].

#### 4. Conclusion

In summary, we demonstrated a III-V-on-silicon SOA with a small-signal gain of 27 dB and a gain saturation power of approximately 17.24 dBm. 17.5 dBm waveguide-coupled output power is recorded, for a power consumption of 540 mW. This type of SOA can be integrated with advanced laser sources such as high-speed directly modulated lasers on the same PIC using the same epitaxial material. This device can therefore be of interest in several applications requiring high optical output power, including high-speed optical transceivers, microwave photonic systems and optical beamforming applications.

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