Sample title

Time-Resolved Photoluminescence Characterization of InGaAs/GaAs Nano-Ridges Monolithically Grown on 300 mm Si Substrates

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The monolithic growth of III-V materials directly on Si substrates provides a promising integration approach for passive and active silicon photonic integrated circuits (PICs) but still faces great challenges in crystal quality due to misfit defect formation. Nano-ridge engineering (NRE) is a new approach which enables the integration of III-V based devices on trench-patterned Si substrates with very high crystal quality. Using selective area growth (SAG) III-V material is deposited into narrow trenches to reduce the dislocation defect density by aspect ratio trapping (ART). The growth is continued out of the trench pattern and a box-shaped III-V nano-ridge is engineered by adjusting the growth parameters. A flat (001) GaAs nano-ridge surface enables the epitaxial integration of a common InGaAs/GaAs multi-quantum-well (MQW) structure as an optical gain medium to build a laser diode. In this study a clear correlation is found between the photoluminescence (PL) lifetime, extracted from time-resolved photoluminescence (TRPL) measurements, with the InGaAs/GaAs nano-ridge size and defect density, which are both predefined by the nano-ridge related pattern trench width. Through addition of an InGaP passivation layer, a MQW PL lifetime of up to 800 ps and 1000 ps is measured, when pumped at 900 nm (QWs only excited) and 800 nm (QWs + barrier excited) respectively. Addition of a bottom carrier blocking layer further increases this lifetime to ~ 2.5 ns (pumped at 800 nm), which clearly demonstrates the high crystal quality of the nano-ridge material. These TRPL measurements not only deliver a quick and valuable feedback about the III-V material quality but also provide an important understanding for the heterostructure design and carrier confinement of the nano-ridge laser diode.

I. INTRODUCTION

To fully exploit the potential of integrated silicon photonics, there is a need for light emitters directly integrated on silicon substrates. So far, only direct bandgap III-V semiconductors seem to offer a viable route towards realizing efficient and compact integrated optical amplifiers and lasers. Also, for various electronics applications such as high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs) or imagers, the integration of III-V on silicon substrates is explored. However, given the large lattice mismatch between silicon and all relevant direct bandgap III-V semiconductors, the monolithic growth of III-V materials on Si substrates suffers from the formation of misfit dislocations (MDs) and threading dislocations (TDs) accompanied by additional challenges typical in III-V/Si heteroepitaxy such as the formation of anti-phase domains (APDs) and planar defects (PDs). To overcome these problems, a thick buffer layer of germanium[1] or III-V compound materials[2–5] is often grown to reduce the defect density. Alternatively, sophisticated integration approaches like selective area growth (SAG) in highly confined patterns, epitaxial lateral overgrowth[6], deposition on V-groove-patterned substrates[7,8], III-V nanowire growth[9] or quantum-well-in-nanopillar growth[10] are used to confine the defect formation. Especially aspect ratio trapping (ART)[11,12]

in trenches was successfully applied to realize first III-V transistors on 300 mm Si substrates[13,14] but also explored for laser applications[15,16]. The heteroepitaxial growth in very narrow trenches is very beneficial to reduce the TD density but restricts the total volume of III-V material. In a novel approach called nano-ridge engineering (NRE), once the trench is filled the growth is continued out of the pattern whereat the growth conditions are adjusted such that specific nano-ridge shape is achieved[17,18]. The InGaAs/GaAs nano-ridges discussed in this paper are deposited with this technique. A GaAs nano-ridge including three InGaAs QWs is engineered above the oxide mask, which can support a low-loss and high-gain optical mode[19]. The huge advantage is that the nano-ridge device region on top of the oxide is clearly separated from the defect region inside the trench for sufficient aspect ratio. Details about the heteroepitaxial growth as well as extensive characterization of the crystal quality through scanning electron microscopy (SEM), transmission electron microscopy (TEM), electron channeling contrast imaging (ECCI) and photoluminescence (PL) spectroscopy were published before[17,20,21]. Single mode lasing at room-temperature (RT) from these InGaAs/GaAs nano-ridges with an InGaP passivation layer deposited around it was demonstrated[19]. All this work shows that ART in line with NRE can indeed lead to the integration of novel III-V nano-ridge laser devices on Si with sufficiently low defect densities.

The achieved crystal quality and performance of the fabricated nano-ridge devices are highly dependent on the dimensions and aspect ratios of the Si/SiO$_2$ trenches. When the height of the oxide mask is fixed, wider trenches with lower aspect ratio result in less efficient trapping of mis-

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fit defects and hence worse crystal quality of the nano-ridge material and the active layers. On the other hand narrower trenches lead to smaller nano-ridge dimensions with a higher surface-to-volume ratio and devices might suffer more from surface and/or interface related defects. Therefore, to systematically investigate how the crystal quality and device performance are linked to the trench width, we carried out detailed time-resolved photoluminescence (TRPL) experiments to extract the PL lifetime of the nano-ridges at both RT and low-temperature. In addition, we investigated how GaAs surface passivation layers and carrier blocking layers inside the nano-ridges impact the PL lifetime. The paper is arranged as follows: first the structure of the nano-ridges is explained in detail, followed by a description of the TRPL setup used for the experiments. Then we report how the measured PL lifetime varies as function of trench width for different nano-ridge heterostructures with and without passivation layer. We also show how an extra InGaP carrier blocking layer at the bottom of the nano-ridge can substantially increase the PL lifetime. Finally, low-temperature measurements confirm the impact of surface defects on the MQW PL lifetime in case of small nano-ridges structures.

II. NANO-RIDGE GROWTH

A trench pattern is fabricated based on an industrial shallow trench isolation (STI) process with a 300 nm thick SiO_2 layer on an exactly oriented (001) Si substrate 300 mm in diameter. The trenches are oriented along the two $\langle 110 \rangle$ orientations and are designed to have different lengths varying from 100 nm to 10 μm and widths varying from 20 nm to 500 nm. The ratio of the Si trench surface versus the total area is kept constant to 10%. Applying a tetramethylammonium hydroxide (TMAH) wet-etch step, a trench depth of about 280 to 300 nm is achieved with a V-shaped Si surface exposing two {111} facets at the bottom to suppress the formation of anti-phase domains at the GaAs/Si interface[22]. The deposition is carried out using metal organic vapor phase epitaxy (MOVPE) with tertiarybutylarsine, tertiarybutylphosphine, trimethylindium, triethylgallium and trimethylgallium as precursors. The heteroepitaxial growth starts with a thin GaAs nucleation layer deposited at low-temperature followed by the high-temperature growth of the main GaAs nano-ridge material, first inside and then outside of the trench in order to engineer box-shaped nano-ridges. These GaAs nano-ridges serve as a fully relaxed buffer for the pseudomorphic growth of the active region on top of the (001) surface, which consists of three compressively strained InGaAs QWs with about 20% indium and a layer thickness of 9-10 nm. During epitaxial growth all nano-ridge surfaces are exposed and three thin InGaAs layers are also deposited on the two {110} side facets, see zoom-in of FIG. 1 d). As the film thickness is only 1.5-2 nm no electron-hole pairs are confined and therefore these layers are not optical active. To suppress carrier losses through non-radiative recombination at the defective GaAs surfaces[23], all InGaAs/GaAs nano-ridges explored in this study except one are completed by depositing a lattice-matched InGaP passivation layer around the nano-ridges.

FIG 1 a)-c) show SEM pictures of cleaved nano-ridges with trench width 60 nm, 100 nm and 500 nm respectively. These images show clearly how the nano-ridge volume (V) is growing faster than the surface area (S). Hence, an increasing trench width is accompanied with a decreasing surface-to-volume ratio S/V. FIG 1 d) is a high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the nano-ridges. The location of the QWs is clearly visible. The thickness of the InGaP cap layer on the {001} and {110} planes is almost equal whereas the InGaP growth rate on the bottom {111} planes is strongly suppressed, resulting in a negligible thickness of the passivation layer along the bottom sides of the nano-ridge (see inset of FIG. 1 d)).

The main strain release, required due to the 4.1% lattice mismatch between GaAs and Si, is accomplished by a high density of MDs along the V-shaped GaAs/Si interface[24]. Remaining strain fields inside the GaAs bulk lead to the nucleation of TD half-loops during growth. Mobile and glissile TDs glide along the {111} planes while the half-loop expands and are finally trapped at the trench side walls for a sufficient trench aspect ratio[21]. Taking into account the angle of 54.7° between the {111} planes and the substrate surface, an aspect ratio of 1.43 is the minimum value to achieve full TD trapping in an ideal case. However, most of the time remaining strain fields initiate the nucleation of dislocation half-loops in the GaAs volume with a certain distance to the GaAs/Si interface, which implies that a higher aspect ratio than 1.43 is needed. Applying ECCI for the defect characterisation of GaAs nano-ridges exploring different trench widths revealed a TD density at the nano-ridge surface of less than 3×10^6 cm^{-2} for the growth in 100, 120 and 150 nm wide trenches[21] corresponding to an aspect ratio of 3, 2.5 and 2 (based on 300 nm oxide thickness). This defect density value is limited by the investigated scan area, hence, the proper TD density could be even lower. The correlation between trench width and ART of TDs is shown in FIG. 2 a) and b). FIG. 2 a) is a bright field (BF) TEM image of a complete MQW device stack grown on top of a 100 nm wide trench whereas b) is an image of the same structure deposited in a 200 nm wide trench. The blurry lines are caused by TDs and the surrounding strain fields. The white arrow indicates the extension of the trench oxide. In FIG. 2 a) all TDs are still trapped inside the trench and the nano-ridge material outside the 100 nm wide trench is free of defects. In the case of the 200 nm wide trench (b)), TDs start to exceed the oxide height and penetrate into the nano-ridge. Therefore, even an aspect ratio of 1.5 is still not enough to fully confine the TDs inside the trench. However, the MQW structure seems to be less affected and remains defect-free in this image. The inset is a dark field (DF) STEM image of the MQW stack of sample b) emphasising the uniform composition profile and abrupt QW interfaces. If the trench width increases to 500 nm, (aspect ratio of 0.6) the TD density at the nano-ridge surface reaches values up to 3×10^8 cm^{-2} based on an ECCI inspection[21], hence the MQW region will be also defective. PDs, such as stacking faults and micro twins, are also easily nucleated in heteroepitaxy at the III-V/Si surface. Origins of PDs are remaining impurities at the interface and/or a
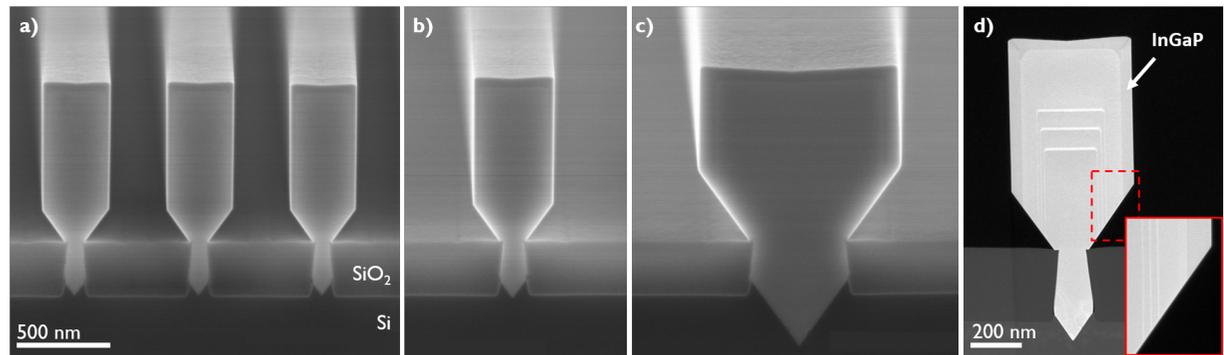
FIG. 1. a)-c) show SEM pictures of cleaved nano-ridges with trench width 60 nm, 100 nm and 500 nm respectively (same scale). d) is a HAADF-STEM image of the reference nano-ridge denoted as S_{Ref} on top of a 100 nm wide trench with 3 InGaAs QWs which are 9-10 nm thick and a 50 nm thick InGaP passivation layer. The Si substrate, the STI oxide, the 3 QWs and the InGaP passivation layer can be clearly identified. The inset is a zoomed-in image of the {111} facet where the InGaP-layer is very thin.

non-optimal seed layer. Currently a density of $0.2 - 0.45 \, \mu m^{-1}$ is reported for GaAs nano-ridges[21]. PDs are less destructive on device performance as no open crystal bonds are involved, hence, we expect the main impact on the time-resolved PL is rather caused by the presence of MDs and TDs.
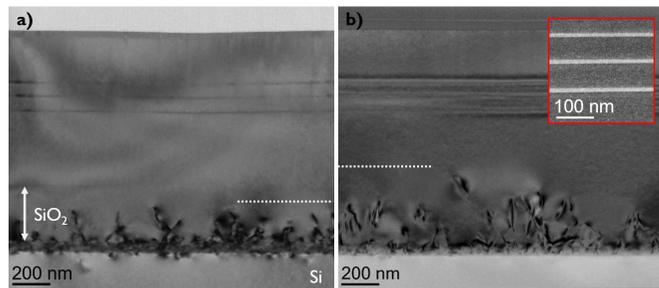
FIG. 2. a) is a bright field (BF) (220) TEM image of a lateral cut along the nano-ridge of the reference structure deposited on top of a 100 nm wide trench (aspect ratio of 3). b) is a BF (004) image of the reference structure based on 200 nm wide trenches (aspect ratio of 1.5). The arrow indicates the extension of the 300 nm thick trench oxide, which is the same for a) and b). The white dashed line marks the penetration height of TDs, which are visible by the blurry lines, and obviously larger in the case of the 200 nm trench width. The inset of b) is a zoom-in dark field (DF) STEM image showing the defect-free MQW region.

III. TIME-RESOLVED PHOTOLUMINESCENCE MEASUREMENT

The nano-ridges were characterized by the time-resolved photoluminescence setup shown in FIG. 3 a). A Mira-HP high-power wavelength-tunable $(680 - 1000 \, nm)$ Titanium:Sapphire (Ti:Sa) laser emitting ~ 200 fs pulses at a repetition rate of 76 MHz is used as the pump source. After traveling through a 1 m long optical fiber, the pulses are broadened to ~ 1 ps, still substantially shorter than the lowest lifetimes measured in the nano-ridges. At the detection side, a spec-

trometer with a 2 nm resolution and a streak camera (up to 2.3 ps time resolution) are used. Mirror M1 and lens L1 generate an approximately circular pump spot with $\sim 200 \, \mu m$ diameter on the sample surface. Lenses L2, L3 are inserted between the sample and the spectrometer to couple the photoluminescence signal into the spectrometer while the filter blocks out the pump light. For low-temperature measurements, the samples are positioned in a cryo chamber at 80 K.

FIG. 3 b) shows the TRPL spectrum of the reference sample S_{Ref} (trench width 100 nm, no InGaP blocking layer, pump power $500 \, \mu W$). By integrating the signal over a certain time range, one can get the PL spectrum for that time interval. Vice-versa, by integrating over a certain wavelength range, one gets the time dependent PL signal. As an example, FIG. 3 c) shows the time dependent PL signal, integrated over the wavelength range from 872 nm to 1200 nm. As 872 nm (1.42 eV) is the bandgap of bulk GaAs at room-temperature, this signal can be considered originating mainly from the InGaAs QW layers. To extract the PL lifetime from these curves, the background is subtracted from the detected signal and a one-term exponential model

$$I_{QW} = A \cdot e^{\frac{-(t-t_0)}{\tau_{QW}}}$$

is fitted to the experimental data, with I_{QW} the PL intensity integrated over the wavelength range 872 nm to 1200 nm, t the time, t_0 the moment when I_{QW} peaks, A a fitting parameter and τ_{QW} the decay time for the QW emission. The range over which the curve is fitted varies from sample to sample but is chosen to start from the time where the intensity peaks (t_0) and to end when the signal reaches $1/10$ of its peak value to exclude the noisy signal in the low intensity tail. Similarly one can extract the life time τ_{GaAs} for the PL originating from the GaAs nano-ridge by integrating the TRPL signal over the wavelength range from 825 nm to 872 nm.
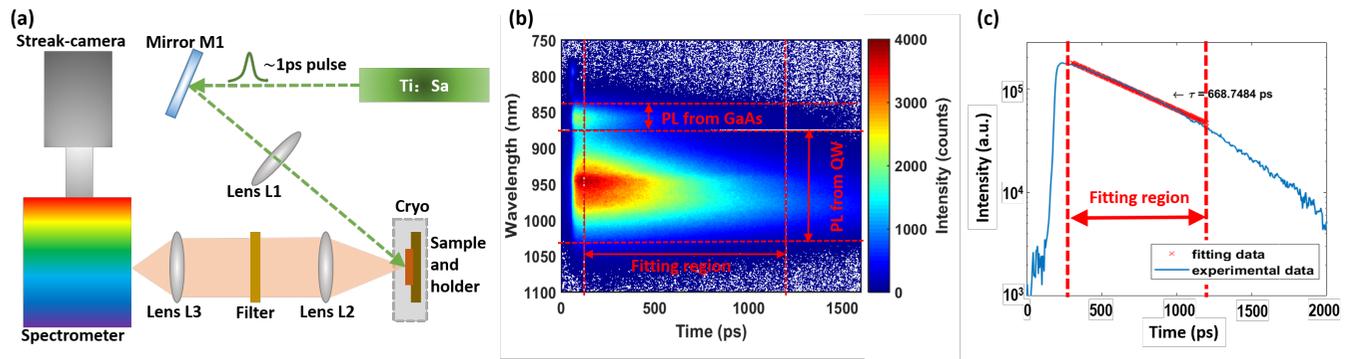
FIG. 3. a) Schematic diagram of the TRPL setup. The cryo chamber is only used for the low-temperature measurements. b) Example of an experimental TRPL spectrum. The horizontal dashed lines indicate the integration ranges to obtain the PL lifetime originating from the QWs and the GaAs nano-ridge respectively. The vertical lines indicate the range over which the lifetime is fitted. c) Integrated PL originating from the QWs (wavelength range 872 nm to 1100 nm) as a function of time. The region between the dashed lines indicates the fitting range.

A. Impact of Trench Size

In a first experiment we determined the PL lifetimes τ_{QW} and τ_{GaAs} of the reference sample S_{Ref} with 3 $In_{0.2}Ga_{0.8}As$ QWs and a ~ 50 nm thick InGaP passivation layer, as a function of the trench width, excitation wavelength and pump power. The results for $10\,\mu m$ long nano-ridges are summarised in FIG. 4. FIG. 4 a) shows the lifetimes τ_{QW} and τ_{GaAs} for a fixed excitation power of $500\,\mu W$ versus the trench width changing from 20 nm to 500 nm comparing results based on the excitation wavelength of 800 and 900 nm.

For the excitation wavelength of 800 nm (1.55 eV), carriers are excited both in the GaAs nano-ridge material (bandgap 1.42 eV at RT) and in the QWs, while for the 900 nm (1.38 eV) pump wavelength electron-hole pairs are only generated in the QW material. Considering first the excitation wavelength of 800 nm, which allows to define the PL lifetime of the QWs as well as for the GaAs material, τ_{QW} is always larger than τ_{GaAs}. This is caused by the fact that carriers from the GaAs barrier also escape into the QWs, hence, this loss mechanism reduces the PL lifetime of GaAs additionally to all other loss paths e.g. caused by crystal defects. τ_{QW} as well as τ_{GaAs} peak for a trench width of 150 nm, and τ_{QW} reaches a value of about 1 ns. For wider trenches with lower aspect ratio both PL lifetimes decrease below 400 ps for 500 nm wide trenches due to the pronounced increase in TD density inside the nano-ridge material. But also for the smaller trench widths the PL lifetimes of the QWs and GaAs material quickly decrease. This effect cannot be correlated to the presence of dislocation defects inside the bulk of the nano-ridges as the aspect ratio is rising for smaller trench width. Therefore we believe that the decrease is linked to a growing impact of surface defects inducing non-radiative recombination as smaller nano-ridges exhibiting a large S/V ratio. Another carrier loss path is the leakage inside the defective trench region caused by MDs and TDs close to the III-V/Si interface, whose relative capture efficiency increases for smaller trench width. Furthermore we notice that the PL lifetime τ_{QW} for an excitation wavelength of 800 nm is slightly longer than that for an excitation wave-
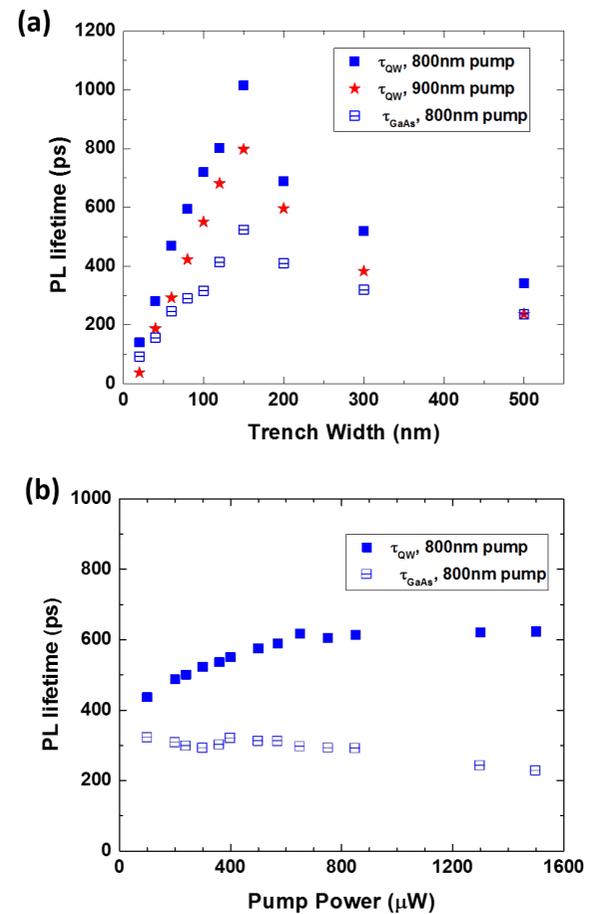

FIG. 4. a) PL lifetime versus trench width for the reference sample S_{Ref}, measured at room-temperature under 800 nm and 900 nm excitation wavelength respectively. The excitation power is $500\,\mu W$. b) PL lifetime as a function of excitation power for a trench width of 80 nm.

length of 900 nm. We believe this can be associated with car-

riers being excited in the GaAs diffusing towards the QW in the case of pumping at 800 nm, thereby extending τ_{QW}. This "QW feeding" with additional carriers from the GaAs barrier is not possible with 900 nm excitation wavelength, which is below the bandgap of GaAs. The effect of "QW feeding" is also visible in FIG. 4 b), which depicts the measured PL lifetime of τ_{QW} and τ_{GaAs} versus the pump power for an excitation wavelength of 800 nm. The lifetime for the PL originating from the QWs first increases and then saturates for pump powers beyond 700 μW. We believe that increasing the pump power generates more electron-holes pairs in the GaAs nanoridge material, which amplifies the impact of carriers diffusing to the QWs and thereby prolongs the PL lifetime. τ_{GaAs} decreases slowly with rising pump power. In all further experiments, to ensure a sufficient signal intensity and at the same time the integrity of the sample, the pump power is set to 500 μW.

Finally we investigated the impact of the trench length. By characterizing τ_{GaAs} for nano-ridges with trench length varying from 100 nm to 10 μm, we found a clear decrease in PL lifetime for a trench length below 3 μm. The TMAH etch step, which is applied to form a V-shape Si bottom, reveals also two {111} facets at the ends of the trenches and perpendicular to the trench orientation. These facets induce anti-phase disorder inside the GaAs material which can cause additional carrier losses at the anti-phase boundaries. Furthermore, the box-shaped nano-ridges reveal different facets at the two nano-ridge ends as more crystal facets contribute to the nano-ridge formation. The layer thicknesses as well as the interface qualities of the different heterolayers are unknown and not controlled, hence, additional crystal and/or surface defects might be nucleated. Both anomalies might explain the strong lifetime reduction for short trenches. In all further experiments we focused on 10 μm long nano-ridges.

B. Impact of Passivation Layer

As shown in FIG. 1, the reference sample S_{ref} has a 50 nm thick InGaP (bandgap 1.76 eV at 300 K) passivation layer grown around the nano-ridge lattice-matched to GaAs. To investigate the impact of this layer, we compared S_{ref} with a sample without passivation layer denoted $S_{0\times Cap}$ and a sample with a 100 nm thick passivation layer $S_{2\times Cap}$. The results for τ_{QW} and τ_{GaAs} are shown in FIG. 5 a) and b). For the sample without passivation layer, the PL lifetime drops by a factor 8 compared to the reference sample. This shows the effectiveness of the InGaP passivation layer in reducing non-radiative recombination at the GaAs-air interfaces. Increasing the thickness of the passivation layer to 100 nm does not further improve the lifetime, indicating that the 50 nm passivation layer is sufficient to avoid carriers tunneling to the InGaP-air interface. Also thermal excitation of the carriers over the GaAs-InGaP barriers seems unlikely, given the large band-offsets between both materials. This leaves the GaAs-InGaP interface as a possible source for carrier losses. However, very low recombination rates of 1.3×10^{-3} cm/s to 2 cm/s have been reported in literature for this interface[25,26]. This points

to the imperfectly passivated {111} facets at the bottom of the nano-ridge and leakage losses to the defective trench as the most likely carrier loss channels in the passivated samples for nano-ridges based on a trench width below 150 nm.
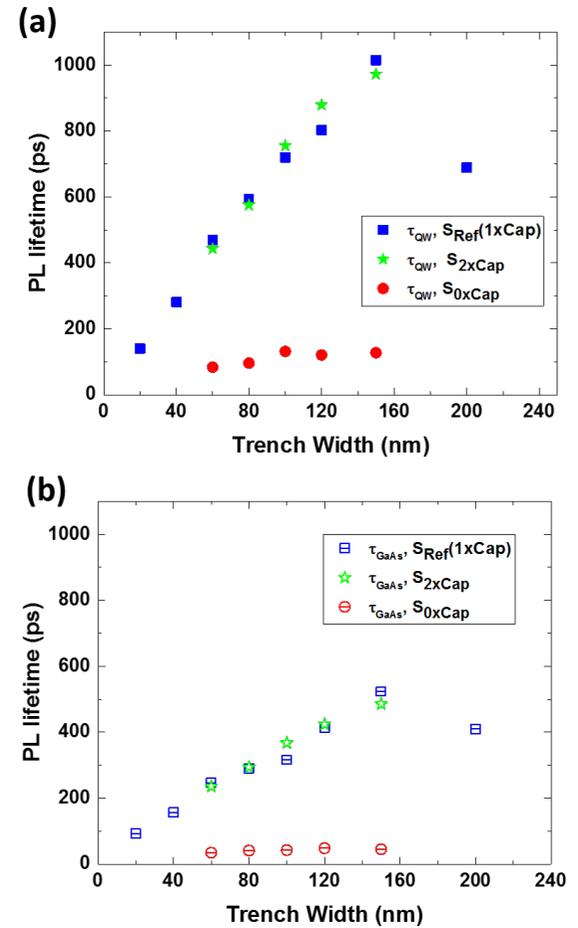

FIG. 5. Room-temperature PL lifetime from the reference sample (S_{ref}) with 50 nm InGaP passivation layer, the sample without passivation layer $S_{0\times Cap}$ and the sample with 100 nm $S_{2\times Cap}$ passivation layer. a) Lifetime τ_{QW} for QW PL emission and b) τ_{GaAs} for GaAs.

C. Impact of Carrier Blocking Layer

To investigate the implication of carrier losses into the defective trench region, an InGaP carrier blocking layer lattice-matched to GaAs is included in the nano-ridge before the QW growth in this specific sample. This layer is clearly visible in FIG. 6 a), which holds a cross section SEM image of a nano-ridge grown in 80 nm wide trenches. Given its large bandgap, this layer serves as a barrier preventing carriers from diffusing into the trench. To keep the nano-ridge size constant, this sample includes only 2 QWs. Therefore another control sample, identical to the reference sample described above but only including 2 QWs was prepared. FIG. 6 b) compares the trench

width dependent PL lifetimes for the reference sample with 3 QWs (S_{ref}), the control sample with 2 QWs ($S_{2\times QW}$) and the sample with InGaP blocking layer (S_{blk}). The measured lifetimes for S_{ref} and $S_{2\times QW}$ are identical, showing that reducing the number of QWs has no impact on the PL lifetime. Introducing now the barrier layer underneath the QWs clearly increases the PL lifetime. It shifts the optimal trench width defined by the maximal PL lifetime of 150 nm to 100 nm and leads to more than a doubling of the maximum lifetime values. This shows that carrier losses towards the defective trench region has a considerable impact on the carrier lifetime but also that very long PL lifetimes, above 2 ns can be reached in the nano-ridge, proving the high quality of the material.
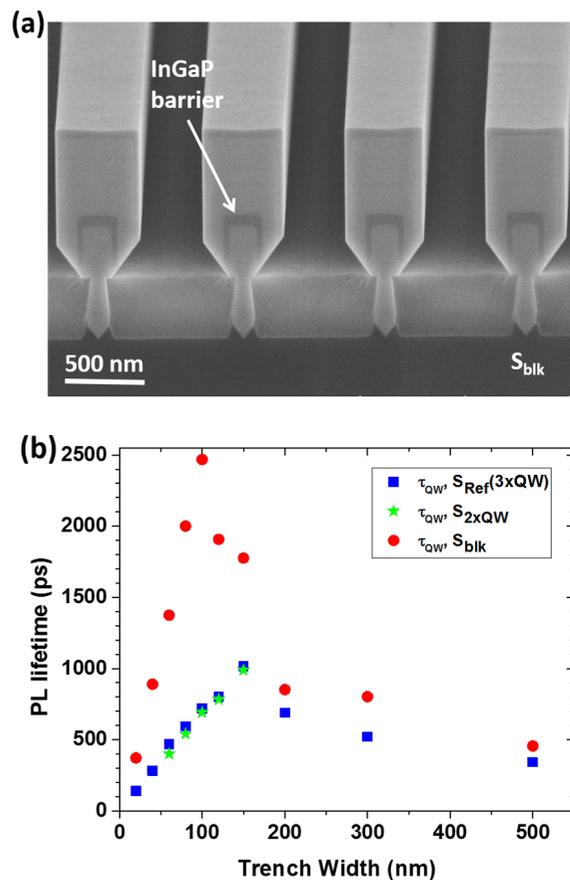
FIG. 6. a) XSEM image of nano-ridge with 2 QWs and an extra InGaP blocking layer (sample denoted as S_{blk}). b) PL lifetime of sample S_{Ref}, $S_{2\times QW}$ and S_{blk}.

D. Low-temperature characterization

To confirm that the strongly decreasing lifetime for smaller trench widths is indeed related to surface effects and not to an increasing number of defects in the MQW stack itself, we carried out TRPL measurements of the samples with and without passivation layer at low-temperature (80 K). At this temperature, we expect the carriers to have insufficient thermal energy to escape from the InGaAs QWs and hence the measured lifetime should be dominated only by the material quality of the QW and not by surface defects or the highly defective trench region close to the III-V/Si. For this experiment the sample was placed in a cryo chamber, which reduced both the excitation and the collection efficiency. To get some insight in how this influences the measurements, FIG. 7 a) shows the PL spectra measured before and after mounting the reference sample inside the cryostat, in the latter case both at 300 K and at 80 K. As the excitation efficiency declines, the RT spectrum of the sample inside the cryo chamber narrows down and is slightly red-shifted as less electron-hole pairs are generated leading to less band filling. The reduced collection efficiency results in a more noisy spectrum at RT. By cooling the sample down to 80 K, the bandgap energy of all materials increases as illustrated by a simplified band diagrams in FIG. 7 b). To compensate for this, we shifted the excitation wavelength to 750 nm. Comparing the PL spectra at 80 K with the one at RT in FIG. 7 a) reveals that the PL peak is indeed blue-shifted by 63 nm as expected. Given the relatively low pump efficiency in the cryo chamber, the GaAs peak which was visible in the RT spectrum taken in the free space setup is no longer present in the 80 K spectrum. Further, the intensity of the spectrum at 80 K increases compared to the RT spectrum taken in the cryostat, which we attribute to an increased radiative recombination efficiency. To cope with the increased background noise in the TRPL measurements, it was explicitly included in the fitting function

$$I_{QW} = I_{bg} + A \cdot e^{\frac{-(t-t_0)}{\tau_{QW}}}$$

This additional fitting parameter and the higher noise increased the uncertainty on the fitted lifetimes to $\Delta\tau_{QW} \approx \pm 50\,ps$. FIG. 7 c) shows the measured PL lifetimes as a function of the trench width for the reference sample S_{Ref} and the sample without passivation layer $S_{0\times Cap}$. At 80 K the lifetimes measured for both samples are identical within the measurement error. Furthermore the lifetime seems to be independent of the trench width, at least up to 200 nm. This is in strong contrast with the RT results shown in FIG. 4 a) which exhibit a very pronounced trench width dependence and a strongly reduced lifetime for the sample without InGaP passivation layer. This confirms our hypothesis that the reduction in lifetime with decreasing trench width is related to non-radiative recombination at the imperfectly passivated bottom {111} facets and/or to carrier losses in the highly defective trench region and not to a decrease in material quality of the nano-ridge material. Currently is it not possible to judge, if carrier recombination at the non-passivated bottom facet or the leakage into the trench is dominating the PL lifetime decrease. No reduction in PL lifetime is observed for the trench width of 200 nm, for which the aspect ratio is not sufficient to fully restrict all dislocation defects inside the trench. This can be explained by the fact that for this width dislocation defects start penetrating the GaAs nano-ridge but not yet the InGaAs MQW stack where the carriers are confined at low-temperature (see FIG. 2).
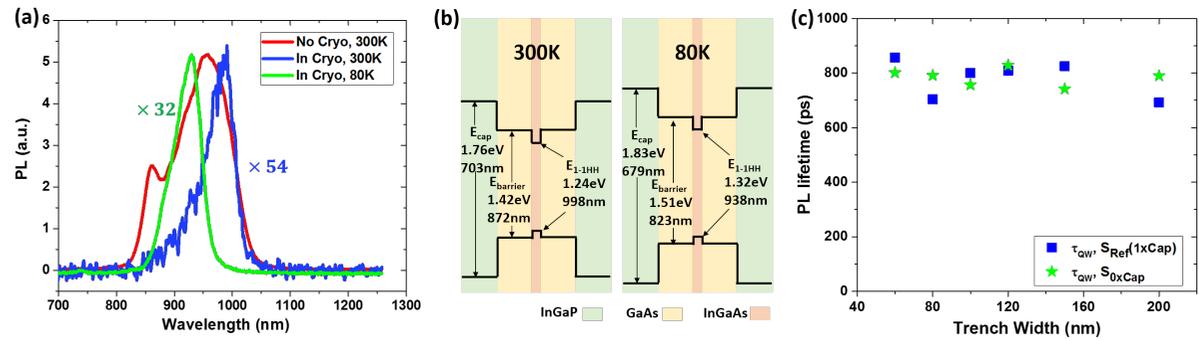
FIG. 7. a) Normalized spectra of sample S_{Ref} with 100 nm trench in the free space setup at 300 K (red), and in the cryo chamber at 300 K (blue) and at 80 K (green) respectively. The 300 K and 80 K spectra are taken with a 800 nm and 750 nm excitation wavelength respectively. b) Calculated energy diagram of the nano-ridge heterostructure at 300 K and 80 K. Only one QW is plotted, while the actual samples have have 3 QWs. For the QW we plotted the energy of the first quantized energy level in the conduction and heavy hole band. c) PL lifetime of sample S_{Ref} and $S_{0 \times Cap}$ as a function of trench width at 80 K. The excitation wavelength is 750 nm.

IV. CONCLUSION

To conclude, we characterized the PL lifetime of InGaAs QWs embedded inside a GaAs nano-ridges monolithically integrated by SAG on 300 mm trench-patterned Si substrate. The lifetime was characterized on a TRPL set-up at both room-temperature (300 K) and low-temperature (80 K). The influence of the trench width, defect density, nano-ridge size as well as of the heterostructure was studied in detail. A strong dependence of the PL lifetime on the trench width is observed as the trench width defines the dislocation defect density in the nano-ridge material as well as the nano-ridge size and therefore the surface-to-volume ratio. For wider trenches the PL lifetime decreases because the nano-ridge material is penetrated by dislocation defects as the aspect ratios of the trenches are not sufficient, while for narrower trenches the larger surface-to-volume ratios lead to an increased impact of carrier losses towards the defective trench region and of non-radiative recombination processes at surface defects. For the 300 nm thick SiO_2 mask layer used in this work, this trade-off leads to an optimum trench width of 150 nm and PL lifetimes above 1 ns under 800 nm-wavelength excitation whereby both QWs and barrier layers are pumped. With the pump at 900 nm, whereby only carriers in the QWs are excited, the PL lifetime slightly reduces to 0.8 ns. An InGaP passivation layer deposited around the nano-ridge seems to be essential to prevent carrier losses at the GaAs-air surface. Without this layer the PL lifetime drops by a factor 8 compared to the reference structure with the 50 nm passivation layer. Increasing the thickness to 100 nm had no further influence. Adding a blocking layer to prevent carrier losses to the defective trench region further increased the PL lifetime to values above 2 ns under the 800 nm-wavelength excitation. Finally, through low-temperature measurements which showed a constant PL lifetime for trench widths below 200 nm, we could show that the decrease in PL lifetime for decreasing trench width at room-temperature is indeed caused by non-radiative recombination at an imperfectly passivated bottom

{111} surface and/or carrier losses into the defective trench region. All these results are crucial to understand the correlation between carrier loss processes inside the nano-ridge material and the heterostructure design, the nano-ridge size and the defect density inside the optical gain medium. It confirms that ART along with NRE enables the integration of high quality III-V nano-ridge material on Si substrates for future device integration especially in silicon photonics but also beyond that.
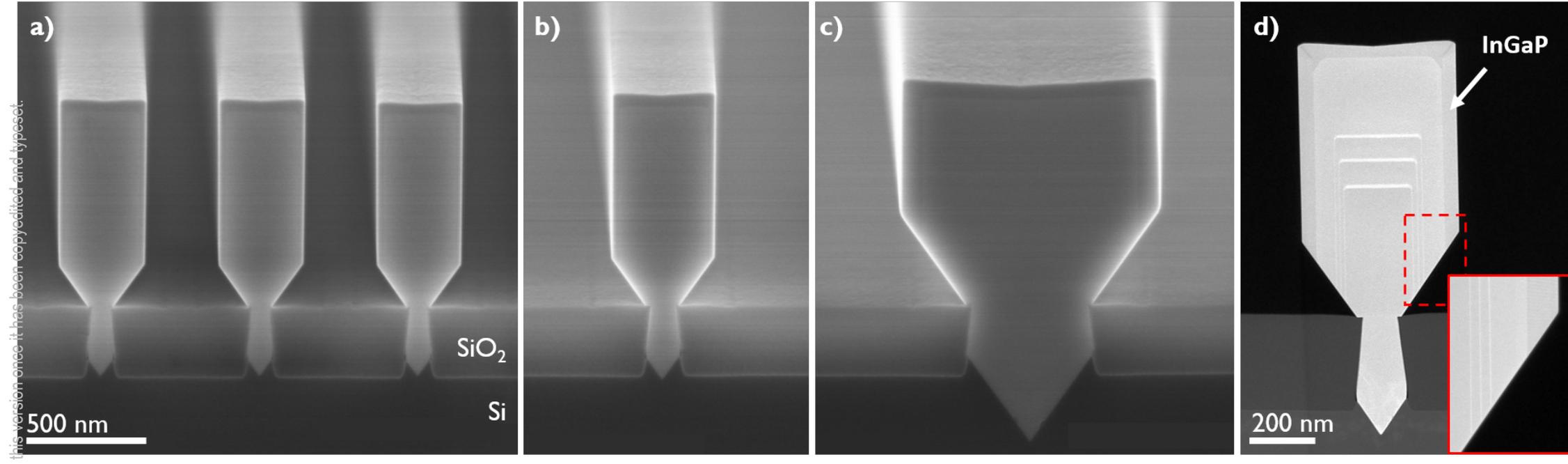
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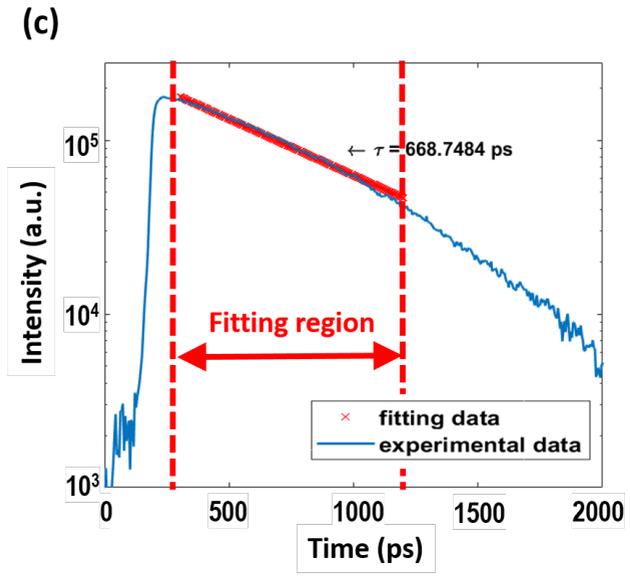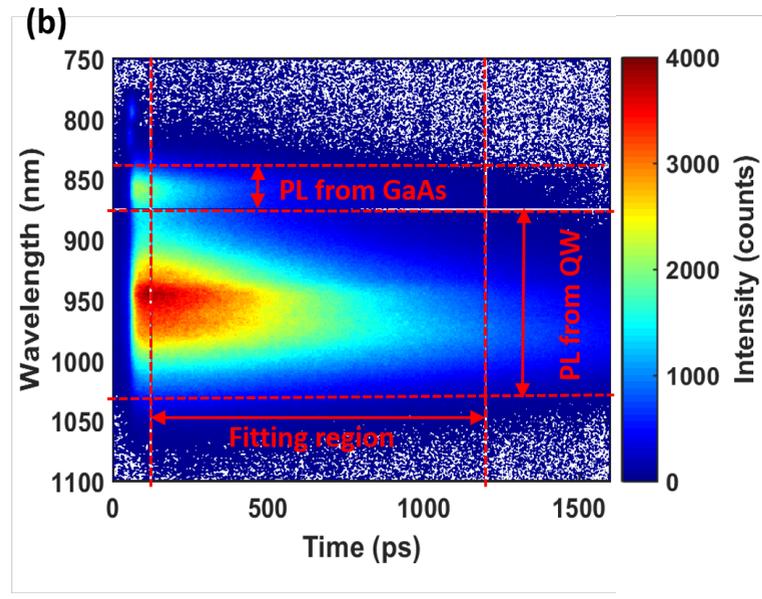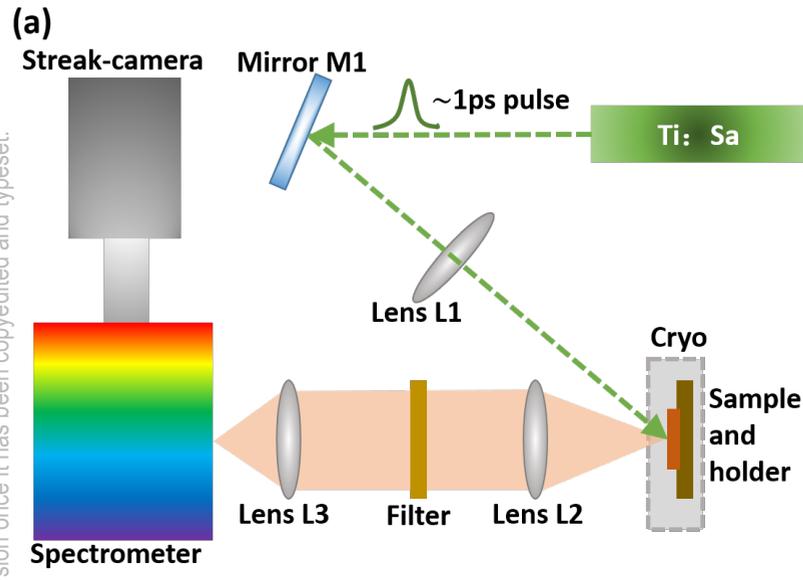
AIP
Publishing

(a)

Streak-camera

Mirror M1

~1ps pulse

Ti: Sa

Lens L1

Cryo

Sample and holder

Lens L3   Filter   Lens L2

Spectrometer

(b)

PL from GaAs

PL from QW

Fitting region

Wavelength (nm)

Time (ps)

Intensity (counts)

(c)

← τ = 668.7484 ps

Fitting region

fitting data
experimental data

Intensity (a.u.)

Time (ps)

(a)

(b)

(a) InGaP barrier

500 nm

S_{blk}

(b)

PL lifetime (ps) vs Trench Width (nm)

- τ_{QW}, S_{Ref}(3xQW)
- τ_{QW}, S_{2xQW}
- τ_{QW}, S_{blk}

(a)

(b)

(c)