

Article

Nano-Ridge Engineering of GaSb for the Integration of InAs/GaSb Heterostructures on 300 mm (001) Si

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Received: 21 March 2020; Accepted: 20 April 2020; Published: 22 April 2020



Abstract: Nano-ridge engineering (NRE) is a novel heteroepitaxial approach for the monolithic integration of lattice-mismatched III-V devices on Si substrates. It has been successfully applied to GaAs for the realization of nano-ridge (NR) laser diodes and heterojunction bipolar transistors on 300 mm Si wafers. In this report we extend NRE to GaSb for the integration of narrow bandgap heterostructures on Si. GaSb is deposited by selective area growth in narrow oxide trenches fabricated on 300 mm Si substrates to reduce the defect density by aspect ratio trapping. The GaSb growth is continued and the NR shape on top of the oxide pattern is manipulated via NRE to achieve a broad (001) NR surface. The impact of different seed layers (GaAs and InAs) on the threading dislocation and planar defect densities in the GaSb NRs is investigated as a function of trench width by using transmission electron microscopy (TEM) as well as electron channeling contrast imaging (ECCI), which provides significantly better defect statistics in comparison to TEM only. An InAs/GaSb multi-layer heterostructure is added on top of an optimized NR structure. The high crystal quality and low defect density emphasize the potential of this monolithic integration approach for infrared optoelectronic devices on 300 mm Si substrates.

Keywords: III-V on silicon; monolithic III-V integration; heteroepitaxy; infrared laser; MOVPE; InAs/GaSb heterostructure

1. Introduction

Silicon photonics provides an integrated platform of optical components which profits from mature complementary metal oxide semiconductor (CMOS) process technology to fabricate photonic devices in high volume and with high yield. Another advantage is the high refractive index contrast of silicon-on-insulator (SOI) waveguides, which enables a very dense integration of photonic components [1,2]. Conversely, the narrow bandgap of the compound semiconductor GaSb and related heterostructures is commonly utilized for optoelectronic devices in the infrared (IR) wavelength regime [3–7]. Hence, the monolithic integration of GaSb-based heterostructures on Si substrates would lead to cost-efficient on-chip sensing applications which take advantage of the unique optoelectronic properties of III-V materials on the one hand and of the established and scalable fabrication of

silicon-based photonics integration circuits (PICs) on the other hand. In particular, compact sensors for biomolecule and trace gas detection are of great interest in the short- to mid-IR waveband range from 2 to 4 μm . Therefore, the heteroepitaxial deposition of GaSb and related type-I heterostructures on Si substrates to realize IR laser sources and photodetectors would finally lead to fully integrated optical sensors. In addition, the monolithic growth of InAs/GaSb type-II superlattices (T2SL) for cooled IR imager applications would open up the door to higher integration density, more advanced large-scale device fabrication and reduced substrate cost [8,9].

Today, the most common way to integrate III-V materials on Si substrates is based on different kinds of bonding approaches such as chip-to-wafer or die-to-wafer [10,11], having their main challenges in process complexity and the limitation in co-integration with CMOS. The heteroepitaxial growth of III-V layers directly on Si substrates could offer a solution to these disadvantages but suffers from defect formation due to plastic relaxation. This is caused by the large difference in the lattice constant and thermal expansion coefficient of III-V compound materials compared to Si. As optoelectronic device performance degrades quickly with the presence of relaxation defects, it is important to achieve a high crystal quality in the active device area and to separate the latter clearly from the region of plastic relaxation. Different methods have been investigated to reduce the defect density in the active layer stack, e.g., the growth of a thick metamorphic buffer or the implementation of defect filter layers such as strained layer superlattices [4,12–14].

The lattice mismatch between III-Sb compound materials and Si is quite large with more than 12%. In addition, antimonides are very soft [15,16] and have a reduced activation energy to form misfit defects in comparison to III-V-arsenides and -phosphides, as the III-Sb bond energy is lower [17,18]. All this promotes the formation of 90° misfit dislocations to release the mismatch strain.

Different research groups have reported [19–21] that under optimized growth conditions for AlSb or GaSb on a (001) Si surface, a periodic interfacial misfit (IMF) array of 90° misfit dislocations is formed at the III-Sb/Si interface, leading to a GaSb film with a very low defect density on the top of this array. If this IMF array releases the entire strain in the III-Sb heterofilm, no micrometer thick buffer layer on Si is needed to reduce the defect density, which is a significant advantage for device co-integration on a silicon photonics platform. Balakrishnan et al. [22] claimed a threading defect density of about $\sim 1 \times 10^6 \text{ cm}^{-2}$ after the deposition of around 1 μm AlSb/GaSb on Si [12]. Relaxation via an IMF array is also possible for GaSb deposited on GaAs substrates, although the lattice mismatch is only 7.8%. A defect density of only $7 \times 10^5 \text{ cm}^{-2}$ was reported for a $\sim 200 \text{ nm}$ thin GaSb layer on GaAs [23].

A fundamentally different approach to control plastic relaxation in III-V heteroepitaxy on Si is selective area growth (SAG) in highly confined patterns [12,24–26]. In particular, the III-V growth in trenches with a high aspect ratio (AR) (trench height/trench width) is of great interest for photonic applications in the C- and O-band [27–29]. Dislocation defects are blocked at the side wall of the pattern by aspect ratio trapping (ART) [12], and the III-V ridge lines serve as waveguides which simplify the light coupling into passive waveguides [30]. Usually, the trench pattern is fabricated utilizing a silicon oxide (SiO_2) layer on top of a Si wafer or a SOI substrate. If the Si surface at the trench bottom is etched into a V-shaped groove exposing two {111} facets (for a trench orientation along $\langle 110 \rangle$ directions), no antiphase disorder is formed inside the III-V layer [31,32].

The growth of GaSb in trenches has been explored by different research groups. Orzali et al. [33] reported about the growth of GaSb in $\sim 90 \text{ nm}$ wide trenches with a V-grooved Si bottom fabricated in a 180 nm thick SiO_2 layer. Before depositing GaSb, the trenches were filled halfway with a GaAs buffer, evolving a V-shaped surface with two top-oriented {111} facets. It was shown that the GaSb relaxation occurs through the formation of an array of 60° misfit dislocations along the two {111} GaSb/GaAs interface planes. A transmission electron microscopy (TEM) inspection across several trenches did not show any indication of threading dislocations in the $\sim 100 \text{ nm}$ thick GaSb layer. Li et al. [34] describe the GaSb growth in a comparable trench pattern (90 nm trenches width, 145 nm oxide thickness), but only a 7 nm thin GaAs nucleation layer was applied as a seed covering the two {111} Si facets. The strain release of the GaAs seed layer on top of the {111} Si surface occurs via stacking fault and

micro twin formation [35–37], whereas the plastic relaxation of GaSb happens again by the formation of a 60° misfit array along both {111} GaSb/GaAs interfaces. In their work, the TEM investigation was also extended to a TEM-lamella preparation in a direction along the trench lines, which provides slightly better defect statistics, and a few threading dislocations were occasionally found in the top GaSb region. The formation of planar defects such as stacking faults and micro twins is also reported in both studies [33,34], which are nucleated at the GaSb/GaAs interfaces.

In our first investigation of GaSb SAG in V-grooved Si/SiO₂ trenches [38], we observed that the direct deposition of GaSb on Si does not easily lead to a good crystal quality and high selectivity, whereas the application of a thin InAs or GaAs seed layer clearly improves the GaSb integration on Si. Another important conclusion was that higher substrate temperatures are beneficial for the GaSb overgrowth to suppress planar defect formation. Although we did not find any indication of threading dislocations in the top GaSb region, we have to be aware that a TEM investigation provides a poor defect statistic (plan view TEM is not useful in SAG with large trench separation). Other faster techniques are necessary to better characterize the defect density and to further improve the heteroepitaxy for device application.

In this paper we apply nano-ridge engineering (NRE) [39,40] to GaSb grown out of narrow trenches using metalorganic vapor phase epitaxy (MOVPE). As the growth rate hierarchy on the different NR facets is determined by the applied deposition conditions, the deliberate adjustment of the MOVPE parameters allows the NR shape to be engineered according to our needs. In this way, the III-V nano-ridge (NR) volume can be increased on top of the trench pattern, and at the same time, a large (001) GaSb surface can be achieved. A pronounced (001) top surface enables a defect analysis based on electron channeling contrast imaging (ECCI), which delivers very good defect statistics compared to a transmission electron microscopy (TEM) study. In addition, we implemented an InAs/GaSb multi-layer stack on top of these GaSb NRs with a very high heterolayer crystal quality, which clearly points towards the opportunities of GaSb NRE for IR device integration on Si.

This paper is structured as follows. Firstly, we will review the defect density in our state-of-the-art GaAs NR as a function of trench width and, hence, AR. These results will be compared with the defect density in GaSb NRs, applying different seed materials and a buffer layer. The overall trend for the defect density in GaSb as a function of trench width is comparable to GaAs, although the kind of defects being initiated in the GaSb NRs depends on the chosen seed layer, which will be discussed in detail. NRE leads to the formation of different NR shapes, from which the box profile with a broad top surface was chosen for the integration of an InAs/GaSb multi-layer stack. Finally, the defect density of this heterostructure will be correlated to the MOVPE conditions, disclosing an advantage of applying low growth temperatures to achieve a high heterolayer crystal quality.

2. Materials and Methods

The epitaxial growth was performed using MOVPE in a 300 mm industrial deposition chamber from Applied Materials. Trimethylgallium (TMGa), triethylgallium (TEGa) and trimethylindium (TMIn) were used as group-III source, triethylantimony (TESb) and tertiarybutyl arsine (TBAs) as group-V precursor. An oxide trench pattern, including die areas of different trench width and pitch, was fabricated on a (001) exactly oriented 300 mm Si substrate, based on a standard shallow trench isolation (STI) process [41]. The STI silicon oxide (SiO₂) layer is 300 nm thick; hence, the trench width variation from 80 nm to 500 nm leads to a change in the AR from 3.75 to 0.6. The open area ratio (Si/SiO₂) was kept constant at 9%, which corresponds to a pitch change from 880 nm to 5.5 μm, respectively. A V-shaped trench bottom exposing two {111} Si facets was achieved using a tetramethylammonium hydroxide (TMAH) wet-etch process. The application of such a multi-patterned 300 mm substrate allows the growth characteristics to be investigated for different trench width and pitch based on one epitaxy experiment. Before entering the MOVPE reactor for deposition, the wafer is loaded into a Siconi chamber from Applied Materials in order to selectively remove the native oxide from the

Si surface at the trench bottom at a temperature below 200 °C [42]; therefore, no high temperature substrate treatment is needed before epitaxial growth.

The growth of the III-V NR starts with a low temperature seed deposition followed by an overgrowth at high temperatures. This overgrowth step ensures the filling of the trench and the NR formation on top of the oxide pattern in order to achieve a broad (001) surface.

The growth of box-shaped GaAs NRs, which were investigated first for comparison with GaSb NRs, was reported before [43,44]. The GaAs seed layer is nucleated on the {111} Si facets at 360 °C, with a V/III gas phase ratio of 70, and the overgrowth is carried out at 580 °C with a V/III ratio of 15.

GaSb NRs were integrated on Si, based on three different approaches: applying an InAs or GaAs seed layer before the GaSb overgrowth and inserting a GaAs buffer on top of a GaAs seed before the GaSb overgrowth. In the case of a 100 nm wide trench, this GaAs buffer filled half of the trench. The growth conditions of the GaAs seed are identical to the ones used for the GaAs NR deposition. In the same way, the GaAs buffer was grown under conditions used for the high temperature overgrowth. The InAs seed was deposited at 365 °C with a V/III ratio of 70 similar to the conditions reported before [38]. The GaSb overgrowth conditions, which were kept constant for all three GaSb samples, were slightly modified to 560 °C and a V/III ratio of 2 in comparison to [38] (530 °C and V/III of 1), and also the growth time was increased in order to achieve a pronounced NR with a funnel profile exposing a large (001) surface. The NR layer stacks of all the samples explored in this study are sketched in Figure 1.

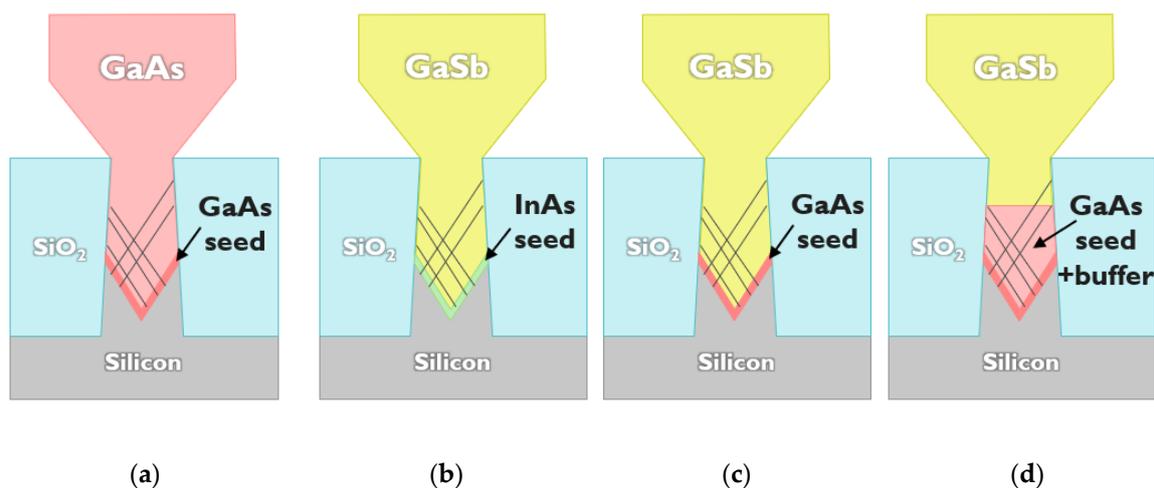


Figure 1. Layer sketch of the investigated GaAs and GaSb nano-ridges (NRs) showing the seed and buffer materials: (a) GaAs NR on GaAs seed, (b) GaSb NR on InAs seed, (c) GaSb NR on GaAs seed, (d) GaSb NR on GaAs seed and GaAs buffer.

For the integration of the InAs/GaSb heterostructures, we selected the GaSb NR with a GaAs seed but slightly decreased the overgrowth temperature to 550 °C to achieve a more pronounced box-shaped NR. After forming the NR with a height and width of around 350 nm and 450 nm, respectively, the deposition temperature was decreased to 450 °C and 500 °C for the growth of the heterolayer. The applied V/III gas phase ratios for the InAs and GaSb heterolayer were 5 and 1, respectively.

Increasing the NR surface area beyond a width of 400 nm using NRE of GaAs as well as of GaSb enables a systematic defect study applying ECCI. It is a scanning electron microscopy (SEM) based technique, which uses the strong dependency of the backscattered electron intensity on the local crystal properties (lattice plane orientation, presence of strain fields, etc.). The inspection method is non-destructive and visualizes individual defects on a smooth sample surface including a 3-dimensional structure like a NR [12,45,46]. Planar defects can be identified as a contrast line, whereas a threading dislocation, which is a 1-dimensional line defect, gives a dot-like contrast feature in the ECCI image. The measurements were performed in a Thermo Fisher Scientific Apreo lab SEM (Waltham, MA, USA)

system using a beam acceleration voltage of 5 kV and a beam current of 0.8 nA. Under these conditions, crystal defects are detected up to a layer depth of 35 nm.

The defect characterization was also supported using transmission electron microscopy (TEM). For the cross-sectional TEM analysis, specimens (TEM-lamellas) were prepared using focus ion beam (FIB). Prior to the FIB preparation, the samples were capped using a spin-on amorphous carbon (SOC) layer and thin ion-sputtered Pt layer as protection against the ion beam damage during FIB. The analysis of the samples was performed using a double corrected Titan3 G2 60–300 system from FEI (Thermo Fischer Scientific) at 120–200 kV voltages. For the defect analysis different magnifications and image conditions were applied such as high-resolution TEM, two-beam bright field (BF) TEM, high angle annular dark field scanning transmission electron microscopy (HAADF-STEM), annular bright field STEM (ABF-STEM) and dark field STEM (DF-STEM).

3. Results and Discussion

NRE, in a heteroepitaxial integration approach on Si, has some important advantages. It allows narrow trenches to be selected for efficient ART. Although this choice provides only a small III-V volume in the beginning, the amount of III-V material can be significantly increased using NRE on top of the trench pattern for the final device integration. In this way, the active device region of the NRs is clearly separated from the defective crystal region inside the trench, which is an important characteristic to achieve a long device lifetime. The first device demonstration of an optically pumped distributed feedback laser based on GaAs NRs waveguides emphasizes the application potential as well as compatibility of this integration concept with silicon photonics [30,47]. A SEM image of such an array of nano-ridge lasers is shown in Figure 2a. Each NR contains a 3× InGaAs/GaAs multi-quantum well stack capped by an InGaP layer. The optical light field is confined inside the NR on top of the pattern with a negligible overlap with the defective trench region. Next to a laser diode, a heterojunction bipolar transistor (HBT) was also demonstrated on 300 mm Si based on NRE [48].

Further growth optimization of the NRs requires fast access to the crystal quality to identify the threading dislocation density (TDD) and planar defect density (PDD), which is given using ECCL. Planar defects (PDs) such as stacking faults and micro twins run along {111} planes. Mobile threading dislocations (TDs) also glide along {111} planes. Therefore, the angle between the {111} planes and the (001) substrate surface determine a minimal AR of 1.43, which is necessary to block defects nucleated at the III-V/Si surface. However, most of the time a higher AR is required to achieve an efficient defect trapping, as remaining strain fields might initiate new misfit defects in an III-V region above the interface [49]. Therefore, it is very important to achieve full relaxation as close as possible to the III-V/Si interface to suppress the presence of residual strain fields and, hence, avoid new misfit formation. A large lattice mismatch between the III-V layer and Si together with optimized seed and overgrowth conditions can ensure full strain relaxation inside the trenches when only mobile and glissile TDs nucleate and TD pinning at the III-V growth surface is prevented. The origin of PDs is related to the MOVPE growth conditions in the first place but can also be caused by impurities at the Si surface or the mask oxide.

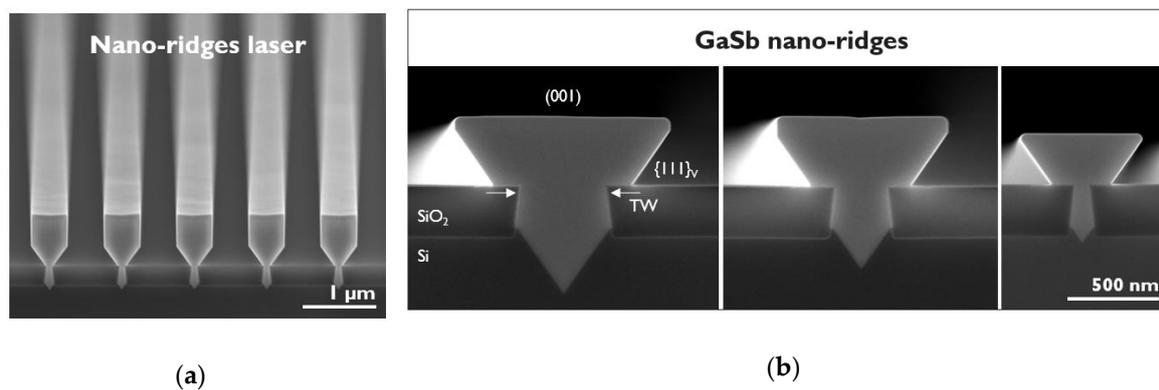


Figure 2. (a) Tilted cross-section scanning electron microscope (SEM) image of a nano-ridge laser array based on GaAs. (b) Cross-section SEM image of GaSb nano-ridges grown on top of a 500 nm, 300 nm and 80 nm wide trench. The white arrows indicate the location to define the trench width (TW). For the chosen growth conditions the NR profile is like a funnel and defined by large (001) and $\{111\}_V$ facets.

In order to better understand the correlation between AR and crystal quality, we explored NRs based on different trench widths. The total NR size varies with the mask pattern (trench width and pitch) on the die region due to loading effects. Figure 2b holds a comparison of representative GaSb NRs deposited on top of a 500 nm, 300 nm and 80 nm wide trench. All NR samples investigated in this study exceeded a NR height of 350 nm to evolve into a sufficiently wider (001) surface broader than 400 nm. It is important to note that ECCI (5kV) exposes crystal defects only in the top layer volume. Furthermore, a free-standing NR on top of the trench pattern leads to a higher aspect ratio as defined by the trench width since defects, lying in a $\{111\}$ plane, can stop at the $\{110\}$ III-V/air side surface. The defect counting based on ECCI represents only the density close to the top NR surface and not inside the complete NR volume, and consequently, a change in NR height affects the defect density obtained for the same trench width. Therefore, the following investigation reveals an overall tendency in the defect density as a function of the trench width, as the impact of different NR heights and, hence, modified ARs, is not taken into account.

3.1. Defect Density in GaAs Nano-Ridges

To start with we explore the crystal quality of our state-of-the-art GaAs NRs, using ECCI, which are already used in different device integration approaches. The TDD of the GaAs NRs decreases with a reduction in trench width as expected for ART. Figure 3a shows clearly this dependency, where each data point relates to a different die area or, in case of the same trench width, to a different growth experiment. For a trench width ≥ 300 nm ($AR \leq 1$), the TDD is above 1×10^8 cm $^{-2}$. Reducing the trench width to 100 nm results in a significant decrease in TDD to the range of 8×10^6 cm $^{-2}$ to 3×10^6 cm $^{-2}$. In the case of 80 nm wide trenches (AR 3.75), no signs of TD were found. In order to define an upper defect limit, we just assumed one defect for the total inspected area A_{insp} ($TDD < 1/A_{insp}$). This calculation leads to the open data symbols in Figure 3a for 80 nm wide trenches. These open data points indicate, in comparison with all solid data points, that the TDD density is only an upper limit based on the investigated surface area. For the maximal inspected area A_{insp} of 220 μm^2 , we claim that the TDD is below 4.5×10^5 cm $^{-2}$.

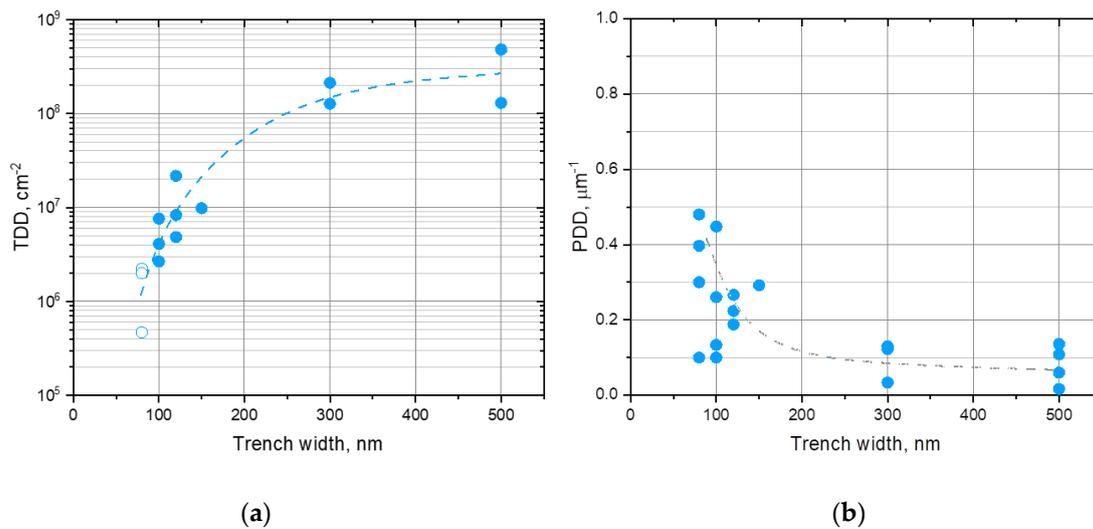


Figure 3. Threading dislocation density (a) and planar defect density (b) of GaAs nano-ridges as a function of underlying trench width based on electron channeling contrast imaging (ECCI). The open data points indicate that no threading dislocation was found, and the threading dislocation density (TDD) value, which was defined by the investigated surface area, is only an upper limit.

The PDD is defined as defects per NR trench lengths, as the majority of PDs infiltrate the full lateral NR width. Only in case of the wide trenches (≥ 300 nm) some PDs penetrate only parts of the NR width. Contrary to our observation for the TDD, the PDD increases with a reduction in trench width, as shown in Figure 3b. For a large trench width ≥ 300 nm the PDD stays below $0.2 \mu\text{m}^{-1}$ but rises sharply up to $0.5 \mu\text{m}^{-1}$ for narrow trenches ≤ 100 nm. For a trench width of 80 nm and 100 nm, several growth experiments under identical MOVPE conditions were carried out but using patterned wafers from different STI fabrication processes. A large spread in PDD in the range of $0.1\text{--}0.6 \mu\text{m}^{-1}$ was noticed, which points to a correlation with the patterned wafer quality.

PDs in III-V heterolayers on Si can be caused by a non-optimized seed nucleation. If this is the case, then the seed growth conditions seem to improve for the deposition in wider trenches with larger pitch, as the PDD decreases. However, impurities or SiO_2 residuals on the Si surface can also initiate PD formation. Therefore, another possible explanation for the observed tendency in PDD is that the cleaning treatment of the patterned wafers as well as the oxide removal process applied before epitaxial growth are more efficient in wider trenches in comparison to narrow trenches with a high AR. This hypothesis is also supported by the fact that we observed a large spread in data for narrow trenches formed on STI wafers coming from different fabrication processes and, therefore, probably having different surface cleanliness.

Dislocation defects such as TDs have the strongest impact on device performance. For our state-of-the-art GaAs NRs we can achieve a defect density below $4.5 \times 10^5 \text{ cm}^{-2}$ for trenches with an AR ≥ 3.75 . As this number is only an upper limit defined by the inspected area, the actual defect density could be even lower. A PD itself does not introduce open bonds or a strong local distortion as dislocation defects do; hence, a PD should be less destructive on device performance. However, inside a 2-dimensional layer on a blanket substrate, a PD is always accompanied by partial dislocations at the plane ends, which again affect the device operation. If a PD inside a NR penetrates the full NR width so that the ends of all the planar defect planes reach a NR surface, no partial dislocations are present inside the NR volume, except the ones present at the origin of the planar defect plane, most likely at the III-V/Si interface. In this case, the PD should have less of an impact on the device operation. A systematic study is needed comparing devices with different PDDs to either confirm or rebut our assumption and to estimate what PDD is acceptable to achieve sufficient device performance. However, the data collection in Figure 3b emphasizes that a PDD of less than $0.2 \mu\text{m}^{-1}$ should be

achievable also for narrow trenches by either optimizing the seed growth or the substrate treatments before deposition.

3.2. Defect Density in GaSb Nano-Ridges

III/Sb tends to nucleate easily as three-dimensional islands on a Si surface [20,50,51], even at low growth temperatures. A further reduction in growth temperature to improve the wetting behavior leads to a diminishing growth rate, whereas a higher material flux into the chamber can cause selectivity issues on the oxide pattern [38]. In this investigation we inserted an InAs or a GaAs seed before a high temperature GaSb overgrowth to simplify the III-V nucleation on Si. These seed layers cover the {111} planes at deposition temperature, but ramping up to the higher temperatures for the overgrowth leads to reflow exposing a slightly rounded V-shaped surface, as already discussed in [38]. In order to study the impact of the GaAs surface, we also explored a sample where we added a GaAs buffer on top of a GaAs seed revealing a flat (001) surface. The sample design in this investigation is very similar to what was explored in [38], but the NR volume and size on top of the oxide is much more pronounced. In addition, all the samples in this investigation are fully relaxed based on (224) reciprocal space mappings (RSMs), and the reciprocal lattice point of the GaSb NR is exactly at the position of strain-free GaSb without any shift, as observed before.

In the first place, we carried out a TEM investigation in both cut directions of all three samples for the NR grown on top of 100 nm wide trenches as the AR should be sufficient for good defect trapping. Due to the challenges in TEM-lamella preparation for GaSb material, the quality of the obtained images was slightly compromised by a range of contrast artefacts in the pictures which cannot be attributed to the sample structure. Among these artefacts are localized spots, probably caused by a local Ga re-deposition during FIB preparation, curtaining effects (CEs) and “scratches”. Nevertheless, for most of the obtained TEM images, the quality was good enough to draw conclusions concerning the crystal quality and to recognize the differences between the samples.

For the GaSb growth on top of the GaAs seed and GaAs buffer, we did not find any indication of TDs in the GaSb NR region on top of the oxide applying different TEM imaging conditions and investigating several micrometer TEM-lamellae. On the other hand, some PDs such as micro twins were identified. Figure 4a is a DF-STEM image acquired across the trench orientation for GaSb growth on top of a GaAs buffer revealing clearly the transition from GaAs to GaSb. Figure 4b,c are the corresponding (004) BF and (220) BF images for a TEM-lamella cut along the trench. The GaAs buffer inside the V-shape bottom contains a slightly higher density of misfit and threading dislocations in comparison to what has been observed for the growth of pure GaAs NR in previous TEM studies [43]. It looks as if the TDs that are initiated at the GaSb/GaAs (001) interface penetrate downwards into the GaAs buffer. A few dislocation defects, visible in the GaSb material inside the trench, are eventually trapped at the oxide sidewalls. A certain number of PDs is most likely generated at the III-V/Si interface, as reported for the GaAs NRs. However, for the GaSb growth on top of the GaAs buffer, micro twins and stacking faults are also introduced at imperfections at the GaSb/GaAs interface (not shown) as well as initiated by dislocation defects. A possible root cause could be the dissociation of a (unit) dislocation into partial dislocations, which introduces a planar defect if the partial dislocations move away from each other. Figure 4c is a magnification of the region framed with a red rectangle in Figure 4b, which clearly shows how PDs are introduced at individual TDs.

The main strain release at the GaSb/GaAs buffer interface is achieved by the formation of an interfacial misfit (IMF) array of 90° dislocations, although the observed periodicity was not perfect and isolated 60° dislocations were still present. In the case of the growth of GaSb directly on the GaAs seed layer, a well-defined regular array of 60° misfit dislocations was discovered in the GaSb layer along the {111} GaAs interface and some 90° misfit dislocations in the valley of the rounded V-shape. The average separation is ~ 5.2 nm and, hence, slightly larger than the calculated value of 4.5 nm of a fully relaxed GaSb layer on top of a {111} GaAs plane. Overall, the defective region is more confined inside the trench and closer to the III-V/Si interface when the GaAs buffer is absent. Figure 4d is a (220)

BF image acquired along the GaSb NR which visualizes the region of plastic relaxation along the GaSb/GaAs seed as well as the GaAs/Si {111} interface.

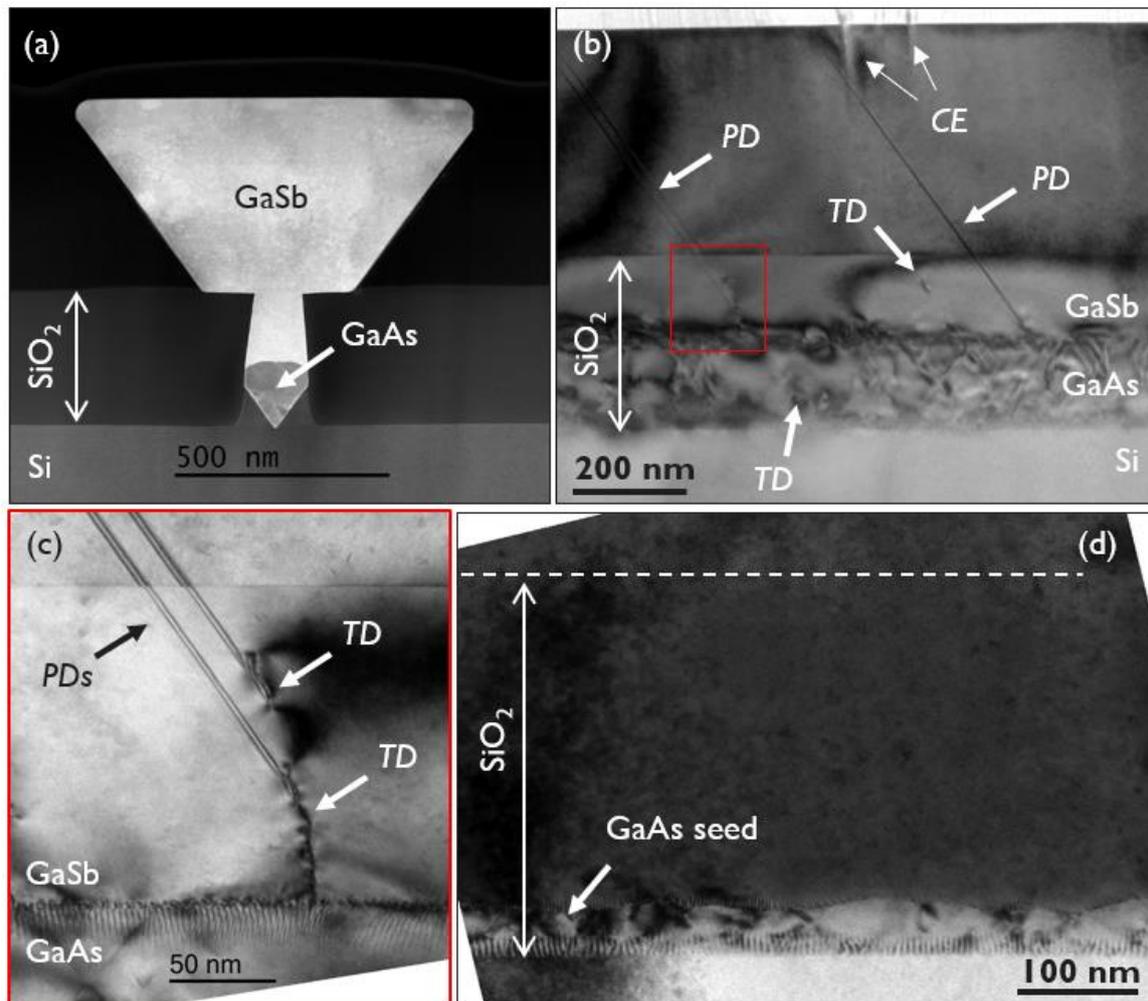


Figure 4. (a) to (c) are transmission electron microscopy (TEM) images from the GaSb NR sample deposited on a GaAs buffer, whereas (d) is a TEM picture from the GaSb NR grown on a GaAs seed layer only. (a) is a dark field scanning transmission electron microscopy (DF-STEM) image showing the complete NR across the trench orientation. (b) and (c) are two-beam (004) BF and (220) BF images obtained in a cut direction along the trench. (c) is a larger magnified picture of the region indicated by the red rectangle in (b). (d) is a two-beam (220) bright field (BF), also prepared in a cut directed along the trench orientation. Contrast artefacts caused by the curtaining effect (CE) are observed in (b).

The TEM analysis of a GaSb NR deposited on top of an InAs seed results in a different observation. No PDs were found in TEM images obtained in both cut directions, whereas some dislocation defects were clearly identified in the GaSb NR region above the oxide level. Figure 5 shows two standard TEM images taken from a cut direction along the trench orientation. Most defects are trapped deep inside the trench, leading to a strong reduction in defect density; nevertheless, some isolated misfit defects were still spotted in the upper GaSb material. Based on a TEM-lamella thickness of 50 nm, the inspected area above the trench oxide results in a defect density of $2 \times 10^9 \text{ cm}^{-2}$.

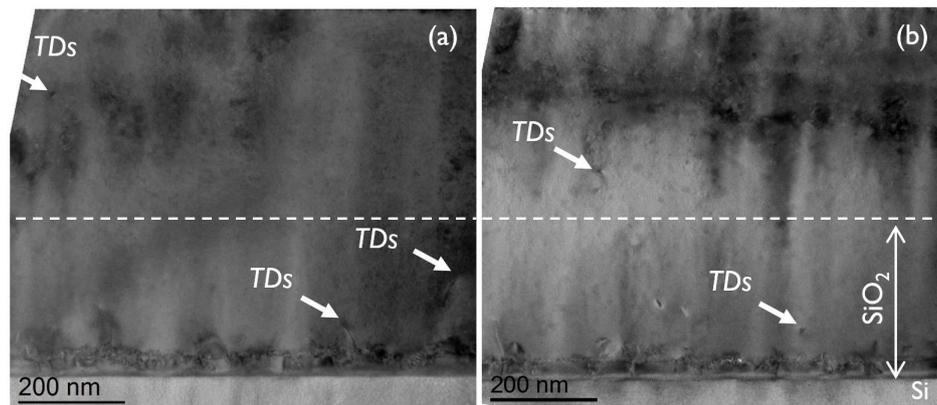
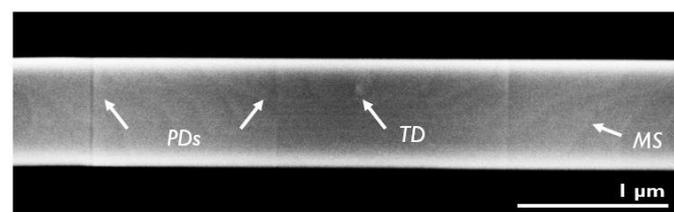


Figure 5. Two standard TEM images (a) and (b) acquired along the trench orientation of the GaSb NR sample with an InAs seed. The white dashed lines indicate the height of the trench oxide.

High magnification STEM images of the InAs/Si interface taken across the GaSb/InAs NR revealed the formation of a regular array of 60° misfit dislocations with a separation of approximately 3.1 nm, which corresponds to the expected spacing in a fully relaxed InAs layer on {111} a Si plane (3.0 nm). A few additional {111} lattice planes in the GaSb material, which originate at the InAs/GaSb interface, point to the presence of 60° misfit dislocations. It is impossible to judge if the corresponding misfit density is sufficient to release the complete mismatch strain between GaSb and InAs, as the small lattice mismatch demands only a misfit defect every 56.7 nm and the total GaSb/InAs interface length inside the trench is below 120 nm.

This first TEM analysis of a GaSb NR based on 100 nm wide trenches suggests that the TDD and PDD depend on the choice of seed material. In order to also provide better defect statistics for different trench widths, we extended our defect characterization to ECCI. The electron channeling contrast (ECC) image quality of a GaSb NR surface is comparable to what has been achieved for GaAs [12]. PD and TD can be clearly identified as straight lines and dot-like features, respectively, but bi- and mono-atomic surface steps (MSs) are also visible in the ECC images. Figure 6a is a typical ECC image of a GaSb NR surface revealing all the mentioned structures. Atomic force microscopy (AFM) was conducted to confirm the presence of MSs, as shown in Figure 6b.



(a)



(b)

Figure 6. (a) is a representative ECC image of a GaSb NR deposited on top of a 100 nm wide trench. (b) is an atomic force microscope (AFM) image of a comparable GaSb NR surface. The white arrow points to only one mono-atomic surface step (MS), but each contrast line is a MSs.

The TDD and PDD as a function of the trench width compiled using ECCI are summarized in Figure 7a,b. For all three GaSb NR samples, a decrease in TDD and an increase in PDD are observed with a reduction in trench width. Therefore, the fundamental dependency of the defect density on the trench width is the same as witnessed for GaAs. However, whereas the TDD decreases towards narrow trenches (100–80 nm) to values below $1 \times 10^6 \text{ cm}^{-2}$ for the GaSb NRs deposited on a GaAs seed or buffer, it stays in the range of $5\text{--}6 \times 10^7 \text{ cm}^{-2}$ for the application of an InAs seed. On the other hand, the PDD rises only very little to $0.12 \mu\text{m}^{-1}$ for the latter seed case but reaches a value close to $1.0 \mu\text{m}^{-1}$ for the deposition on GaAs. These PDD numbers are also higher than what was detected for GaAs NR, see Figure 2b. The ECCI inspection confirms what was already indicated by the TEM investigation, although the TDD of the InAs-seed sample (100 nm trenches) based on the TEM analysis is an order of magnitude higher, as defined using ECCI. This deviation could be explained by the poor statistics of a TEM investigation or by the fact that the full NR depth until the top of the oxide trench is considered, whereas ECCI only detects defects close to the top (001) NR surface.

To discuss possible explanations for our observation, we first consider the cause of TDs and PDs independently from each other. The main driving force to nucleate misfit dislocations is the lattice mismatch between the heterolayers. If the lattice mismatch is very large, dislocation defects start to nucleate soon after the deposition of a few monolayers, as the critical layer thickness is quickly exceeded. This is the case for the growth of an InAs as well as GaAs seed film on Si with a lattice mismatch of 11.6% and 4.1%, respectively. The growth of GaSb on top of a fully relaxed GaAs layer introduces another lattice mismatch of 7.8%, which is sufficient to achieve efficient strain release after the deposition of the relatively thin layer. Hence, plastic relaxation will still take place inside the trench, and threading dislocations can be trapped at the trench sidewalls. However, in the case of growing GaSb on top of a fully relaxed InAs seed layer, the lattice mismatch is only 0.6%, which implies a very large critical layer thickness for GaSb. Thus, misfit and threading dislocations are nucleated at a later stage of the GaSb growth, when the trench is almost filled, before enough strain energy has been built up to initiate plastic relaxation. Overall, it is very difficult to achieve a fully relaxed GaSb layer on top of an InAs film due to the small lattice mismatch. Using an InAs seed, the risk is very high that remaining strain fields in the GaSb volume will introduce dislocation defects, even in the NR material grown on top of the trench pattern. This threat might be confirmed by the presence of dislocation defects in the GaSb material outside of the trench pattern and could explain why ART is so inefficient, even for deposition in narrow trenches. Figure 8 holds a sketch of the different heterostructures, emphasizing the lattice mismatch between each layer.

For the GaSb deposition on GaAs, the decrease in TDD with trench width shows the same slope as discussed in Figure 2a for GaAs NRs. Comparing the TDD in Figure 7a for the GaSb growth on top of a GaAs seed and GaAs buffer indicates that the defect reduction in the latter case is slightly better for 150 nm and 120 nm wide trenches. As we observe a certain data spreading in the defect density for the same trench width but in a repeated growth experiment, further trials are necessary to confirm a difference between the application of a GaAs seed only or a GaAs buffer. In addition, there is still room to further optimize GaSb nucleation on the flat (001) GaAs surface, as the IMF array of 90° misfit dislocation in our sample is not perfect yet. It is also important to note that the GaAs buffer thickness was optimized to achieve a flat (001) surface in narrow trenches (≤ 150 nm), whereas wider trenches require a longer GaAs buffer growth time to completely fill the V-groove. Dedicated growth experiments with optimized deposition conditions for each trench width are necessary to further explore the difference between both GaSb NR samples based on GaAs.

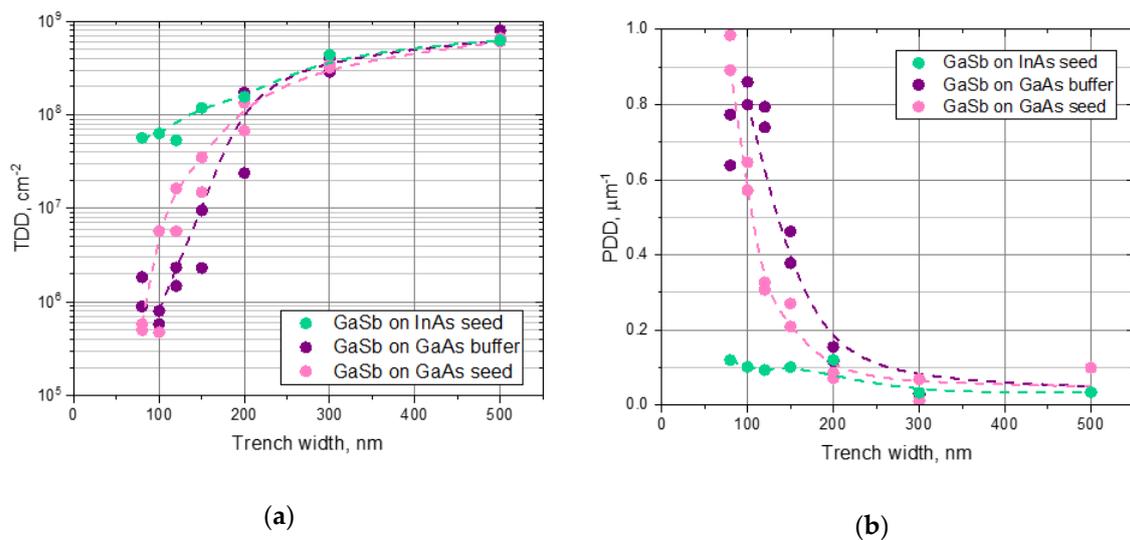


Figure 7. Threading dislocation density (a) and planar defect density (b) of GaSb nano-ridges as a function of underlying trench width based on ECCI. The different data groups indicated by a different color represent the three different integration approaches for GaSb.

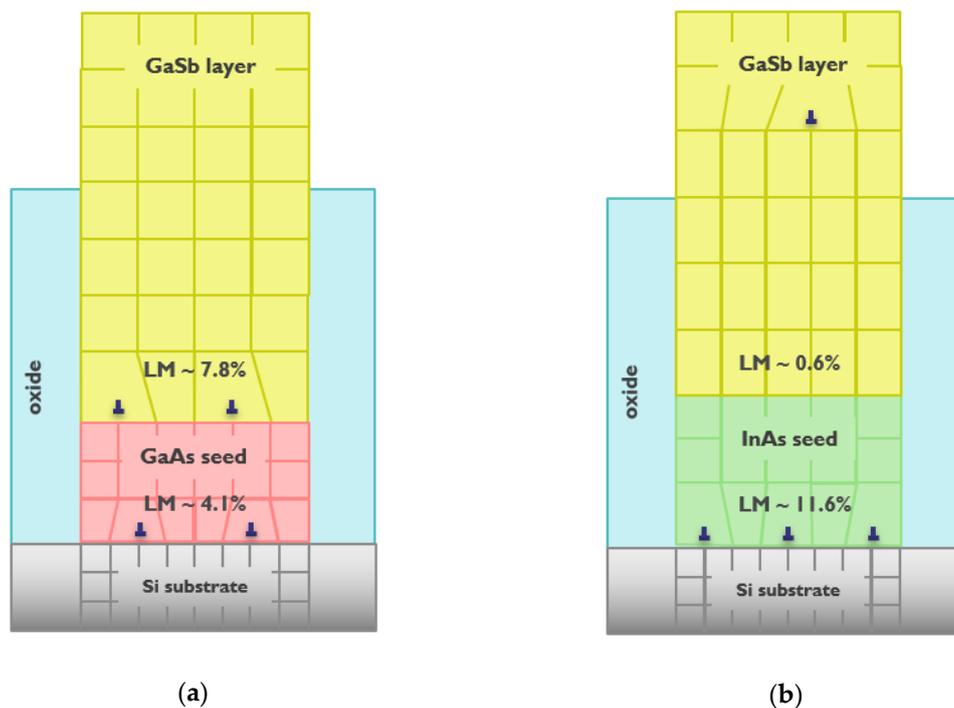


Figure 8. Layer sketch illustrating the various lattice mismatches (LM) towards the underlying layer for the GaSb integration on a GaAs (a) and InAs (b) seed.

The nucleation of planar defects can have very different sources. The correlation to the seed growth conditions and residuals on the Si surface has already been discussed in the previous section looking at GaAs NRs. The trend of the PDD in the GaSb NR deposited on GaAs seed and buffer is comparable, although the GaAs seed sample seems to be slightly better for 80–150 nm wide trenches. Additional growth experiments are necessary to verify this conclusion. However, overall, the PDD for narrow trenches ≤ 150 nm is significantly higher than what is observed for GaAs NRs. Additional root causes were already identified using the TEM investigation. Those are imperfections at the GaSb/GaAs interface and dislocation defects in the GaSb layer, as discussed in Figure 4c, which could explain

the higher PDD in GaSb NRs on GaAs seed and buffer. However, it is not clear why these additional PDs in GaSb on GaAs only show up in narrow trenches. In the case of the GaSb growth on top of an InAs seed, the PDD is very low and depends only slightly on the trench width. Either the InAs seed layer is less sensitive to impurity on the Si surface or the growth conditions are better than those chosen for the GaAs seed layer. Furthermore, it is known that Ga droplets, which are easily formed at low growth temperatures for non-ideal growth conditions, can dissolve Si and etch into the Si surface [52]. These melt-back defects could cause PDs in the GaAs layer, whereas applying an InAs seed circumvents this issue.

In a last attempt to explain our observations, we will assume a correlation between the TDD and PDD for narrow trenches. In the case of GaSb NRs on top of GaAs seed or buffer, we can achieve a low TDD density but suffer from a high PDD. For the InAs seed sample, this dependency is the opposite. If a PD ends inside a crystal or at an III-V/Si heterointerface, the participation of partial dislocations contributes to plastic relaxation. Therefore, a high density of PDs can also lead to a certain strain release at the III-V/Si interface and, hence, facilitate achieving full relaxation inside the trench, which reduces the risk of TD formation in the NR volume. On the other hand, the absence of PDs increases the risk of residual strain fields being present in the NR, which in turn initiate dislocation defects. This correlation between TDD and PDD is still a hypothesis, and more research is necessary to prove this link for GaSb. Nevertheless, in the case of pure GaAs NRs, a low TDD and PDD was achieved in some growth experiments, although the large distribution in PDD data for the same trench width in Figure 2b emphasizes the challenge of reproducibility.

3.3. Integration of an InAs/GaSb Heterostructure

The profile of the NR shape depends on the chosen MOVPE growth conditions together with the mask layout, as the open area ratio defines the material transport to the III-V surfaces and thereby the growth rate. NRE was explored for the deposition of GaSb NRs applying altered growth parameters to manipulate the growth rate hierarchy on the different facets. The NR shape is always defined by the facets with the lowest growth rate, whereas the NR planes with the higher growth rates disappear quickly during deposition. Figure 9 together with Figure 2b portray some examples of NRs with very different profiles. In general, the growth window to maintain a stable NR form is smaller for GaSb in comparison to GaAs and already small changes in temperature, growth rate or V/III gas phase ratio induce a different shape evolution. For the integration of the InAs/GaSb heterostructure we selected growth conditions which provide a box-shape NR, as depicted in Figure 9c.

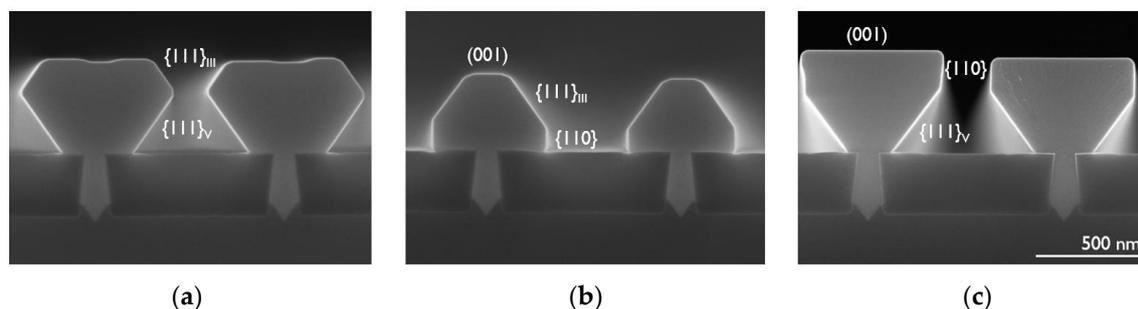


Figure 9. (a–c) Cross-section SEM images of GaSb NR grown under different MOVPE conditions. The facets with the fastest growth rate vanish quickly whereas the NR shape is defined by the planes with the lowest deposition rate.

In the first experiment the substrate temperature was reduced to 500 °C for the deposition of the multi-layer stack. At this temperature the GaSb tends to form a funnel NR profile as a result of a high growth rate on the {110} and {111}_{III} facets and a slow deposition rate on the {111}_V and (001) planes. A DF-STEM image of the complete heterostructure in cross section is shown in Figure 10a. A detailed

TEM analysis utilizing different imaging conditions and magnifications revealed that the InAs/GaSb multi-layer stack has very defined and abrupt interfaces and is free of defects in the center of the NR. An HAADF-STEM image of such a multi-layer stack taken from the central NR location is shown in Figure 10e, illustrating the high interface and crystal quality.

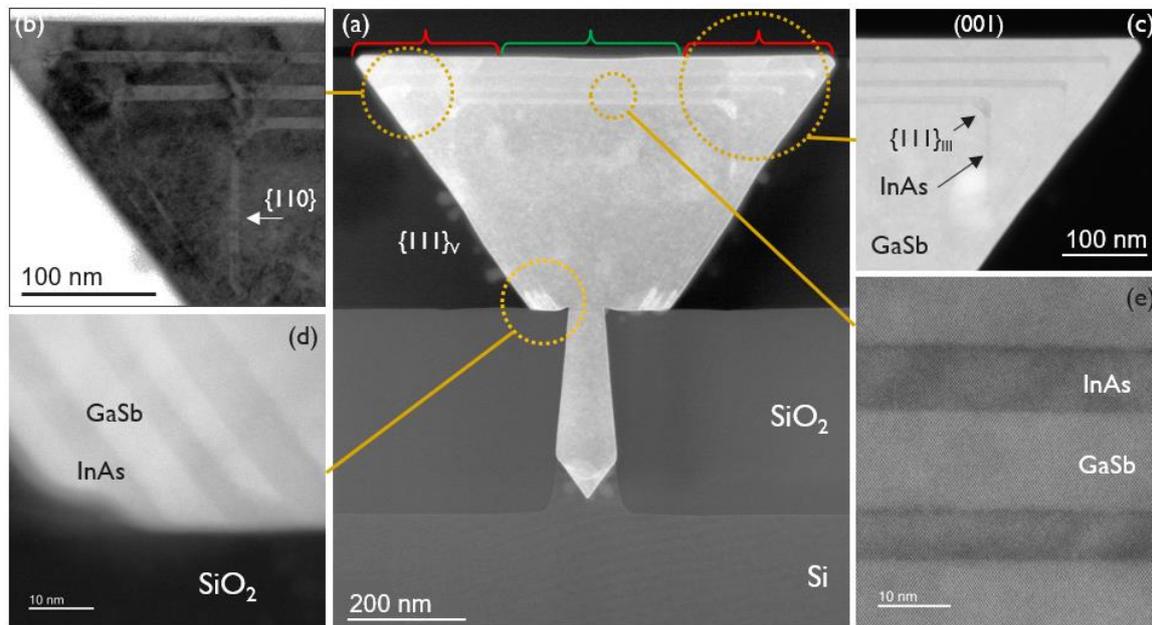


Figure 10. Summary of different TEM images prepared across the trench orientation of the multi-layer stack deposited at 500 °C. (a) is a DF-STEM image, (b) is a two-beam (004) BF and (c–e) are high angle annular dark field (HAADF)-STEM images with different magnification. The orange circles in (a) indicate the magnified image areas of (b) to (e) and the green and red brackets the defect-free and defective NR zones, respectively. The white spot in figure (c) is caused by a local Ga deposition during focus ion beam (FIB) preparation.

The growth time for the InAs and GaSb films at 500 °C was kept constant. However, during growth, the box-shaped NR transforms into a funnel-shaped NR and increases in size, which leads to a continuous change in the NR surface exposing less {110} facet area. Therefore, the thickness of each heterolayer varies as a function of the NR transformation. This interplay is recognizable in Figure 10c, which is a HAADF-STEM image of the edge of the NR region. It is also noticeable in Figure 10c, that the InAs layer thickness increases at the NR corners (based on each underlying GaSb NR surface before InAs deposition), where a short {111}III facet is exposed. This accumulation of InAs at the NR corners leads to the introduction of a high density of dislocation defects and occasionally PDs. Figure 10b is a (004) BF image revealing several dislocation defects, which are initiated at the corners, and threading dislocations penetrating towards the NR surface. In conclusion, although the central NR zone is defect-free, both edge regions are highly defective. The green and red brackets in Figure 10a classify these three zones. This division into centered defect-free and highly defective edge zones at the NR surface was also confirmed by an ECCI inspection scanning over a larger NR surface area.

Another unexpected feature, which was discovered in our TEM analysis, was a local change in the InAs growth rate on the {111}V facets, when the material comes into contact with the oxide mask surface. The increase in growth rate affects a facet length of about 50 nm until it switches back to a constant growth rate for the remaining {111}V surface area. Figure 10d is a magnified HAADF-STEM image of such a region. Despite the strong variation in layer thickness and the contact with the mask surface, no dislocation defects were found.

In a second integration attempt the growth temperature of the InAs/GaSb heterostructure was reduced further to 450 °C. At this low temperature the growth rate on the $\{111\}_{\text{III}}$ facet decreases and the $\{111\}_{\text{III}}$ plane expands more and more during deposition, which initiates the transition from a box to a diamond shaped NR. This transition in NR profile is clearly visible in Figure 11a, which holds a HAADF-STEM image. Another important difference to the growth experiment at 500 °C lies in the InAs layer thickness along the different NR facets. The InAs film is very uniform on the $\{110\}$ and $\{111\}_{\text{III}}$ facets but clearly thicker on top of the (001) plane. No indications of TD or PD were found in the edge region, as observed in the first heterostructure. Figure 11b,c are DF-STEM images of this area with different magnifications showing the defect-free deposition of InAs on the different NR planes. The profile of the InAs layer inside the NR becomes more obvious when performing energy dispersive X-ray spectroscopy (EDS). Figure 11d,e are EDS scans visualizing the presence of In and Sb in the NR. Applying this detection technique, a very fine EDS In-trace is recognizable along the $\{111\}_{\text{V}}$ plane in Figure 11d, which indicates the presence of a very thin InAs layer along this facet. Figure 11e is a magnified EDS image of the edge region highlighting the GaSb layers. A strong InAs growth rate on the top (001) plane is desired for the integration of active device stacks, but the related GaSb growth rate was unexpectedly low on the (001) facets. Therefore, some further MOVPE parameter adjustment is needed to optimize the growth rate hierarchy for GaSb on the different NR facets at 450 °C growth temperature.

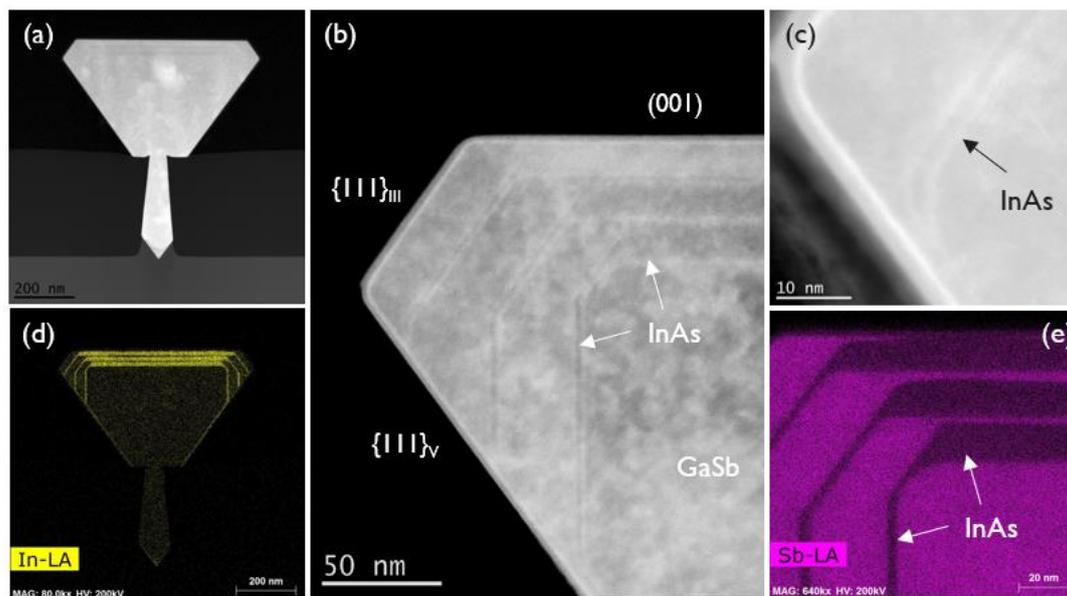


Figure 11. Collection of different TEM images prepared across the trench orientation of the multi-layer stack deposited at 450 °C. (a) is a HAADF-STEM image, (b) and (c) are DF-STEM images and (d) and (e) are energy dispersive X-ray spectroscopy (EDS) scans detecting $L\alpha$ energy transition visualizing the presence of In and Sb, respectively. The white spot in figure (a) is caused by a local Ga deposition during FIB preparation.

4. Conclusions

NRE was successfully applied to the growth of GaSb NRs on trench-patterned 300 mm Si wafers. An increased GaSb NR volume in line with a broad (001) top surface enables a systematic defect characterization using ECCI comparing the crystal quality of GaSb with GaAs NRs as a function of the trench width in the oxide pattern. The overall dependence of the TDD and PDD on the trench width is the same for GaSb and GaAs, but the absolute defect density depends strongly on the chosen seed material for GaSb. The deposition of GaSb on a GaAs seed or buffer leads to an efficient TD reduction below $1 \times 10^6 \text{ cm}^{-2}$ for the growth in narrow trenches, which is almost comparable to what is

observed for pure GaAs NRs and is significantly better than applying an InAs seed. Contrariwise, the application of an InAs seed for the deposition of GaSb NR results in a much lower PDD in narrow trenches. Application of ECCI next to TEM provides a clear advantage concerning defect statistics but bears the risk that not all defects are detected, especially for the case where a very low defect density is realized in a NR. The addition of other techniques, e.g., etch-pitch density or cathodoluminescence measurements, to visualize crystal defects would be important to support our observations. Nevertheless, this extensive defect investigation, exploring different seed and buffer layers for the monolithic integration of GaSb, contributes to a better understanding of the origin of defects, which in turn allows us to further optimize our monolithic integration approach. In the next step towards device integration, an InAs/GaSb multi-layer stack was deposited defect-free and with very abrupt interfaces on a box shaped GaSb NR after optimizing the growth mode on the different NR facets. The high crystal quality of this heterostructures emphasizes the large potential of GaSb NRE for monolithic integration of IR devices on 300 mm Si substrates.

Author Contributions: Conceptualization, B.K.; investigation, M.B., Y.M., Y.I., R.A., H.H., T.H., O.R.; methodology, H.H., T.H., O.R. and B.K.; resources, D.V.T., M.P., J.V.C. and R.L.; writing—original draft preparation, M.B. and B.K.; supervision, B.K.; project administration, R.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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