Micro-transfer-printed III-V-on-Silicon DBR lasers

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Abstract: III-V-on-silicon DBR lasers are realized by micro-transfer-printing pre-fabricated III-V semiconductor optical amplifiers on a silicon waveguide circuit and the effect of misalignment, inherent to the process, on the threshold current is investigated.

1. Introduction

High-volume and high-throughput integration of semiconductor optical amplifiers (SOAs) and lasers is indispensable for the development of advanced photonic systems on-chip. Many approaches are in development including pick-and-place of micro-packaged lasers, flip-chip integration, die-to-wafer or wafer-to-wafer bonding, hetero-epitaxial growth, each at a different technology readiness level. Micro-transfer printing is an emerging heterogeneous integration technique promising wafer-level integration, versatility in terms of the type of devices that can be integrated in close proximity and flexibility to integrate the devices in a complex silicon photonics (SiPh) platform without altering the generic process flow. The process starts with fabricating arrays of SOAs on an InP epitaxial wafer. This includes patterning the SOA mesa, etching of active layer region, p- and n- metallization using a lift-off process and defining individual coupons. Subsequently, the fabricated coupons are anchored to the InP substrate with dielectric tethers and then the sacrifical layer (InGaAs or InAlAs) underneath the epitaxial layer stack is under etched with $FeCl_3$:H_2O. The devices can now be picked from the source wafer using a poly-dimethylsiloxane (PDMS) stamp and printed onto a silicon photonic target wafer. Figure 1(a) shows a printed SOA coupon on a Si waveguide. A thin layer of DVS-BCB is spin coated on the target wafer to improve the yield of the printing process. Encapsulation and tethers are dry etched and the thin BCB layer is fully cured. The final step involves opening of the p- and n-metal vias and thick metal deposition. Figure 1(b) shows a top view of the DBR lasers after contact metal deposition. This process has been described in detail in [1]. One of the main challenge in micro-transfer printing of patterned SOAs is the misalignment between the Si and the III-V waveguides printed on top. State-of-the-art transfer printing tools provide an alignment accuracy of ± 1.5 μm (3σ). The micron-scale accuracy of the transfer printing tool requires good alignment tolerance of the adiabatic taper structure used to couple light from III-V to Si waveguide and vice versa [1]. In order to solve this problem, we designed an alignment tolerant adiabatic taper which can provide high-coupling efficiency for up to 1.0 μm misalignment [1]. In this paper, we use the same SOAs as in [1] and transfer print them between two identical DBRs patterned in the Si waveguide layer to form a laser cavity. The variability in the threshold current due to misalignment inherent to the micro-transfer printing process is investigated by realizing several copies of the same design and measuring the misalignment of each coupon using image processing of the microscopic images.

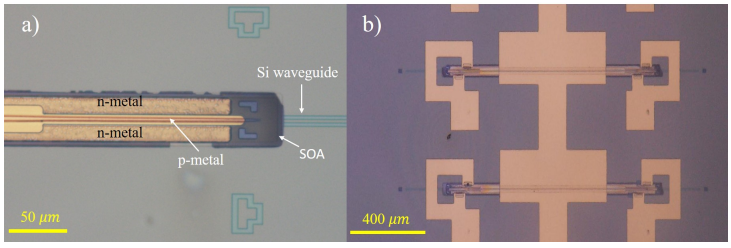

Fig. 1. a) Top-image of a micro-transfer printed SOA on a Si waveguide, b) Top-image of DBR lasers after contact metal desposition.

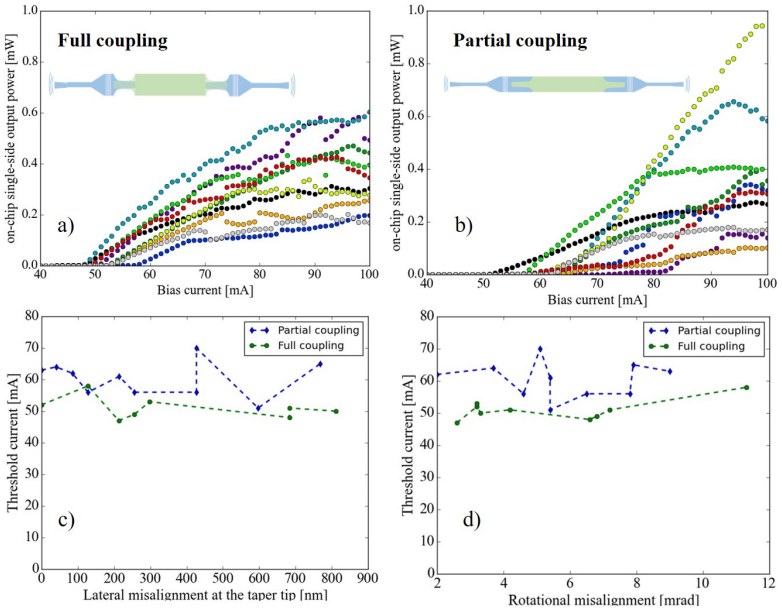

Fig. 2. on-chip output power against bias current of a) full coupling design and b) partial coupling design. c) Measured threshold current plotted against the measured (c) lateral misalignment and the (d) rotational misalignment between III-V and Si waveguide after transfer printing.

2. Design design and characterization

The III-V epitaxial layer structure used to fabricate the SOAs is described in detail [1]. It comprises 6 AlInGaAs QWs sandwiched between AlInGaAs barriers (C-band gain spectrum) as an active region. The silicon device layer is 400 nm thick and it is etched 180 nm to define the waveguides. The DBR gratings are etched 180 nm in the Si waveguide with a period of 258 nm and 50 percent duty cycle. They are designed to have a reflectivity of 60 %. The buried oxide layer (BOX) is 2 μm thick underneath the silicon device layer. We use grating couplers to couple light out of the chip. The III-V SOA is 1.1 mm long including a 700 μm gain section and two 225 μm III-V alignment-tolerant adiabactic tapers on both sides of the SOA. Two types of structures are evaluated: one with full coupling of light between the III-V and silicon waveguide and one hybrid design where the optical mode in the laser structure is only partially confined in the III-V. The III-V waveguide width in the gain section is 3.2 μm. The partial coupling design has 3.0 μm under the SOA whereas the full coupling design has no Si waveguide underneath, as shown in the inset of Fig. 2(a-b). The III-V-on-silicon PIC is placed on a temperature-controlled stage for the measurements and kept at 20 ^{o}C. The PIC is optically probed with cleaved standard single mode fibers using a fiber stage. Grating couplers are used to interface with the optical fibers. To calibrate out the grating coupler response, reference passive silicon waveguides are also fabricated on the III-V-on-silicon PIC and they undergo the same processing steps as the grating couplers used for interfacing with the DBR laser. The DBR laser is electrically probed with needles and is biased through a Keithley 2400 source meter. The DBR lasers have a similar resistance of 9 Ω. Figure 2(a-b) shows that the single-sided on-chip output power varying between 0.1 mW to 1 mW and 0.18 mW to 0.6 mW for partial coupling and full coupling design, respectively. Mean threshold current I_{th} is 60 mA and standard deviation is 5 mA for partial coupling design. On the other hand, for the full coupling design the mean I_{th} is 51 mA and standard deviation is 3 mA. In order to investigate the effect of misalignment on the threshold current, microscopic images are taken using the Olympus DSX-500 microscope at the 5547x magnification with each pixel representing 43 nm. The images are then processed using the OpenCv Python library to calculate the rotational misalignment and the lateral misalignment, at the III-V taper tip, between III-V and silicon waveguides. Figure 2(c-d) shows no correlation between the misalignment and the threshold current. This indicates that alignment tolerant adiabatic taper performs well within the alignment tolerance of the micro-transfer printing tool and the variation in the threshold current is due to the III-V processing carried out in our cleanroom.

References

1. B. Haq and et al., “Micro-transfer-printed III-V-on-silicon C-band semiconductor optical amplifiers,” Laser & Photonics Rev. .