

# High-Efficiency Si<sub>3</sub>N<sub>4</sub> Grating Coupler with Bottom Bragg Reflector for Micro-Transfer Printed InP Photodiodes

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**Abstract:** We present FDTD simulation results and a corner analysis for the design of Si<sub>3</sub>N<sub>4</sub> grating couplers with embedded amorphous-Si/SiO<sub>2</sub> DBR bottom mirror providing up to 99.58% coupling efficiency at 1560nm to micro-transfer printed InP photodiodes. © 2023 The Author(s)

## 1. Introduction

Silicon based photonic integrated circuits (PICs) offer the potential to implement high-complexity optical functionality on a small footprint at low cost and high yield by relying on the well-established mature CMOS processes. Several Si photonics platform options are currently available, including silicon-on-insulator (SOI) and silicon nitride (Si<sub>3</sub>N<sub>4</sub>) [1]. The advantages of Si<sub>3</sub>N<sub>4</sub> over SOI circuits include an extended wavelength range, lower loss and higher power handling [2], while SOI provides a higher index contrast and therefore results in an increased miniaturization. The low-loss nature of the Si<sub>3</sub>N<sub>4</sub> platform makes it a good candidate for quantum applications, where near-lossless operation is key. However, several crucial building blocks are natively missing from the Si<sub>3</sub>N<sub>4</sub> platform. Micro-transfer printing has been proposed as a heterogeneous integration technique that enables the integration of a wide range of materials/devices on wafer scale in a massively parallel way while making efficient use of the non-native source material [3,4]. In this paper, we discuss the design of a grating coupler providing up to 99.58% coupling efficiency from the Si<sub>3</sub>N<sub>4</sub> device layer to the micro-transfer printed (uTP) InP photodiode (PD) at 1560nm, paving the road to achieve photodetection with over 99% quantum efficiency.

## 2. Simulation results and corner analysis

The final layer stack of the devised coupling structure is described in Fig. 1. During the design process, we constructed the layer stack based on 2D FDTD simulations. The first step consisted of designing the grating while assuming a metal mirror below the bottom oxide. This resulted in a grating with 99.78% top transmission. Next, the mirror was replaced by a distributed Bragg reflector (DBR) [5-7]. Four periods of alternating amorphous Si (a-Si) and SiO<sub>2</sub> lead to a DBR with 99.79% power reflection for orthogonal incidence. This results in a coupler with 99.66% top transmission. Next, we add a semi-infinite InP layer on top of the top oxide (TOX) and sweep the TOX thickness. This semi-infinite InP layer serves as an approximate model for the printed PD. Unfortunately, even for the optimal TOX thickness the top transmission has dropped down to 99.46%. This is due to the additional reflections at the SiO<sub>2</sub>-InP interface, which can be reduced by adopting a  $\lambda/4$  anti-reflection coating (ARC). Ideally, the refractive index of this ARC should be 2.138 resulting in a re-optimized top transmission of 99.71%. However, we used a Si<sub>3</sub>N<sub>4</sub> ARC resulting in a 99.67% coupling to the InP.

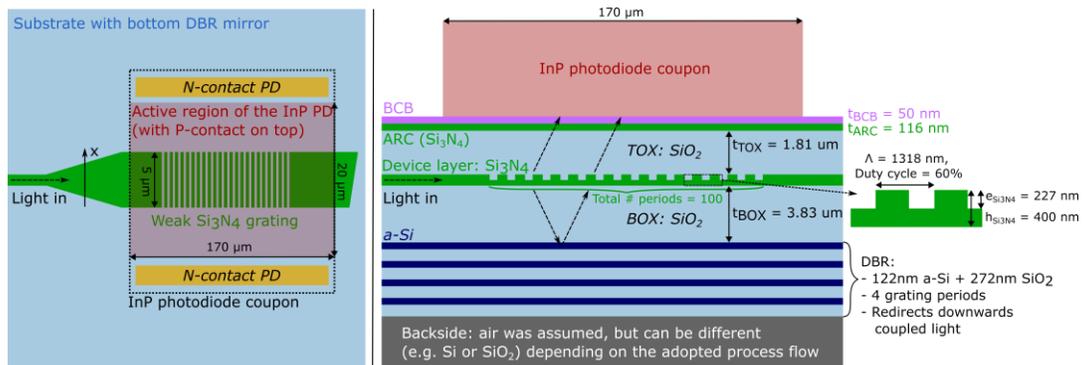


Fig. 1. Envisioned geometry of the Si<sub>3</sub>N<sub>4</sub> coupler with DBR bottom mirror and Si<sub>3</sub>N<sub>4</sub> ARC to accommodate for >99% coupling: (left) top view (right) cross-sectional side view.

The final layer that was added to the stack is benzocyclobutene (BCB), which serves as an adhesive bonding agent to enhance the adhesion during the micro-transfer printing. A typical BCB thickness used for these applications is around 50nm. After adding the BCB to the layer model, we finalize the design by re-optimizing the ARC thickness, resulting in 99.65% coupling. During corner analysis, we've decide to increase the PD length (from 100um to 170um) and the number of gratings (from 50 to 100) to improve the fabrication tolerance of the grating coupler, resulting in a top transmission of 99.72%, a back-reflection of 0.06%, and a bottom transmission of 0.1%. Corner analysis of the 2D geometry with achievable fabrication tolerance levels show that this coupling structure can reach >99% coupling to the InP for all process corners, when the bottom oxide is realized as a thermal oxide.

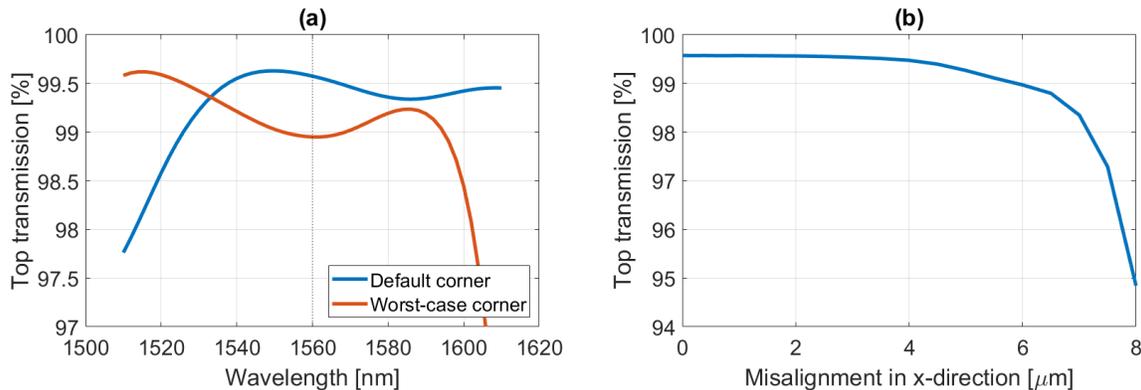


Fig. 2. Coupler performance - 3D FDTD simulation results: (a) Top transmission for both the default and worst-case fabrication corner. (b) Tolerance to printing misalignment in the x-direction shown in Fig. 1

The wavelength dependence of the coupling from the  $\text{Si}_3\text{N}_4$  waveguide to the InP photodiode for both the default and worst-case corner are shown in Fig. 2(a). For these simulations 3D FDTD was used, assuming an active region width of 20um for the PD while the width of the coupler was set to 5um. Resulting top transmissions for the default and worst-case corner are respectively 99.58 and 98.95% at 1560nm. Finally, the robustness to printing misalignment in the x-direction was evaluated through 3D FDTD, as shown in Fig. 2(b). A misalignment of 2 - 4 um results in a degradation of coupling efficiency by only 0.01% - 0.1%. With commercial printing tools,  $3\sigma$  printing accuracies of +/- 500nm can be expected, showing that the devised coupling structure is compatible with the micro-transfer printing tools that are used nowadays.

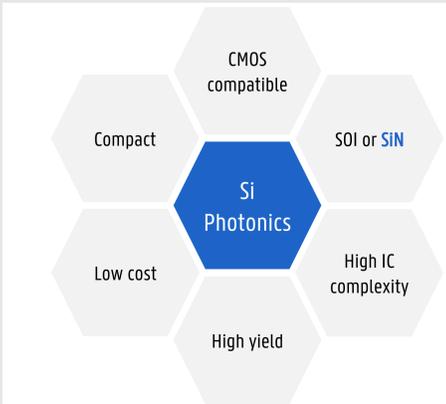
### 3. Conclusion

We have designed an ultra-high efficiency grating coupler based on an unapodized  $\text{Si}_3\text{N}_4$  shallow-etched grating in combination with a bottom DBR mirror and a  $\text{Si}_3\text{N}_4$  anti-reflection coating. The structure is compatible with micro-transfer printing, due to a high tolerance to printing misalignment and the presence of a BCB layer. Furthermore, it was verified through 3D FDTD simulations that it can provide up to 99.58% coupling efficiency from the  $\text{Si}_3\text{N}_4$  device layer to the InP active layer at an operation wavelength of 1560nm. Corner simulations were performed to investigate the fabrication tolerances and it was found that we can expect that even for the worst-case corner, this structure can still offer 98.95% coupling efficiency. By adopting the proposed coupling structure, photodetection with quantum efficiency over 99% seems feasible, presenting a key building block in integrated quantum circuits. Furthermore, due to the high-throughput potential of uTP, a large number of these high-quantum efficiency PDs can be densely integrated on a wafer. More work is, however, required to establish such a platform and assess the performance and actual process variations since both the accurate control of the bottom oxide thickness and the growth of the DBR mirror are not trivial.

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# HIGH-EFFICIENCY $\text{Si}_3\text{N}_4$ GRATING COUPLER WITH BOTTOM BRAGG REFLECTOR FOR MICRO-TRANSFER PRINTED INP PHOTODIODES



## High quantum efficiency (QE) photodetection for quantum applications

	SOI	$\text{Si}_3\text{N}_4$
Index contrast (higher for SOI)	Very compact More efficient grating couplers Higher losses ( $\sim 1$ dB/cm)	Compact Better fabrication tolerance Lower loss ( $< 0.1$ dB/cm, <b>Quantum!</b> )
Linearity	Worse (2-photon absorption)	Better (no 2-PA)
Thermo-optic coefficient	Higher	Lower
Transparency range	Down to 1100 nm	Down to 400 nm
Active components	Modulators/PDs available but worse than III-V, no lasers $\rightarrow$ <b>micro-TP</b>	(nearly) Absent $\rightarrow$ <b>micro-TP</b>

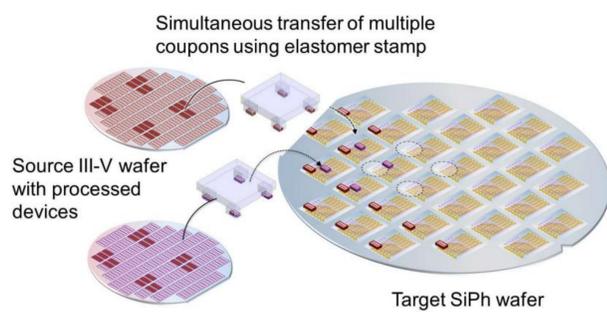
GOAL: Efficient and robust grating coupling scheme from 400 nm SiN waveguide to InP photodiode?

- Wavelength = 1560 nm
- Target quantum efficiency  $\geq 99\%$  (room temp.)
- PD area is capacitance limited

Micro-transfer printing compatibility is required

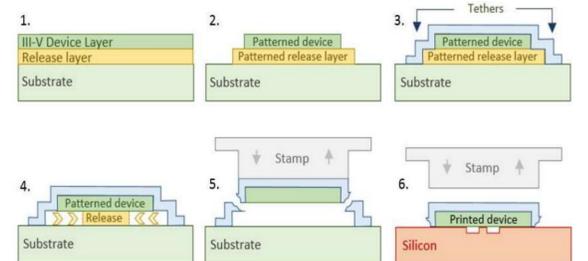
- Thin adhesive layer (BCB)
- Sufficient printing misalignment tolerance ( $\geq 1\mu\text{m}$ )

## Micro-transfer printing to integrate high QE photodetectors on the low-loss SiN



Heterogeneous integration of non-native building blocks  
III/V amplifiers & photodetectors,  $\text{LiNbO}_3$  & PZT modulators, electronic chiplets, optical isolators, single-photon sources ...

- Wafer scale processing
- Massively parallel, high throughput
- High integration density
- Efficient use of non-native source material
- Minimal changes to target platform (back-end integration)
- Minimal post-processing after printing (metallization, ...)
- Known good die

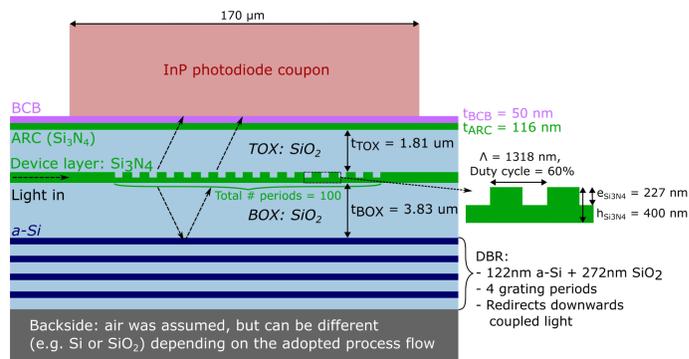


J. Zhang et al., "III-V-on-Si photonic integrated circuits realized using micro-transfer-printing," APL Photonics 4 (11), 110803 (2019).  
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Presentations at FIO on transfer printing in our group:  
FW5E.5 – We 11 Oct, 16.15-16.30 – M. Niels:  $\text{LiNbO}_3$   
FTh3E.6 – Th 12 Oct, 12.00-12.15 – L. Reis: GaP

## 2D layer stack design and sensitivity

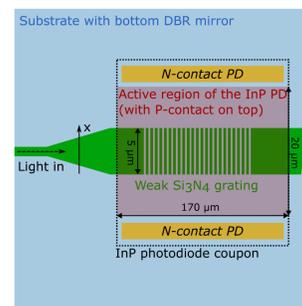
- Weak 400nm SiN grating coupler with partial etch (unapodized)
- Backside DBR mirror to avoid bottom leakage
  - 4 periods [amorphous-Si ( $n=3.545$ ) /  $\text{SiO}_2$  ( $n=1.444$ )]
- High-QE InP photodetector through transfer printing
  - BCB as an adhesive layer: better yield and performance
  - Anti-reflection coating between  $\text{SiO}_2$  and InP



- Lumerical 2D FDTD simulations (ideal & corner analysis):
- SiN waveguide  $\rightarrow$  InP: 99.72% ( $\geq 99\%$  for all corners)
  - Bottom leakage: 0.1%
  - Back-reflection: 0.06%

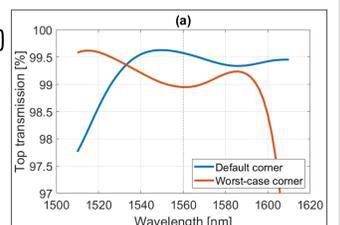
Beyond 99% coupling requires thermal bottom oxide (better process control than CVD)

## 3D performance and printing tolerance ( $3\sigma = 0.5-1.0 \mu\text{m}$ )

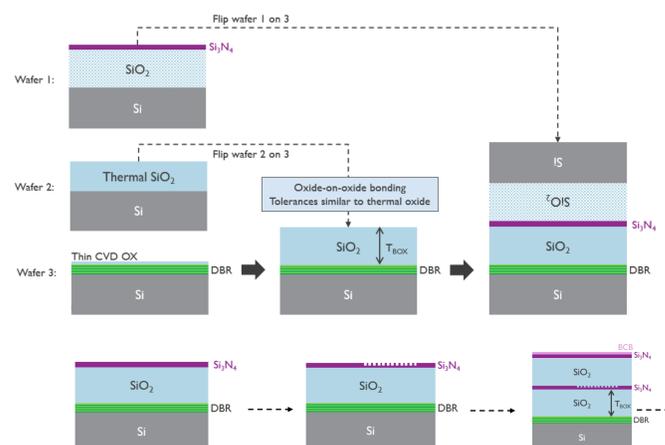


Lumerical 3D FDTD simulation & convergence test  
InP absorption area:  $170 \mu\text{m} \times 20 \mu\text{m}$

- SiN  $\rightarrow$  InP: 99.58% ( $\geq 98.95\%$  for all corners)
- Bottom leakage: 0.19%
- Back-reflection: 0.022%
- 2/4  $\mu\text{m}$  misalignment = 0.01/0.1% degradation



## Potential process flow



## Alternative

