

Towards a low-power nanophotonic semiconductor amplifier heterogeneously integrated with SOI waveguides

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Abstract— In this paper we propose an optically pumped nanophotonic III-V semiconductor optical amplifier heterogeneously integrated on a silicon-on-insulator waveguide circuit through wafer bonding technology. 10 μ m long adiabatic tapers allow a full power transfer from the silicon waveguide layer to the III-V membrane. Low-power consumption is expected, given the high optical confinement in the 100nm thick III-V membrane waveguide, making it suitable for intra-chip optical interconnect networks. We report on the design and preliminary characterization of this novel type of high-index contrast nanophotonic device.

I. INTRODUCTION

High index contrast waveguide structures show great promise to reduce the size of photonic integrated circuits. Silicon-on-insulator is considered as a very important platform on which to realize these photonic integrated circuits, since it allows using CMOS tools for fabrication, and permits integration of electronics along with the optical functions. One approach to enabling efficient light emission and amplification on this platform involves the integration of III-V semiconductors on top of the SOI waveguide. In literature, thick III-V layer stacks ($>0.5\mu\text{m}$) were transferred to a silicon waveguide circuit using adhesive and molecular bonding to realize III-V thin film lasers and optical amplifiers integrated on and coupled to the SOI waveguide circuit [1]. The use of thick III-V layer stacks in order to allow efficient electrical pumping, limits the

optical confinement in the gain region however and therefore doesn't exploit the full potential of the high index contrast III-V membrane structure. In this paper we propose to use 100nm thick III-V membranes that are optically pumped from the SOI waveguide layer, to realize a nanophotonic optical amplifier heterogeneously integrated on top of the silicon waveguide circuit. This thin III-V layer stack allows optimal confinement of the optical mode in the III-V quantum wells. Moreover, the reduced height of the III-V layer stack can facilitate integration with the standard CMOS metallization approaches (with typically 500nm inter-metal dielectric thickness).

II. DEVICE CONFIGURATION

The device structure is schematically outlined in figure 1, showing the adiabatic inverted taper couplers for high efficiency and large optical bandwidth coupling between the silicon waveguide circuit and the III-V membrane layer (which is bonded onto the silicon waveguide circuit using an adhesive BCB die-to-wafer bonding approach [2]). Both the optical pump and the signal are coupled

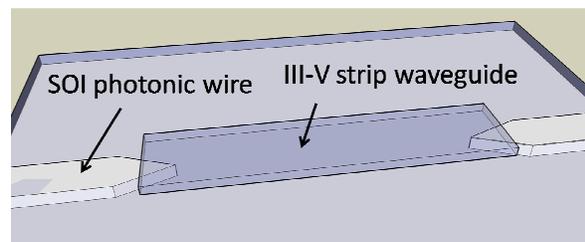


Fig. 1. Heterogeneous III-V/SOI nanophotonic semiconductor amplifier device layout

to the III-V membrane through the silicon waveguide layer. The III-V strip waveguide is 2 μm wide and is formed in an 80nm thick III-V epitaxial layer stack, consisting of four 8nm InGaAsP quantum wells (1% compressively strained – 1.55 μm emission wavelength) separated by five 10nm thick InGaAsP barriers (bandgap wavelength 1.17 μm) and cladded by two 10nm thick InP cladding layers. The SOI adiabatic tapers are formed in a 220nm thick silicon waveguide layer by tapering the width of the silicon waveguide from 700nm down to 100nm over a length of 10 μm . Assuming a DVS-BCB bonding layer thickness of 100nm this results in an adiabatic power transfer from the silicon waveguide mode to the fundamental optical mode supported by the III-V strip waveguide.

III. DEVICE FABRICATION

Silicon-on-insulator waveguide circuits were fabricated using 193nm deep UV lithography and dry etching on an 8inch SOI wafer in a CMOS pilot-line [3]. After die singulation, the SOI dies were cleaned in a Standard Clean-1 solution, after which the DVS-BCB polymer layer was spin coated (diluted using mesitylene in order to achieve an ultra-thin bonding layer). After evaporation of the solvents, the III-V die (which is prepared by removing a sacrificial InP/InGaAs layer pair) was attached to the SOI waveguide circuit and the stack is cured at 250C for 1 hour. After curing, the substrate of the III-V die is removed using a combination of mechanical grinding and wet chemical etching (using 3HCl:H₂O) until an InGaAs etch stop layer is reached, which is in turn also removed using H₂SO₄:3H₂O₂:H₂O. This leaves the 100nm thick III-V layer attached to the SOI waveguide circuit. This layer is then patterned into III-V strip waveguides using a 400nm thick SiO₂ hard mask and standard contact lithography and III-V dry etching (CH₄:H₂ plasma). A microscope image of the fabricated devices and a cross-section of such a device are depicted in figure 2.

IV. DEVICE CHARACTERIZATION

First measurements using a continuous wave (CW) pump-probe configuration show substantial

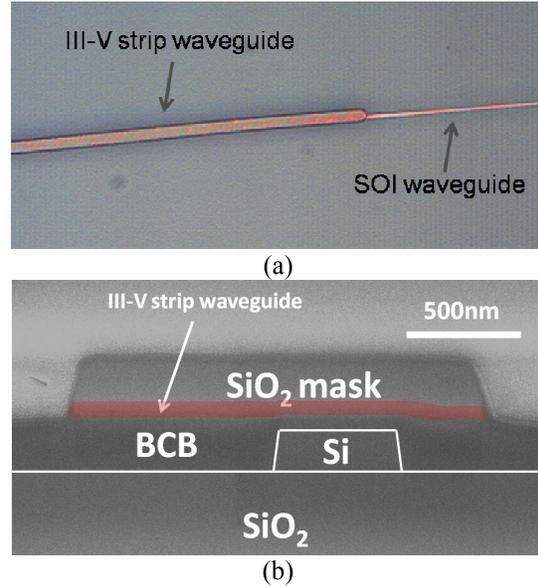


Fig. 2. Microscope image of a fabricated III-V strip waveguide amplifier (a) and a cross-section of the fabricated device in the adiabatic taper region

saturation/reduction of probe absorption with injected pump powers in the range of 1-2mW, as shown in figure 3. This figure shows the insertion loss of a 100 μm long III-V strip waveguide. As a pump, a 1.45 μm pump laser is used, which is injected along with the optical signal in the 1.55 μm wavelength range. The optical spectrum at the output of the III-V/SOI waveguide structure, both with and without optical pump is shown in figure 4, showing enhanced signal transmission and the spontaneous emission from the III-V layer. While a large saturation of the absorption is observed, no net gain from silicon input

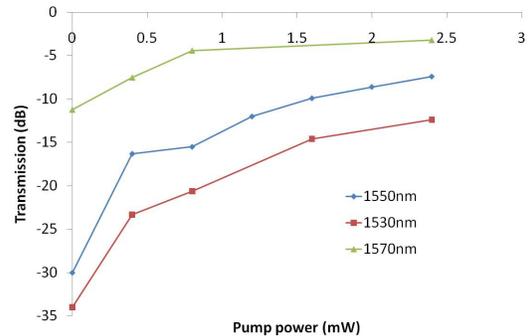


Fig. 3. Transmission of the 100 μm long III-V/SOI waveguide structure as a function of the signal wavelength. 1.45 μm pump light is injected along with the low-power 1.55 μm band signal.

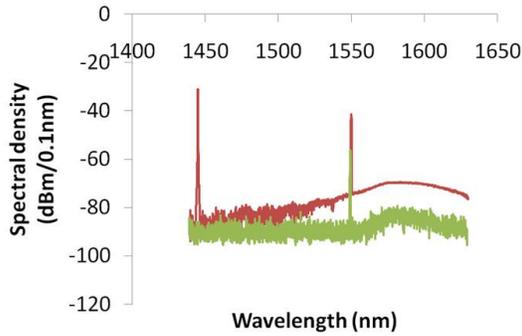


Fig. 4. Output spectrum of the III-V stripe waveguide. The lower graph is without pump signal, the upper graph is with an 800µW pump signal at 1.45µm.

waveguide to silicon output waveguide is obtained at this point. As can be seen in figure 3 and 4, the bandgap wavelength has shifted to longer wavelengths compared to the original layer stack (1.55µm as confirmed by photoluminescence measurements). This may point either toward a modification of the III-V epitaxial layer stack due to the layer transfer (given the fact that this is an ultra-thin epitaxial layer which is sensitive to residual stress in the bonded stack) or it may suggest an increased temperature of the III-V strip membrane due to the optical pumping of the device. In order to assess the device layer quality,

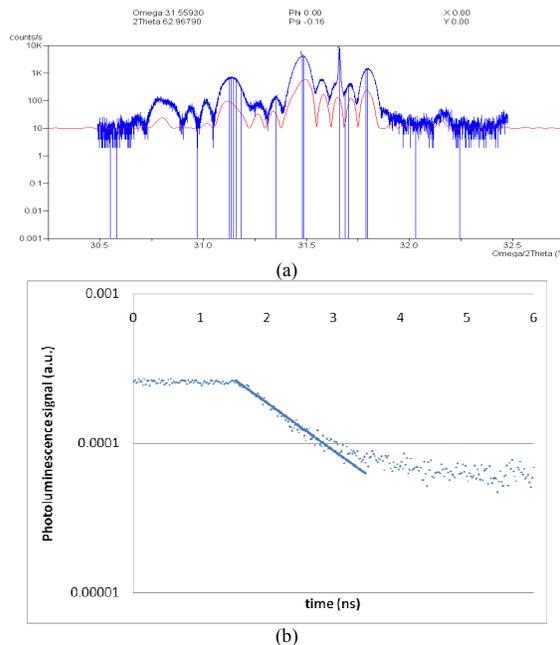


Fig. 5. X-ray diffraction analysis of the bonded bonded III-V epitaxial layer and comparison to the model (top graph is measurement, bottom graph is model) (a) and (b) carrier lifetime analysis in the III-V layer stack in a modulated pump probe configuration, showing a carrier lifetime in the nanosecond range.

XRD measurements of the layer stack and a carrier lifetime measurement was performed. The results of these measurements are outlined in figure 5. These measurements show the good epitaxial layer quality since the measured XRD spectrum corresponds to the model simulation, in which we assumed the same strain in the bonded epitaxial layer stack as when it was still on the InP growth substrate. Also the photoluminescence lifetime is in the nanosecond range, suggesting long free carrier lifetimes, and a low defect density. Given the good epitaxial layer quality after bonding, we can therefore attribute the lack of continuous wave amplification to the self-heating of the device. Indeed, thermal simulations show that there is substantial self-heating of the device due to the high thermal resistance of the DVS-BCB bonding layer and the SiO₂ buried oxide layer. At the conference we will discuss several specific methods for addressing and improving this thermal behaviour.

V. CONCLUSIONS

In this paper we present for the first time the study of a nanophotonic III-V/SOI amplifier based on a 100nm thick III-V strip waveguide layer bonded on top of a silicon waveguide circuit. The device is optically pumped through the silicon waveguide layer. Self-heating of the device is currently a limiting factor, preventing net optical gain. Methods to alleviate the self-heating will be discussed at the conference. While no net gain has yet been achieved, the device in its current form can already be used as a broadband all-optical switch, given the low pump power required (a few mW) to nearly bleach the absorption.

VI. ACKNOWLEDGEMENTS

G. Roelkens acknowledges the Fund for Scientific Research Flanders for a post-doctoral grant. This work was partly carried out in the FP7 HISTORIC project.

VII. REFERENCES

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