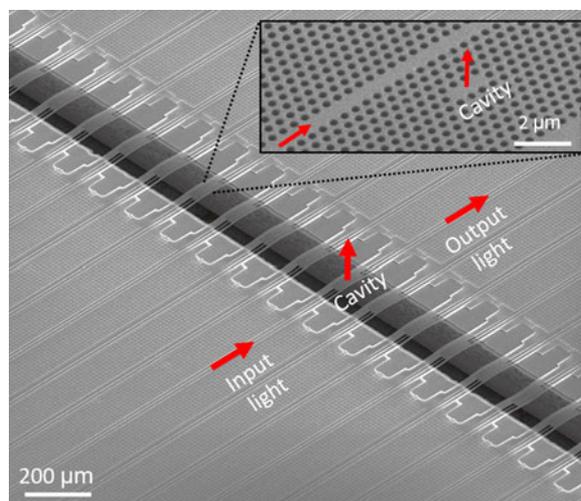


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Kumar Saurav
Sulakshna Kumari
Nicolas Le Thomas



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CMOS Fabricated Large Array of Free Standing Substrate-Less Photonic Crystal Cavities for Biosensing Applications

Kumar Saurav,^{1,2} Sulakshna Kumari,^{1,2} and Nicolas Le Thomas^{1,2}

¹Photonics Research Group, Ghent University-imec, 9052 Ghent, Belgium

²Center for Nano- and Biophotonics, Ghent University-imec, 9000 Ghent, Belgium

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Abstract: In this paper, we present a methodology to postprocess a large array of a few hundred nanometer thin photonic membranes that were fabricated using complementary metal-oxide-semiconductor (CMOS) technological platform. The postprocessing results in local removal of the silicon substrate and of the buried oxide, which provides a free access from both side of the photonic structures. The membranes are patterned with photonic crystal cavities by deep ultraviolet lithography. We show that the proposed process is compatible with the integration of micrometer-sized SU8-based polymer waveguides. These polymer waveguides, together with high index contrast adiabatic nanometer-sized silicon inverted tapers, act as spot size converters. In addition, although a significant number of processing steps is required to achieve such free-standing substrate-less cavities, the quality (Q) factors of the cavities that is of the order of a few thousand remains unaffected.

Index Terms: Biosensors, fabrication and characterization, nanocavities, photonic crystals, silicon nanophotonics, waveguide devices.

1. Introduction

Photonic crystal (PhC) cavities have been intensively investigated in recent years for biosensing applications due to their high quality (Q) factor and low mode volume (V) [1]–[11]. High Q factor and low V enables enhanced light-matter interactions in the cavity mode volume and can in principle provide fast label-free detection with high sensitivity. In particular, PhC cavities patterned in thin membrane of silicon benefit from ultra high Q factor, low V, convenience in integration with waveguides, small footprint and compatibility with complementary metal-oxide-semiconductor (CMOS) fabrication platform [12]–[19]. With such assets, these cavities are potential candidates as nanoscale refractive sensors (RI) for various biosensing applications such as accurate diagnosis, drug discovery, toxicity issues, single molecule detection, etc.

Decreasing the sensing volume V, challenges the transportation of analytes with standard integrated microfluidic channels as the velocity of fluid vanishes at the channel wall [20], [21]. Depending on the concentration of the analytes, the time that these analytes require to diffuse from the bulk solution to the sensor surface can vary from days to even years till the total flux of the analytes gets transported on the surface of the sensor [21]. This mass transportation problem significantly slows down the detection speed. As a result, there is a need for sensor architectures in which the transportation of analytes to the sensor surface can be done more effectively.

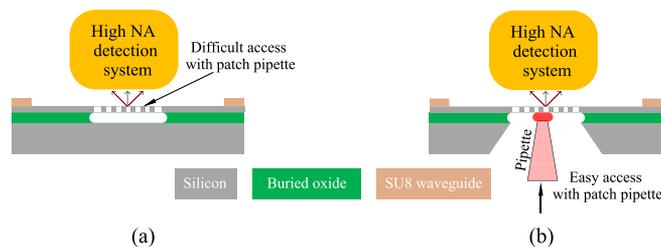


Fig. 1. Schematic of an integrated PhC cavity cross-section (a) highlighting the congestion of the high NA signal detection system and (b) of the microdroplet transportation system of the analytes.

One of the possible solution is to transport the analytes in small amounts toward the cavity surface with available dispensing techniques, e.g., micropipetting or droplet spotting [22]–[26]. PhC cavities with a free access from both sides benefit from ease in the transportation of analytes and simultaneous detection of signal variation induced by the analytes. Moreover, the photodetector can be integrated on one side of the PhC cavity while the analytes transportation can be carried out from the other side. In order to have a free accessibility from both the sides of the cavity, the substrate below the cavity needs however to be removed locally.

Note that in general, biomolecules are in aqueous environment, which can drastically reduce the Q factor of the cavity due to light absorption [27], [28]. Such a detrimental effect can be advantageously minimized by the proposed local transportation approach.

PhC structures without silicon substrate has been reported earlier by Huang *et al.* [29]. These authors have used a sensor window of $200 \times 200 \mu\text{m}^2$ silicon nitride membrane whose silicon substrate was etched before performing e-beam lithography (EBL) to pattern the photonic structure. However, the removal of the substrate below the cavity before the structure patterning is not compatible with a CMOS fabrication due to contamination issues. Also, it should be noted that the structure was patterned on a silicon nitride membrane and the etching solution which is used to remove local silicon substrate has very high selectivity against silicon nitride. Therefore, this process might not be suitable when the top layer is patterned in silicon.

Elewout *et al.* [30] have reported an integrated optical pressure sensor where they have used a silicon based ring resonator whose substrate was also removed. In this case, a stack of protection layer (against the top silicon etch) was deposited on the top surface which may not be compatible with various structures present in device layer (e.g., polymer waveguides, active devices etc). This compatibility issue comes due to difficulties in the complete removal of the protection layer in a high selective way.

Here, we introduce a fabrication process flow that allows us to locally remove the substrate below PhC without jeopardizing the top device layer. This process yields an array of CMOS fabricated silicon PhC cavities free of substrate with a window size as large as $3.5 \text{ mm} \times 50 \mu\text{m}$. This air suspended array can contain more than 150 PhC cavities coupled to access waveguides which is compatible with a large scale biological sensing. It offers the opportunity for the implementation of various types of cavity design that targets different dedicated applications. Although we present the process for substrate-less fabrication at the chip level, it can conveniently be transposed at a wafer scale. Importantly, the top layer (device) does not need any kind of masking material, which means that the same process flow can be used for any kind of top layer (e.g., III–V, silicon nitride), as well as for various active devices.

The paper is organised as follows. In Section II, we first describe the fabrication process to etch locally silicon substrate below the integrated PhC cavity. Next, we show that this process is compatible with the patterning of SU8 waveguides using contact photolithography. Finally, the local buried oxide (BOX) is removed below the cavity to make it free-standing. In Section III we experimentally compare the transmission spectra of air-suspended PhC cavity with and without substrate. We show that the Q factor of both cavities remain unaffected despite of the various processing steps, which makes our device architecture a good candidate for sensing applications.

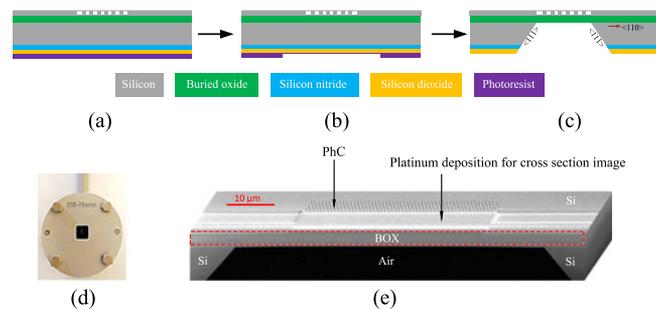


Fig. 2. Schematic of (a) spin coating of photoresist on top of hard mask, (b) dry etch of hard mask after contact photolithography, and (c) silicon substrate anisotropic wet etch in KOH. (d) Camera image of holder containing the chip whose backside is exposed. (e) SEM image of the cross section of PhC cavity after removal of substrate.

2. Device Fabrication

The PhC cavities were fabricated on a silicon-on-insulator (SOI) wafer with a 220 nm thick top silicon layer (device layer) on a 2 μm thick BOX layer. The SOI stack is supported by a 740 μm thick silicon substrate. The fabrication was done on $\langle 110 \rangle$ crystalline plane of silicon in a Multi Project Wafer (MPW) run at imec by using 193 nm deep ultraviolet lithography and 200 mm SOI wafers [31]. After lithography, the exposed structures were dry etched and the patterned wafer was diced into smaller chips of size 2.5 cm \times 2.5 cm.

2.1 Fabrication of Free-Standing Substrate-Less PhC Cavities

Removing only the BOX layer below the PhC makes the cavity free-standing already but it is difficult to access the cavity surface for analyte transportation as shown in Fig. 1(a). This difficulty arises when a detection system of high numerical aperture (NA) is used to optimize the signal to noise ratio. To solve analyte transportation issue, we first removed the silicon substrate below the PhC cavity before to remove the BOX layer as shown in Fig. 1(b). The red colored droplet below PhC cavity in Fig. 1(b) represents a micro-droplet containing analytes. The resulting free-standing cavity without substrate eases up the analyte transportation to the cavity surface. This section will explain all the necessary steps to implement an array of integrated PhC cavities with SU8 polymer waveguide on top of a silicon inverted taper without any BOX or silicon substrate below photonic crystal area. Fig. 2 shows the procedure to completely remove the silicon substrate below a PhC cavity. In order to protect the device layer from any damage during the different post processing steps, at start of each process a thick photoresist AZ9260 is spin coated at 1000 rpm and baked at 100 $^{\circ}\text{C}$ for 3 minutes.

The local substrate removal below the PhC was done in three step: a thin film deposition on the backside of a thinned and polished chip, which acts as a hard mask (Fig. 2(a)); a patterning on the hard mask to define the etching window by photolithography (Fig. 2(b)); and a wet etching in potassium hydroxide (KOH) (Fig. 2(c)) to remove the silicon substrate. At first, we thinned down the chip to 240 μm by mechanically lapping the standard SOI chip. The backside of the chip is then polished by using a chemical slurry which contains 30 nm silica particles.

KOH is normally used as the wet etchant for silicon. In order to etch the silicon substrate locally, the pattern has to be transferred onto a suitable mask by using contact photolithography. In this case, the use of a photoresist is not suitable as a masking material as it gets immediately removed by KOH in a few seconds. One possible solution is to use silicon dioxide as a masking material if the etching duration is short (< 30 minutes for shallow etch) but for a through-chip etch (> 3 hours), this layer also gets etched away in KOH. For deep etch, silicon nitride layer must be employed which has a negligible (< 1 nm/hour) etch rate compared to silicon oxide (300 nm/hour) in 20% KOH solution [32], but due to the lattice mismatch between silicon and silicon nitride layers, stress develops in the

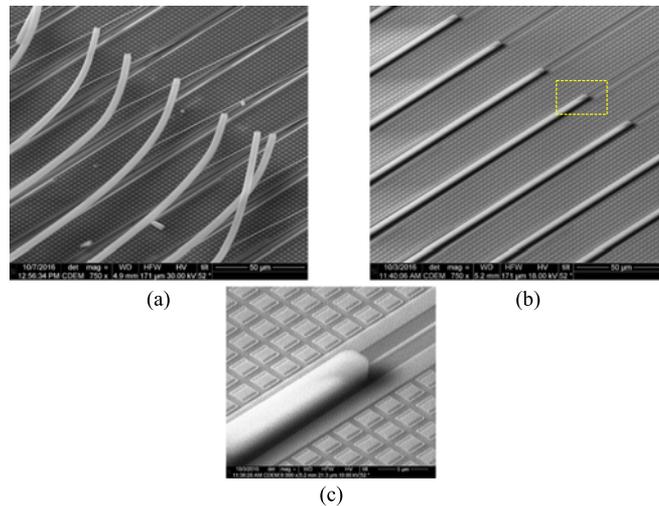


Fig. 3. SEM image of (a) peeling of patterned SU8 waveguide observed after mechanical lapping. (b) Patterned SU8 waveguide after silicon substrate removal. (c) Zoomed in interface of SU8 waveguide and silicon wire waveguide.

subsequent deposited layers. In this case an additional layer of silicon dioxide is deposited between silicon and silicon nitride. Here silicon dioxide layer also acts as a buffer layer between them which minimizes the stress induced effects and improves adhesion. Therefore on the polished backside, we deposit a stack of 500 nm of silicon dioxide and mixed frequency low-stress 600 nm silicon nitride using plasma enhanced chemical vapor deposition (PECVD). The mixed frequency silicon nitride deposition was done by changing the radio frequency (RF) generator frequency while using the same gas and power levels. In the mixed frequency PECVD process, both high (13.56 MHz signal) and low (100 KHz signal) RF frequency was applied alternatively for 6 second and 1 second, respectively. Adjusting the ion bombardment with high and low frequency mixture provides control over the film stress, film density and conformal properties [33]. This allows for densely stacked tensile and compressive layers. For wet etching of the silicon substrate below the PhC cavity, all the photolithographic steps were done on the backside of the chip. The selectivity of silicon etch in the KOH solution between $\langle 100 \rangle$ and $\langle 111 \rangle$ crystalline plane is of the order of 200:1. This produces a characteristic anisotropic V-etch with sidewalls which forms a 54.7° angle with the surface, which leads to a very narrow opening on the top layer as shown in Fig. 2(c). The size of the patterned window on the hard mask depends on the substrate thickness. As in the present case a window size of around $50 \mu\text{m} \times 3.5 \text{mm}$ was required on the device layer, a rectangular window of $305 \mu\text{m} \times 3.75 \text{mm}$ was patterned on the backside by using contact photolithography. Cross and vernier markers located on the top layer of the chip were guaranteeing the high accuracy of the alignment of the photolithographic step, which was done in the backside alignment mode. The hard mask of the patterned window was dry etched with SF_6 and O_2 gases in a Reactive Ion Etching (RIE) chamber.

After removal of the hard mask, the SOI chip was placed in a holder (see in Fig. 2(d)) that protects the top side and exposes the backside window to the etching solution. The black dotted rectangle at the centre of holder highlights the backside of the chip (lithographically patterned). Since, the etch rate of silicon in the 20% KOH solution is around $1.3 \mu\text{m}/\text{min}$ and the device layer consists of 220 nm of silicon, even a very diluted drop of the solution can jeopardize the photonic structures by etching away the full device layer in a fraction of second. The holder was immersed in a 20% KOH solution at 80°C to etch the exposed silicon window and the whole system was stirred at 50 rpm. The holder was removed from the KOH solution after the etching of the silicon stops at the BOX layer. The chip was then removed from the holder and rinsed in deionized water thoroughly. Fig. 2(e) shows a scanning electron microscope (SEM) image of the cross section of the fabricated

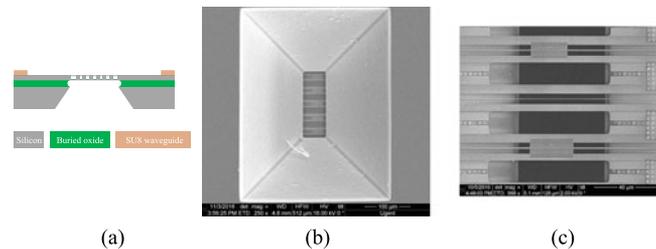


Fig. 4. (a) Cross section of schematic of BOX etch after SU8 waveguide patterning. SEM image of substrate-less suspended PhC cavity array (b) from backside (i.e., viewed from the side of the substrate) and (c) from top side.

PhC cavity without local silicon substrate. The trapezoidal window below the BOX layer represents the area with no silicon substrate and is a characteristic signature of anisotropic silicon etch. The red dotted rectangular window highlights the BOX layer below PhC cavity. A platinum layer was deposited on the top layer for sectioning purpose through the PhC structures.

2.2 Patterning of SU-8 Waveguide on Top of Inverted Silicon Adiabatic Tapers

Efficient injection (coupling) of light from an optical fiber to a photonic integrated circuit (PIC) can be done by integrating coupling structures directly on the chip. These possible coupling structures can be classified into two main groups depending on the physical direction in which the fiber is coupled to PIC: in-plane and out-of-plane coupling. Typical in-plane coupling schemes is based on horizontal spot size converters, where the fiber is positioned in the chip plane. For out-of-plane coupling, grating couplers is widely employed which couples light from a different direction (mainly vertical) than that of the waveguide. Since these grating couplers have a limited bandwidth, we have considered polymer waveguide couplers based horizontal spot size converters which is compatible with an end-fire coupling scheme. Among various horizontal spot size converters, we choose SU8 based waveguide couplers for which an efficient light coupling has already been successfully reported [34], [35].

The goal of using SU8 polymer waveguide is to efficiently couple light from an optical lensed fiber into a strongly confined high index contrast 450 nm wide silicon waveguide. The spot-size conversion is achieved by using a silicon adiabatic taper with the taper tip width of 150 nm covered by a low-index SU8 waveguide of width 3 μm . Once the mode is converted from the SU8 polymer waveguide to that of the higher high-index waveguide, it can be coupled much more efficiently into the wire waveguide and hence into the PhC cavity. The coupling efficiency of such spot size converter improves with the reduction in the taper tip width. However, a minimal feature size of the tip width is imposed by standard deep UV lithography due to technological challenges.

The SU-8 polymer waveguide can be patterned on the adiabatic silicon inverted taper with contact photolithography on the top layer. Since removal of the silicon substrate locally makes the device layer very fragile, patterning of the SU8 waveguide before thinning the substrate would be an obvious choice, but after thinning of the silicon substrate, patterned SU-8 waveguide peeled off from the device layer, as shown in Fig. 3(a). For thinning, the chips were bonded on a thick glass plate with hot wax. The peeling of the SU8 waveguides occurs when the chip is removed after thinning from the glass plate due to surface tension between the hot melted wax and the SU8 surface. That is why we opted to pattern the SU-8 waveguide after the complete substrate removal. The patterning of the SU8 waveguide at this stage also allowed a thorough cleaning of the substrate-less chip, which removes any residual layer of photoresist and particles from device layer. Fig. 3(b) shows the SEM image of the access waveguide array with patterned SU8 waveguide after complete removal of the substrate. In Fig. 3(c), a zoom in image of the yellow dotted rectangular area marked in Fig. 3(b) highlights the clear interface between the silicon wire waveguide and the SU8 waveguide.

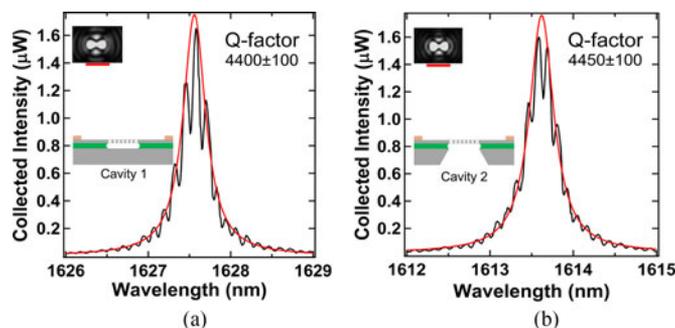


Fig. 5. Transmission spectra of suspended PhC cavity (a) with substrate and (b) without substrate, respectively, (Inset) Intensity pattern of the cavity field at resonance; the red scale of the image corresponds to $1.5 \mu\text{m}$.

2.3 Removal of Silicon Dioxide Layer Below PhC Cavity

After patterning the SU-8 waveguide on the top of silicon inverted taper, the local BOX was etched in 40% Hydrofluoric (HF) acid (see Fig. 4(a)). The chip was then dried using a Critical Point Drier (CPD) in order to avoid any stiction between the waveguides. Fig. 4(b) and (c) shows the SEM images of a substrate-less suspended PhC cavity array from the back and top respectively. Later, for the end-fire coupling the chip was cleaved through the SU8 waveguide around $150 \mu\text{m}$ far from the start of the silicon tapers.

3. Experiment and Result

To characterize the PhC cavity structures, we have implemented a standard end-fire optical setup that also allows collection of the out-of-plane scattered light from the cavity surface. For comparison between transmission of PhC cavity membrane with and without silicon substrate, we have chosen the well-known L3 cavity due to its high fabrication tolerance in terms of design. A L3 defect in a PhC pattern is created by removing three holes along Γ K direction of a triangular lattice.

The photonic structure is excited with a TE-polarized, monochromatic diode laser that is tunable in the wavelength range of 1500 nm–1640 nm. The integration of the spot size converter decreases the coupling loss in a wire waveguide by factor of 15. Thus, this spot size converter also efficiently couples input light into the wire waveguide which excites cavity via a W1 waveguide in PhC cavity structure. The light radiating out of the cavity surface is collected through a high numerical aperture (0.95) microscope objective and detected with an infrared camera (Xenics) and InGaAs photodetector. Imaging the cavity surface allows us to monitor the radiated field from the cavity surface. Fig. 5(a) and (b) shows the transmission spectra of two PhC cavity membranes where cavity 1 is free-standing with substrate and cavity 2 is also free-standing but without substrate. The black curve in the figure is the measured intensity collected from the top cavity surface and red curve is the Lorentzian fit of the transmission spectrum.

The oscillation in transmission spectra of the cavities is due to Fabry-Perot interference caused by reflections at the sample facets and at the interface between the PhC pattern and access waveguides. Both cavities had a measured lattice constant of 460 nm and hole radius of 112 nm. Inset of Figure Fig. 5(a) and (b) shows the intensity pattern of L3 cavity emission in far field. We can infer from the experimental cavity spectra that the Q factor extracted by Lorentzian fit of out-of-plane spectra and mode of substrate-less L3 cavity is similar for cavity 1 and cavity 2. The difference in resonance wavelength of both cavities is due to the difference in location of the individual chips on an entire wafer.

4. Conclusion

In conclusion, we have developed a process flow to realize substrate-less air suspended PhC cavity which can find many applications in biosensing. We have demonstrated that the integration of a spot size converter which in our case consisted of SU8 waveguide on the top of silicon inverted adiabatic taper is compatible with this process. We have verified that the process flow which is required for such an integrated sensor architecture does not affect the intrinsic properties of the PhC cavity such as the Q factor. We envision that our process will foster the implementation of the unique properties of the PhC cavities for new biosensing applications.

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